**Verification of PI6ULS5V9617A IBIS model**

1. **Introduction:To verify the correlation between the ibis model and hspice model, we need to do some simulations:**
2. **Port A to Port B: Vccb=3.3V.**

PI6ULS5V9617A

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

SCL**B**

**SCL\_C**

**SDA\_C**

SDA**B**

**SCL\_C**

**SDA\_C**

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

SCL**A**

**SCL\_C**

**SDA\_C**

SDA**A**

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

1. **The frequency of signal is 1MHz:** Vin input 0 pulse (0 pwr\_a 0 1n 1n 499n 1u)

Add **1KΩ** resistor between the output and VDD and **50p** capacitance to the OUTPUT.

1. Simulation **without** package data;
2. Simulation **with** package data.
3. **The frequency of signal is 0.2MHz:** Vin input 0 pulse (0 pwr\_a 0 0.01u 0.01u 2.49u 5u)

Add **1KΩ** resistor between the output and VDD and **200p** capacitance to the OUTPUT.

1. Simulation **without** package data;
2. Simulation **with** package data.
3. **Port B to Port A:**

**The frequency of signal is 1MHz:** Vin input 0 pulse (0 pwr\_a 0 1n 1n 499n 1u)

Add **1KΩ** resistor between the output and VDD and **50p** capacitance to the OUTPUT

PI6ULS5V9617A

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

SCL**A**

**SCL\_C**

**SDA\_C**

SDA**A**

**SCL\_C**

**SDA\_C**

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

SCL**B**

**SCL\_C**

**SDA\_C**

SDA**B**

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

1. **Vcca=1.8V, Vccb=3.3V**
2. Simulation **without** package data;
3. Simulation **with** package data.
4. **Vcca=3.3V, Vccb=3.3V**
5. Simulation **without** package data;
6. Simulation **with** package data.
7. **Conclusion:**

For the verification, the simulation results of IBIS model can match quite well with the HSPICE model at different simulating conditions.

1. **Simulation Result:**
2. **Port A to Port B:** Vcca=1.8V, Vccb=3.3V
3. The frequency is 1MHz and add 50p capacitance to the OUTPUT.
4. Simulation **without** package data;



1. Simulation **with** package data.



1. The frequency is 0.2MHz and add 200p capacitance to the OUTPUT.
2. Simulation **without** package data;



1. Simulation **with** package data.



1. **Port B to Port A:**
2. Vcca=1.8V, Vccb=3.3V
3. Simulation **without** package data;



1. Simulation **with** package data.



1. Vcca=3.3V, Vccb=3.3V
2. Simulation **without** package data;



1. Simulation **with** package data.

