

## Type-C application using PI3USB30532 and PI3USB31532

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## 1.0 Introduction

The PI3USB30532, PI3USB31532 type-C cross switch family is developed using cutting-edge technology to achieve high performance of DP 1.2, DP 1.3, USB 3.0, USB 3.1 signals in type-C applications. PI3USB3X532 is fully compliant to type-C specifications. PI3USB3X532 was first to the market and successfully designed in many and various applications, such as notebook, tablet, AIO, PC, monitor, HDTV, docking stations, etc. PI3USB3X532 was also designed in Intel reference schematic and designed in Intel customer reference demonstration tablet.

## 2.0 Why passive MUX (PI3USB3X532) is better than active MUX in notebook design?

The market requests notebooks:

- Running for 6-8 hours in battery operation
- Boot-up after power-off for 6-8 days

Intel mobile CPU/chipset can now achieve 6W power consumption, thus:

- The ~0.4W to ~0.6W power consumption from an active MUX is way too high and not reasonable.
- Especially when compared to the <0.003W power consumption from PI3USB3X532, which is a 99% power saving compared to an active MUX.

## 3.0 PI3USB3X532 in source-host: Notebook, tablet, AIO and desktop PC

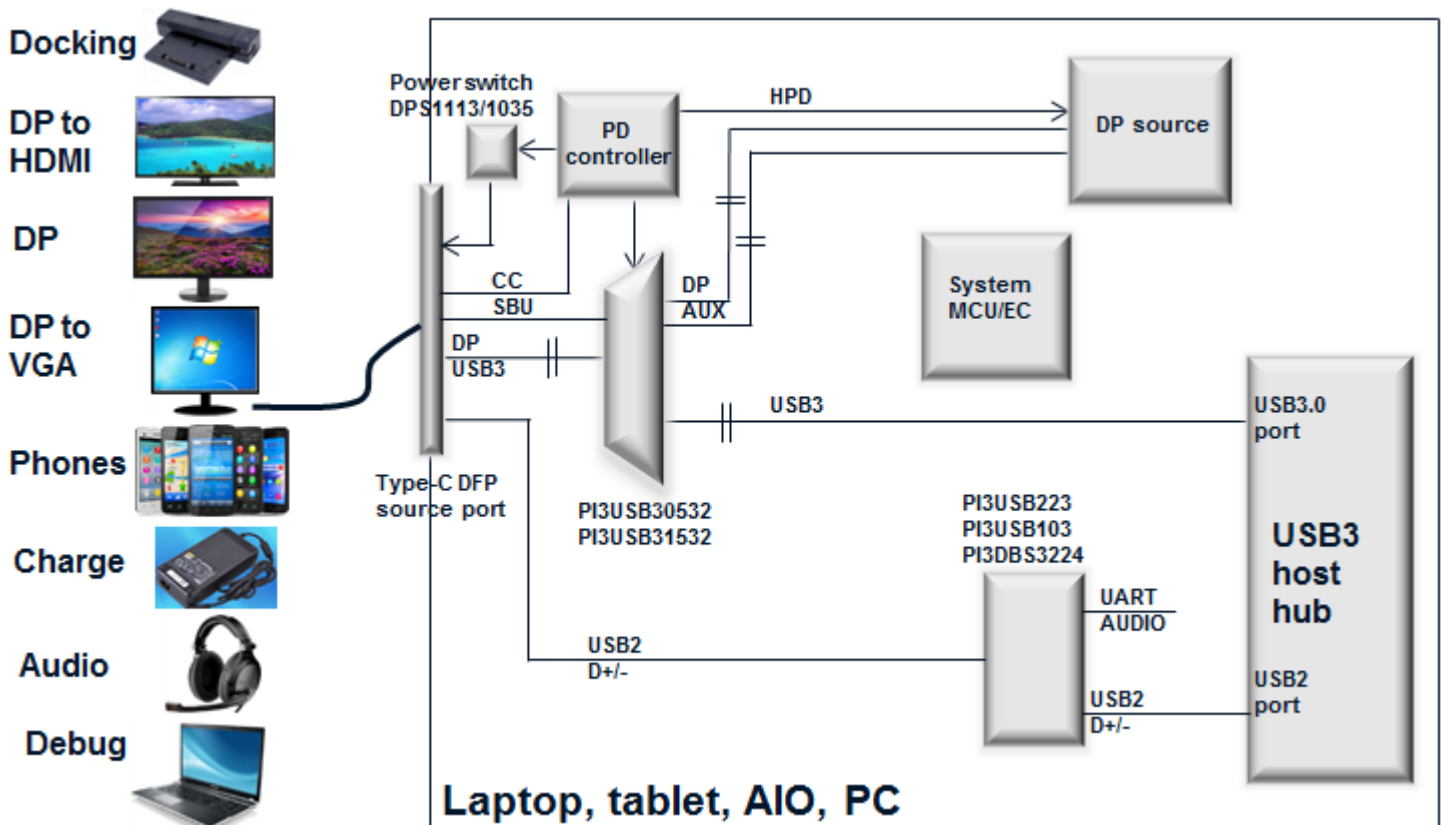


Figure 1, PI3USB30532, PI3USB31532 in notebook, tablet all-in-one and desktop PC

## 4.0 What are the recommended maximum traces for PI3USB3X532 in Intel notebook design?

### 4.1 DP 1.2, DP 1.3

In Intel Kabylake design guideline, Intel recommends maximum 8" DP 1.2 trace without passive MUX and 4.1" with passive MUX as to pass DP 1.2 compliance test.

Intel deducted 3.9" trace from the 8" DP 1.2 trace for the passive MUX, which is conservative for a high performance passive MUX such as PI3USB3X532, as explained in figure 2, figure 3a, figure 3b and in table-1 below.

Based on the PI3USB30532 DP 1.2 eye compliance test results in figure 3a and figure 3b, as well the trace data in figure 2 and table-1, it is recommended as below.

Maximum 6.2" trace for DP 1.2 (5.4Gbps) path, as:

- Intel DP 1.2 source → PI3USB3X532 → type-C connector

Maximum 4.0" trace for DP 1.3 (8Gbps) path, as:

- Intel DP 1.3 source → PI3USB31532 → type-C connector

(Assuming the layout and schematics are as recommended as using 90ohm traces without chokes, etc., and in reasonable system conditions)

### 4.2 USB3.0, USB3.1

Based on the PI3USB30532 USB 3.0 eye compliance test results in figure 4a and figure 4b, as well the trace data in figure 2 and table-1, it is recommended as below.

Maximum 8.5" trace for USB3.0 (5Gbps) path, as:

- USB3.0 host → PI3USB3X532 → type-C connector

Maximum 4.5" trace for USB3.1 (10Gbps) path, as:

- USB3.1 host → PI3USB31532 → type-C connector

(Assuming the layout and schematics are as recommended below and in reasonable system conditions)

**Table 1 the insertion loss of PI3USB3X532 versus Intel trace board**

	Insertion loss of 3" trace on Intel trace board	Per inch	PI3USB30532			PI3USB31532		
			30532: Insertion loss	30532: equivalent trace length (loss of 30532/1" trace)	30532: good-max DP 1.2 trace in Intel 8" trace topology	31532: Insertion loss	31532: equivalent trace length (loss of 31532/1" trace)	31532: good-max DP 1.2 trace in Intel 8" trace topology
Insertion loss at 5Gbps (USB3.0)	-2.1db	-0.70db	-1.2db	1.71" (1.2db/0.70db)	NA	-1.06db	1.51" (1.06db/0.70db)	NA
Insertion loss at 5.4Gbps (DP1.2)	-2.3db	-0.77db	-1.3db	1.69" (1.3db/0.77db)	6.31" (8"-1.69")	-1.23db	1.60" (1.23db/0.77db)	6.40" (8"-1.60")
Insertion loss at 8Gbps (DP1.3)	-3.2db	-1.07db	NA	NA	NA	-1.63db	1.52" (1.63db/1.07db)	NA
Insertion loss at 10Gbps (USB3.1)	-3.96db	-1.32db	NA	NA	NA	-1.68db	1.27" (1.68db/1.32db)	NA

Table 1 the insertion loss of the 3" FR4 differential trace was measured using Intel trace board and Agilent N5230A 20GHz Network Analyzer, as setup in figure-2.

Note:

- The data above is not linear, because the performances vary with different switch-routings and signal-types between PI3USB30532 and PI3USB31532, while PI3USB31532 has better performance than PI3USB30532 mostly at higher speed.
- NA is for not applicable.

### 4.3 The insertion loss of 3" differential trace on Intel trace board

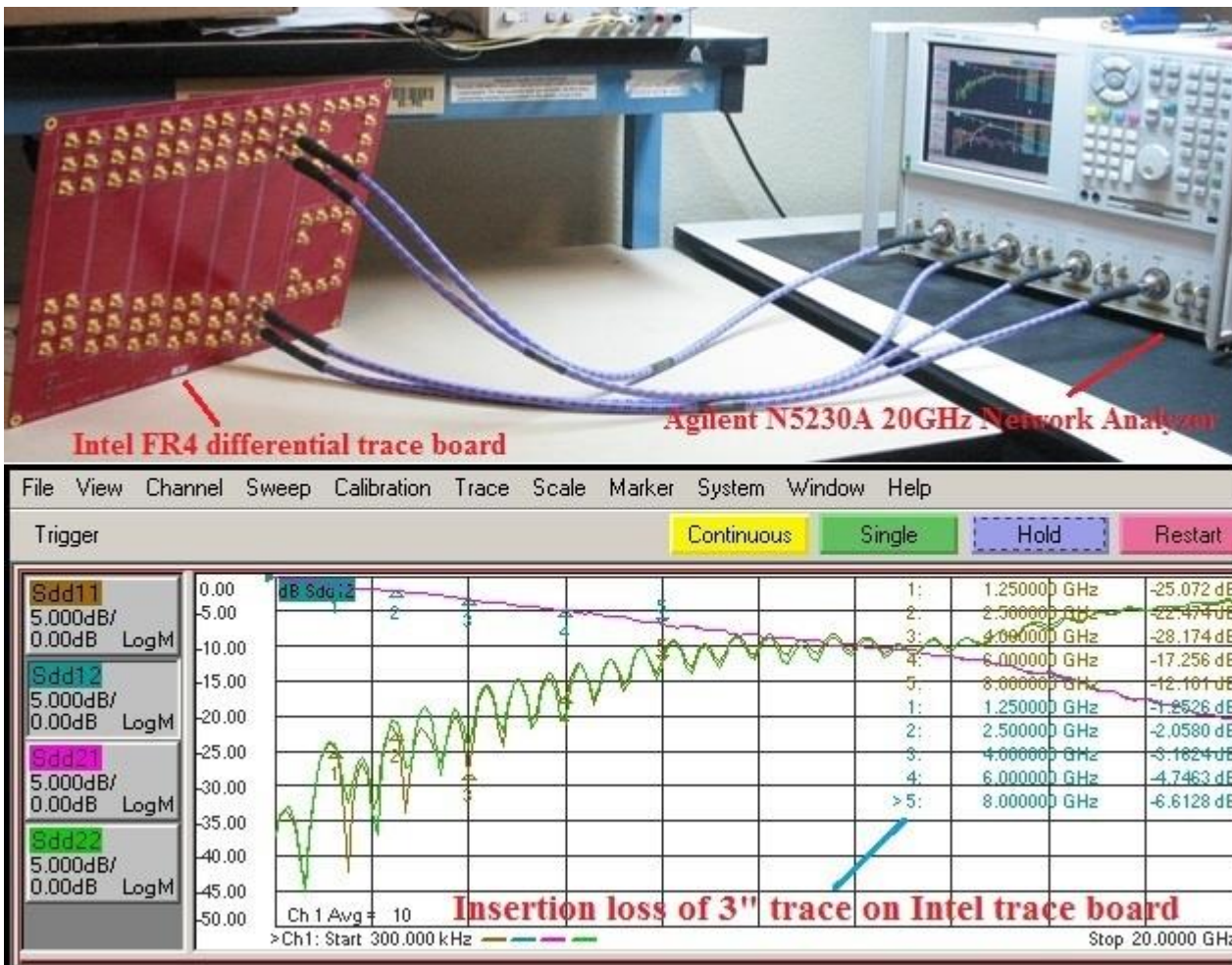


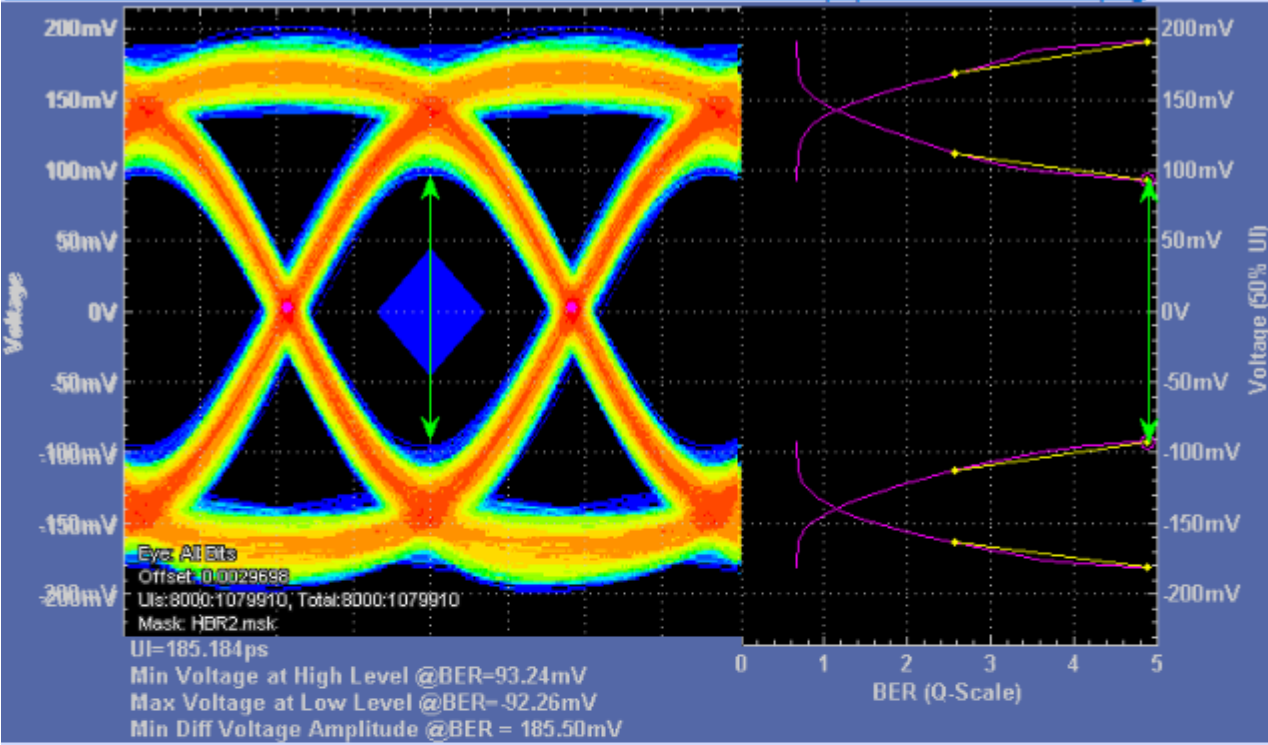
Figure 2 the insertion loss of 3" FR4 differential trace on Intel trace board is measured using Agilent N5230A 20GHz Network Analyzer (chart by James Liu)

### 4.4 The PI3USB30532 Intel Haswell MB DP 1.2 eye compliance test result



Test 3.1 Eye diagram testing

Lane0 CH1 COMP-EYE HBR2 3.5dB SSC 400mV Level0 20usdiv 20pspt MATH\_TP3EQ-1.png



Lane0 CH1 COMP-EYE HBR2 3.5dB SSC 400mV Level0 20usdiv 20pspt MATH\_TP3EQZeroCable-1.png

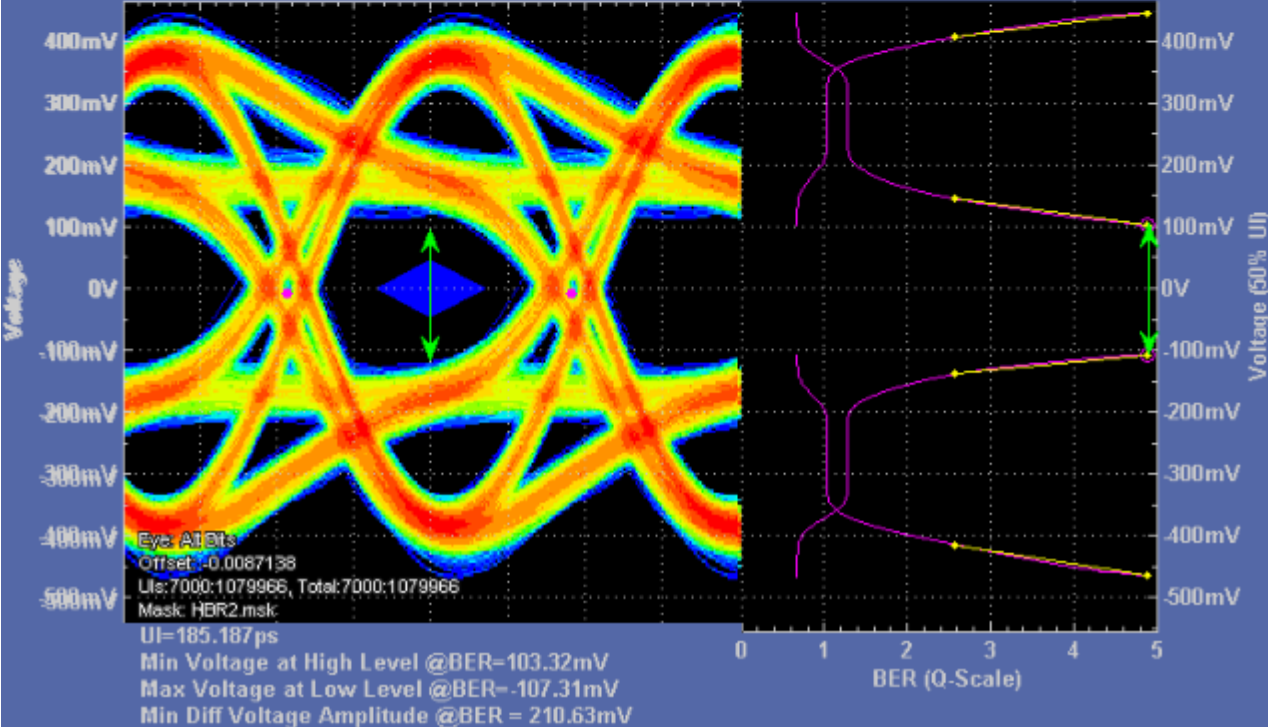
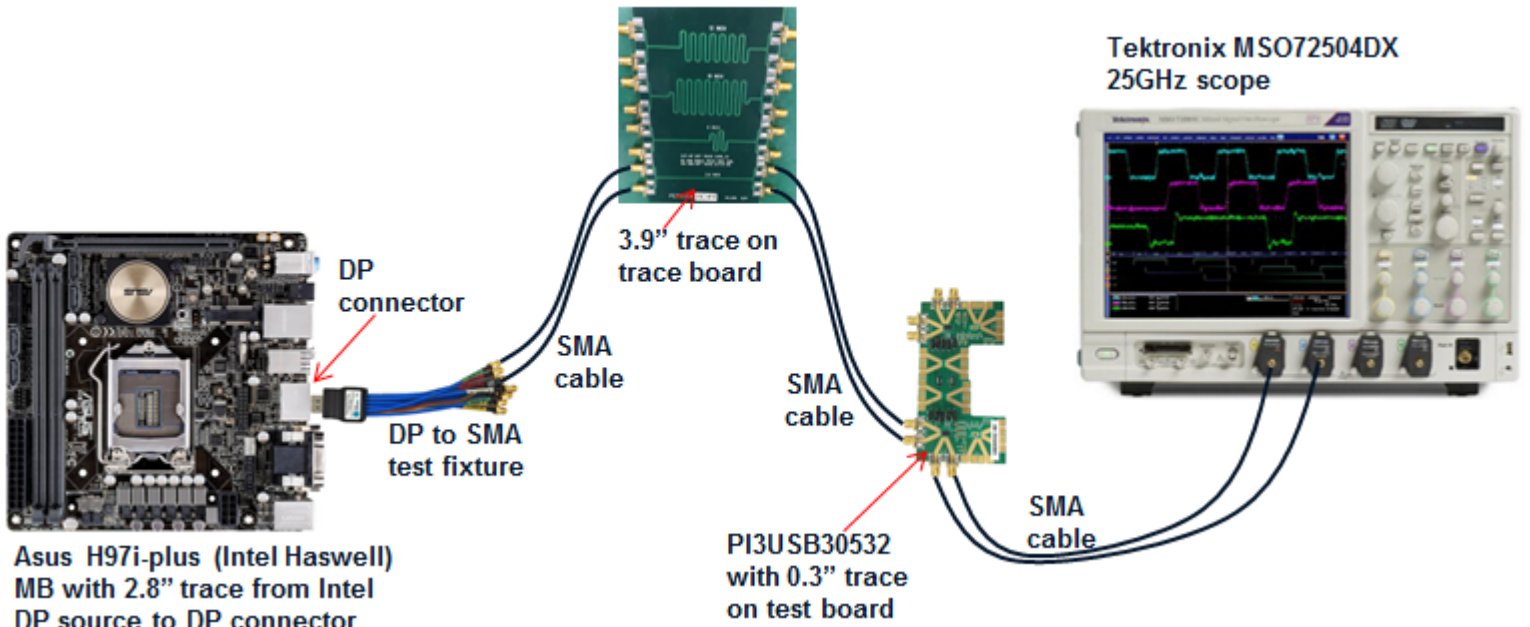


Figure 3a the eye of DP 1.2 (5.4Gbps) compliance test using PI3USB30532 setup (figure 3b) with Asus H97i-plus MB (Intel Haswell) and 7" trace passed the DP 1.2 HBR2 compliance test 3.1 using Tektronix scope at 400mV, 3.5db pre-emphasis. The upper waveform is at T3 with emulation cable in scope. The lower waveform is at T2 without emulation cable (waveform by Jerry Chou).

## 4.5 The test setup of 4.4



Asus H97i-plus (Intel Haswell) MB with 2.8" trace from Intel DP source to DP connector

Figure 3b the test setup of PI3USB30532 with 7" trace (2.8"+3.9"+0.3") using Intel Haswell DP 1.2 source passed DP 1.2 (5.4Gbps) eye compliance test 3.1 as in figure 3a

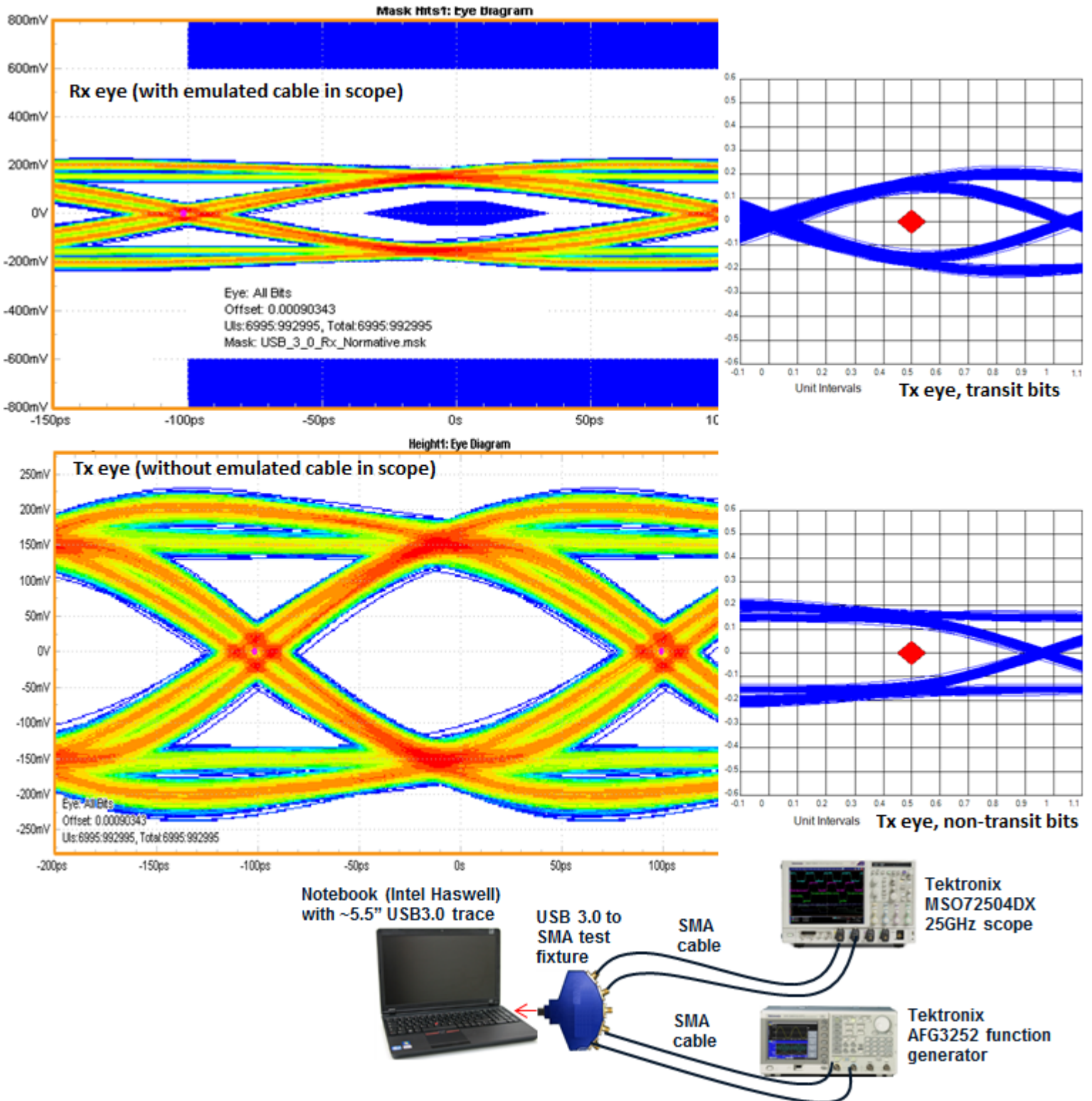


Figure 4a the Tx and Rx eyes passed the USB 3.0 (5Gbps) compliance test at the USB 3.0 connector of notebook (Intel Haswell) without PI3USB30532 EV board. To be compared to figure 4b with PI3USB30532 EVB (waveform by Jerry Chou)



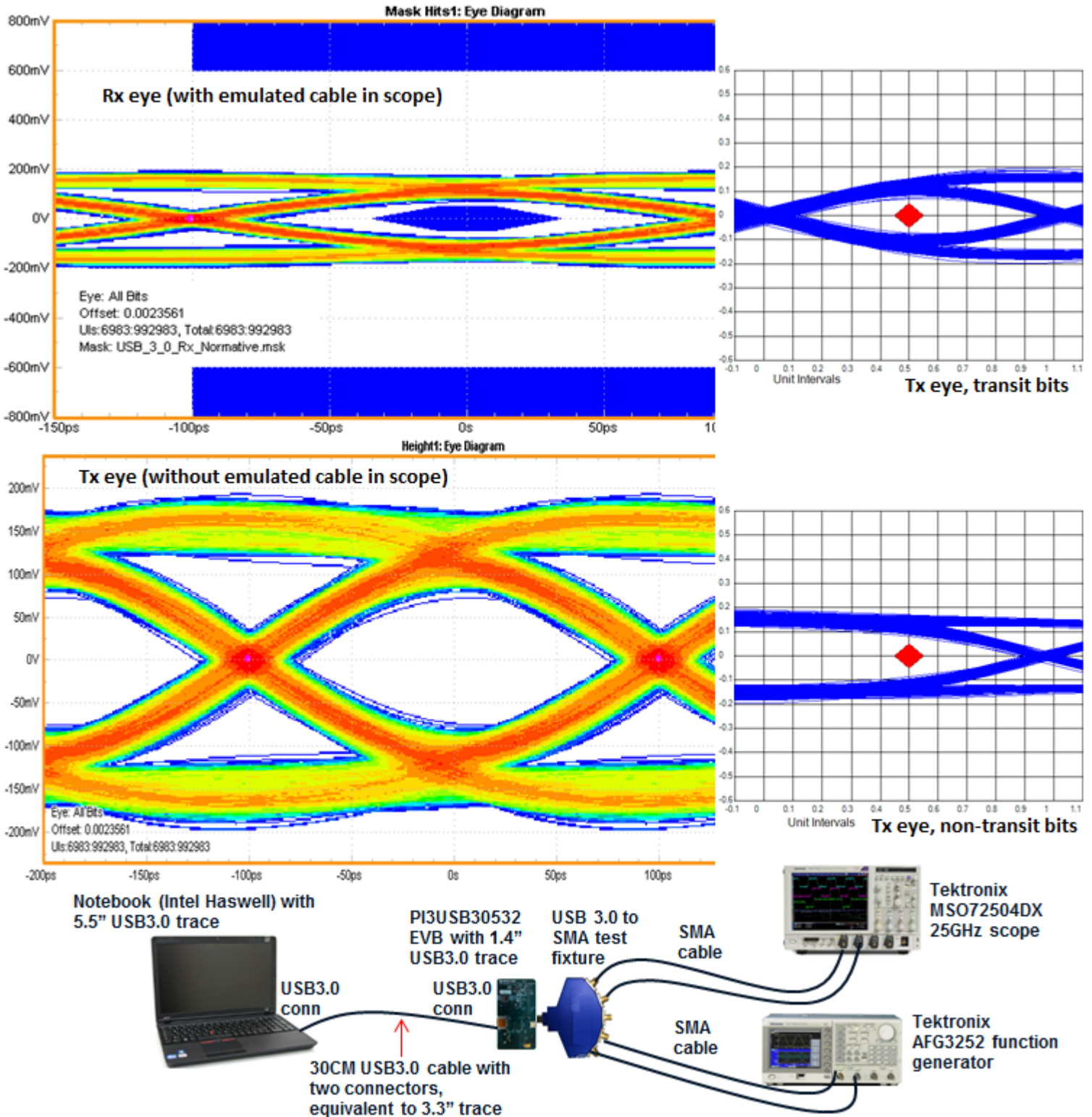


Figure 4b the Tx and Rx eyes passed USB 3.0 (5Gbps) compliance test with 10.2" trace (5.5"+3.3"+1.4") using notebook (Intel Haswell) and PI3USB30532 EV board. To be compared to figure 4a without PI3USB30532 EV board (waveform by Jerry Chou).



## 5.0 PI3USB3X532 in sink-device: Monitor and HDTV

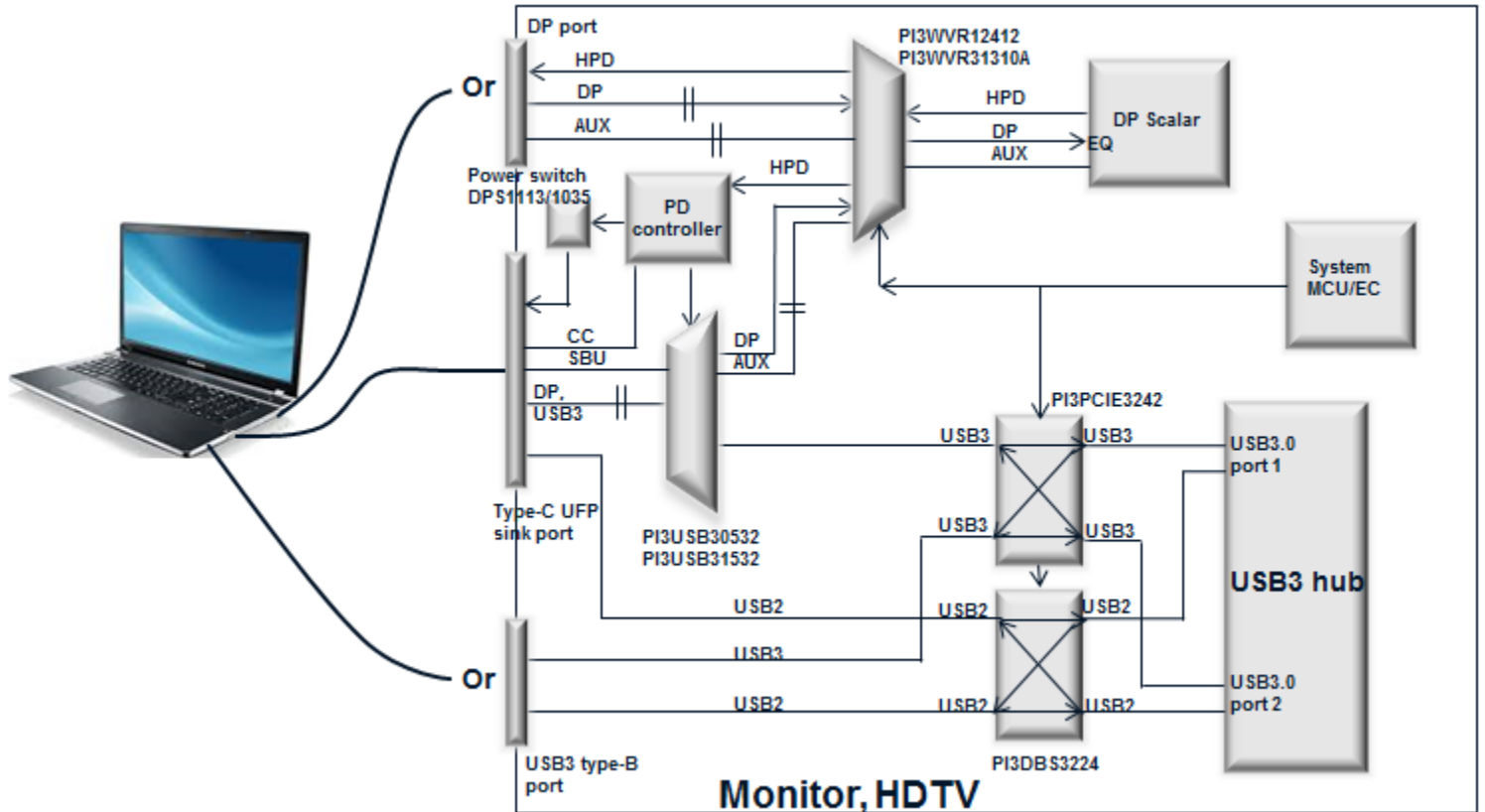


Figure 5, PI3USB30532, PI3USB31532 in monitor and HDTV

- No active DP re-driver and USB3.0 re-driver needed in type-C MUX (PI3USB30532) or between the switches in cascading (PI3USB30532, PI3WVR12412, PI3PCIE3242).
  - Because there are sufficient total source and sink equalization, as:
    - Up to 9db output pre-emphasis (equalization) in DP source and USB3.0 Tx
    - Up to 9db input equalization in DP scalar and USB3.0 Rx receiver.
  - The total 18db equalization in source and sink is sufficient to compensate the estimated total insertion loss from the topology in figure 5:
    - Max 7.7db from total 10” traces
    - Max 4db from 2m type-Cable
    - Max 1.5db from PI3USEB30532
    - Max 1.5db from PI3WVR12412 or PI3PCIE3242

## 6.0 PI3USB3X532 in sink-device: Docking station

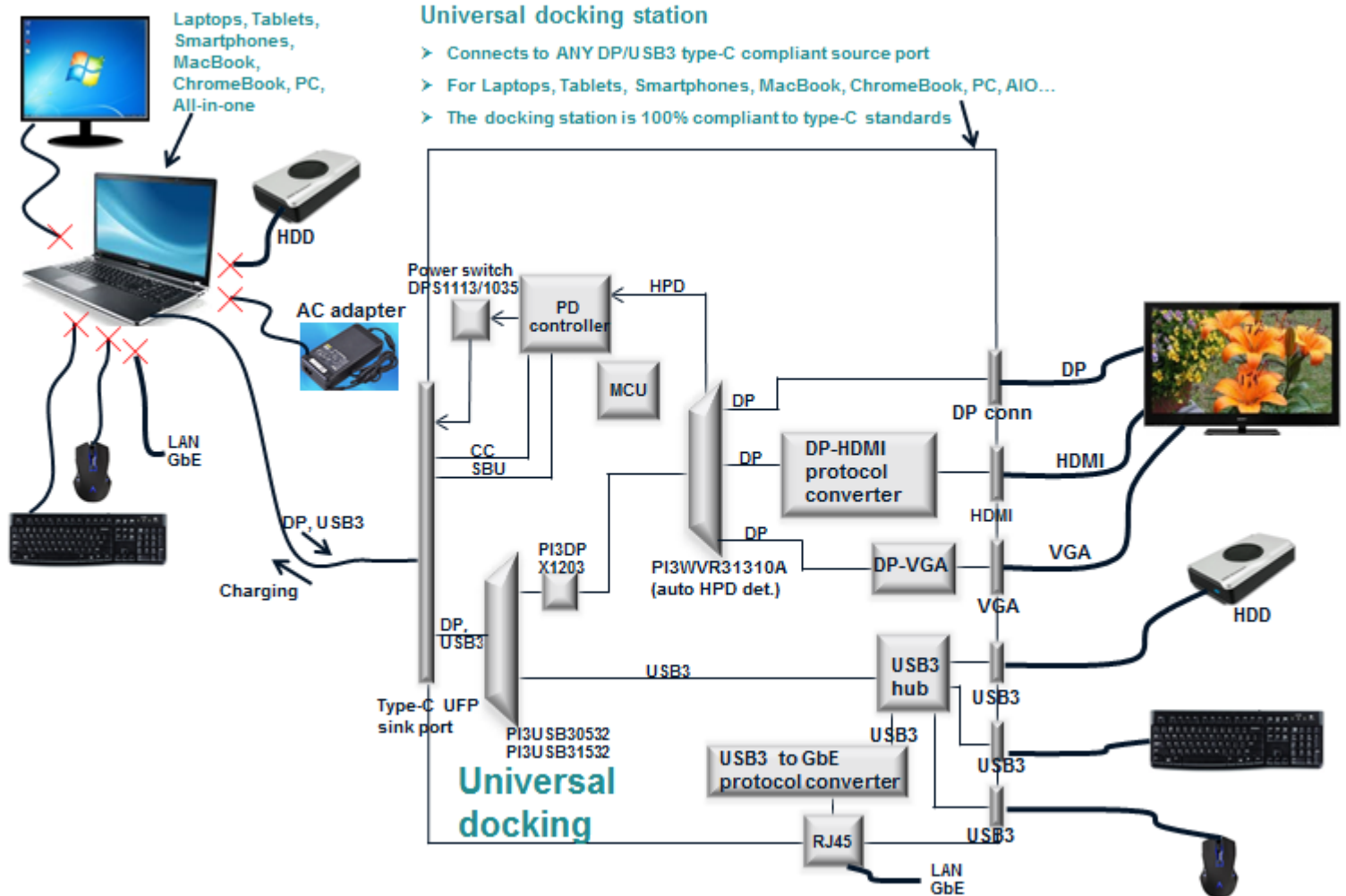


Figure 6, PI3USB30532, PI3USB31532 in docking station

## 7.0 The I2C control of PI3USB3X532

PI3USB3X532 has total three I2C registers as Conf [2:0], which is mapped between the I2C control signals and the configuration tables (source, sink) as in figure-7.

When using I2C interface to control PI3USB3X532, the I2C controller (in PD or MCU) will need sending total three bytes to PI3USB30532 in sequence as:

Start →

→#1 byte for address as “10101000” (assuming A1\_A0 set to 00, while last 0 for write)”

→#2 byte for chip-ID as fixed “00000000”

→#3 byte for Conf [2:0] control as “00000111” (assuming Conf [2:0]=111 as for USB3+DPx2 swapped)

→Stop (must have stop, otherwise uncertainty may occur)

## Configuration Table for Source Application (page 3)

Switch	Open	Open	4 lane of DP1.2	4 lane of DP1.2 Swap	USB3	USB3 Swap	USB3 +2 lane of DP1.2	USB3 +2 lane of DP1.2 Swap
Conf[2:0]	000	001	010	011	100	101	110	111

## Configuration Table for Sink Application (page 4)

Switch	Open	Open	4 lane of DP1.2	4 lane of DP1.2 Swap	USB3	USB3 Swap	USB3 +2 lane of DP1.2	USB3 +2 lane of DP1.2 Swap
Conf[2:0]	000	001	010	011	100	101	110	111

## I2C Control register: (page 8)

	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address (First byte is slave address)	1	0	1	0	1	A1	A0	0/1 (W/R)
Vendor ID (Second byte is vendor ID, read only)	0	0	0	0	0	0	0	0
Selection control (Third byte is for selection control, read/write)	0	0	0	0	0	conf[2]	conf[1]	conf[0]

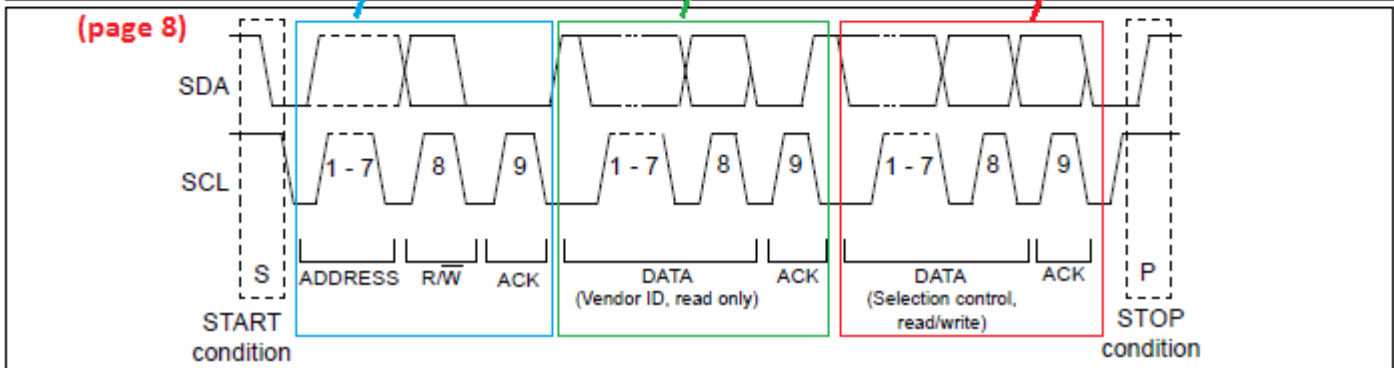


Figure 7, The I2C-control of the configuration table for source-sink (source-sink tables are the same)

### I2C-controls PI3USB30532 in real application

For both source and sink applications, when a type-C plug is plugging into the source or sink type-C connectors with PI3USB30532 and PD, the I2C controller (in PD or MCU) shall I2C-control PI3USB30532 as:

DPx4 only, non-swap:

Start → 10101000 (last 0 for write) → 00000000 → 00000010 → stop

DPx4 only, swapped:

Start → 10101000 → 00000000 → 00000011 → stop

USB3.0 only, non-swap:

Start → 10101000 → 00000000 → 00000100 → stop

USB3.0 only, swapped:

Start → 10101000 → 00000000 → 00000101 → stop

USB3+DPx2, non-swap:

Start → 10101000 → 00000000 → 00000110 → stop

USB3+DPx2, swapped:

Start → 10101000 → 00000000 → 00000111 → stop

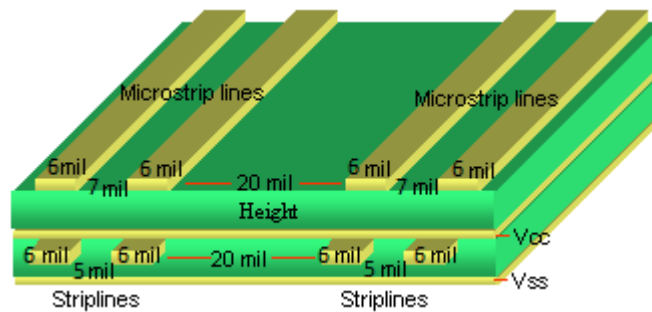
## 8.0 Power and power de-coupling

Use 0.1uf in size of 0402 for all the Vdd (any power pins) pins of the IC device, as close to the Vdd pins as possible, within 2-3mm if feasible.

Use dedicated Vdd and GND planes for to minimize the jitters coupled between channel trough power sources.

## 9.0 Layout guideline

### 9.1 Recommend 90 ohm differential impedance trace for differential DP and USB 3.0 signals



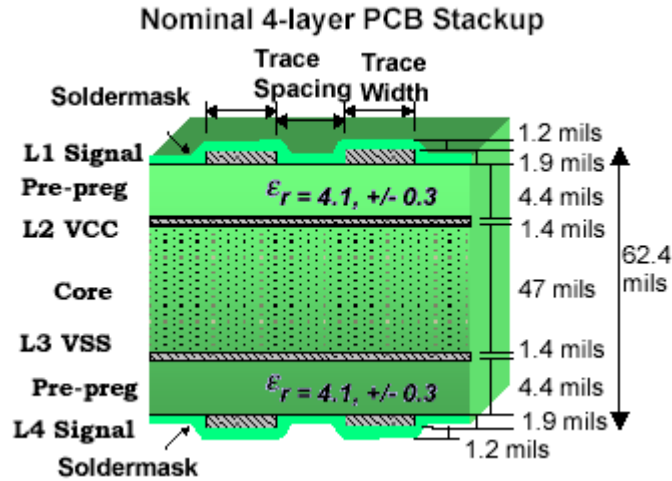
**Figure 8, the trace width and clearance**

- ❑ Use 6-7-6 mils for trace-space-trace for the micro-strip lines (the traces on top and bottom layers) for 90 ohm differential impedance.
- ❑ Use 6-5-6 mils for trace-space-trace for the strip-lines (the traces inside layers) for 90 ohm differential impedance.
- ❑ Use FR4.
- ❑ Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- ❑ For micro-strip lines, using ½ OZ Cu plated is ok.
- ❑ For strip-lines in 6 plus players, using 1 OZ Cu is better.
- ❑ The trace length miss-matching shall be less than 5 mils for the “+” and “-“ traces in the same pairs
- ❑ More pair-to-pair spacing for minimal crosstalk
- ❑ Target differential Zo of 90 ohm ±15%



## 9.2 The PCB Layers Stackup

- No new PCB technology required. Use FR4 is fine.
- Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro strip lines, using ½ OZ Cu plated is ok.
- For strip line in 6 plus players, using 1 OZ Cu is better.



### Stack-up

Plane	Material	Thickness (mil)
Solder mask	Mask paint	1.2
Signal	Copper	1.9
Prepreg	2116	4.4
Vcc	Copper	1.4
Core		47
Vss	Copper	1.4
Prepreg	2116	4.4
Signal	Copper	1.9
Solder mask	Mask paint	1.2
Total		62.4

## 9.3 The Layout Guidance for the Trace Routings

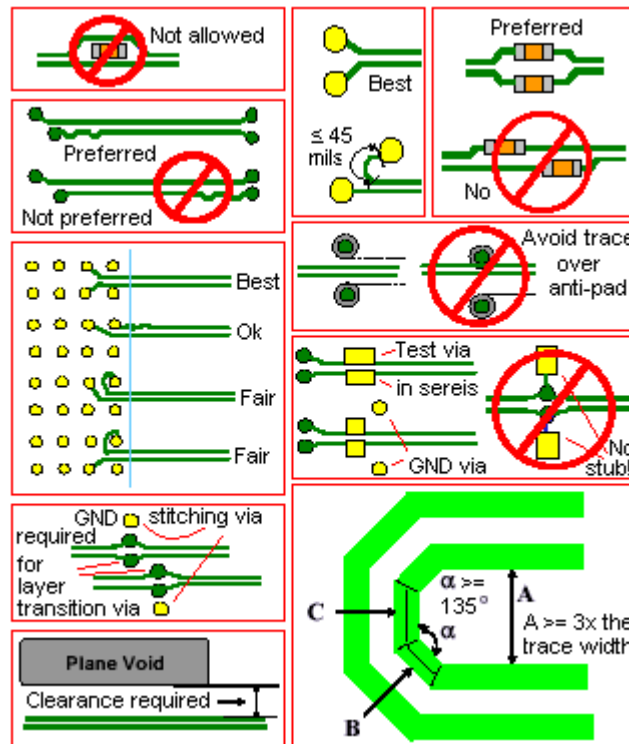


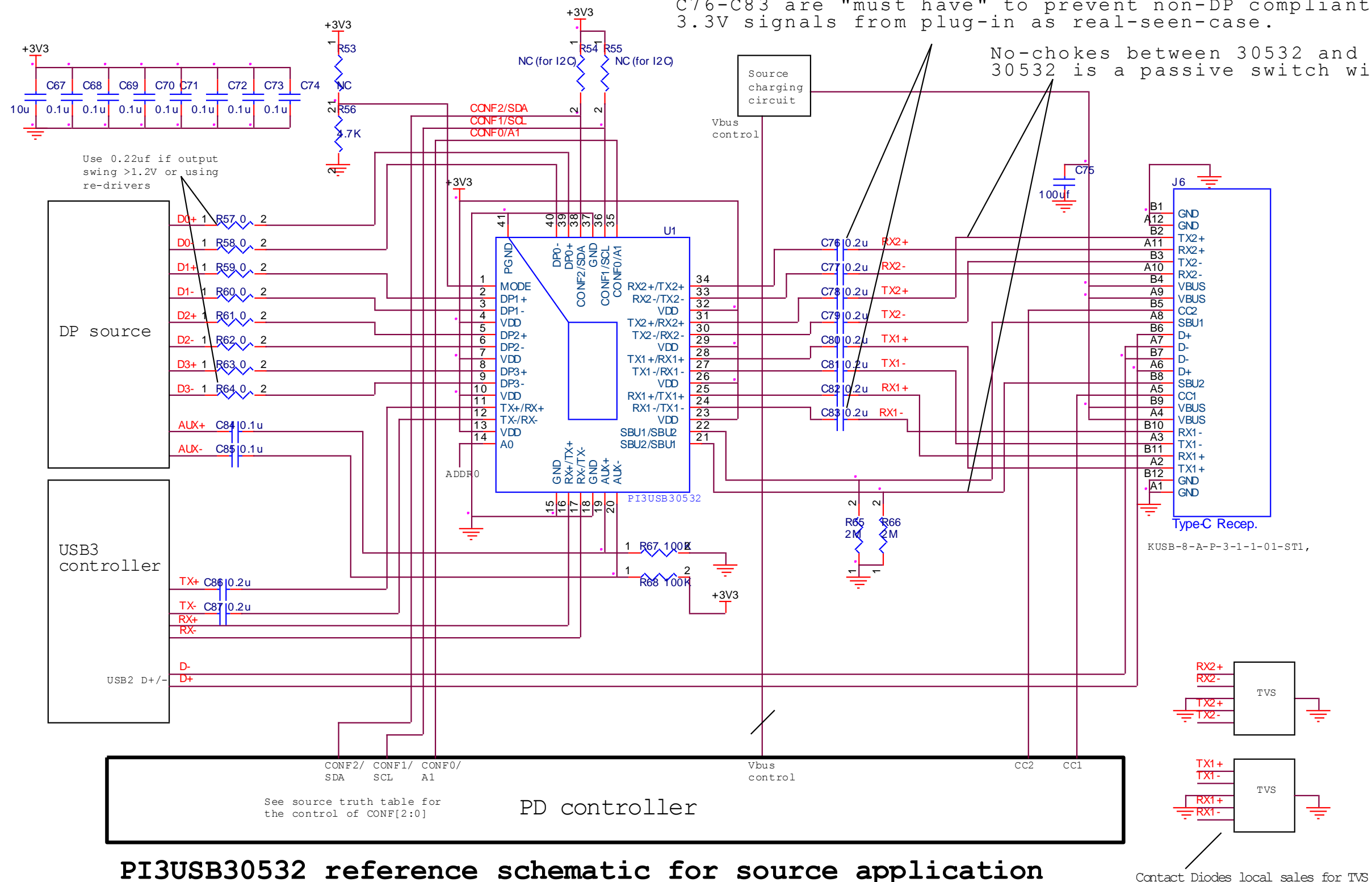
Figure 10, The layout guidance for the trace routings

- Don't use EMI chokes, because PI3USB30532 and PI3USB31532 are passive switches not having EMI issues.
- The differential traces shall be away from the strong EMI source and devices, such as TTL, switching-power traces and devices, with at least 30mil to 50mil space.
- No other components shall piggy ride on the differential traces.

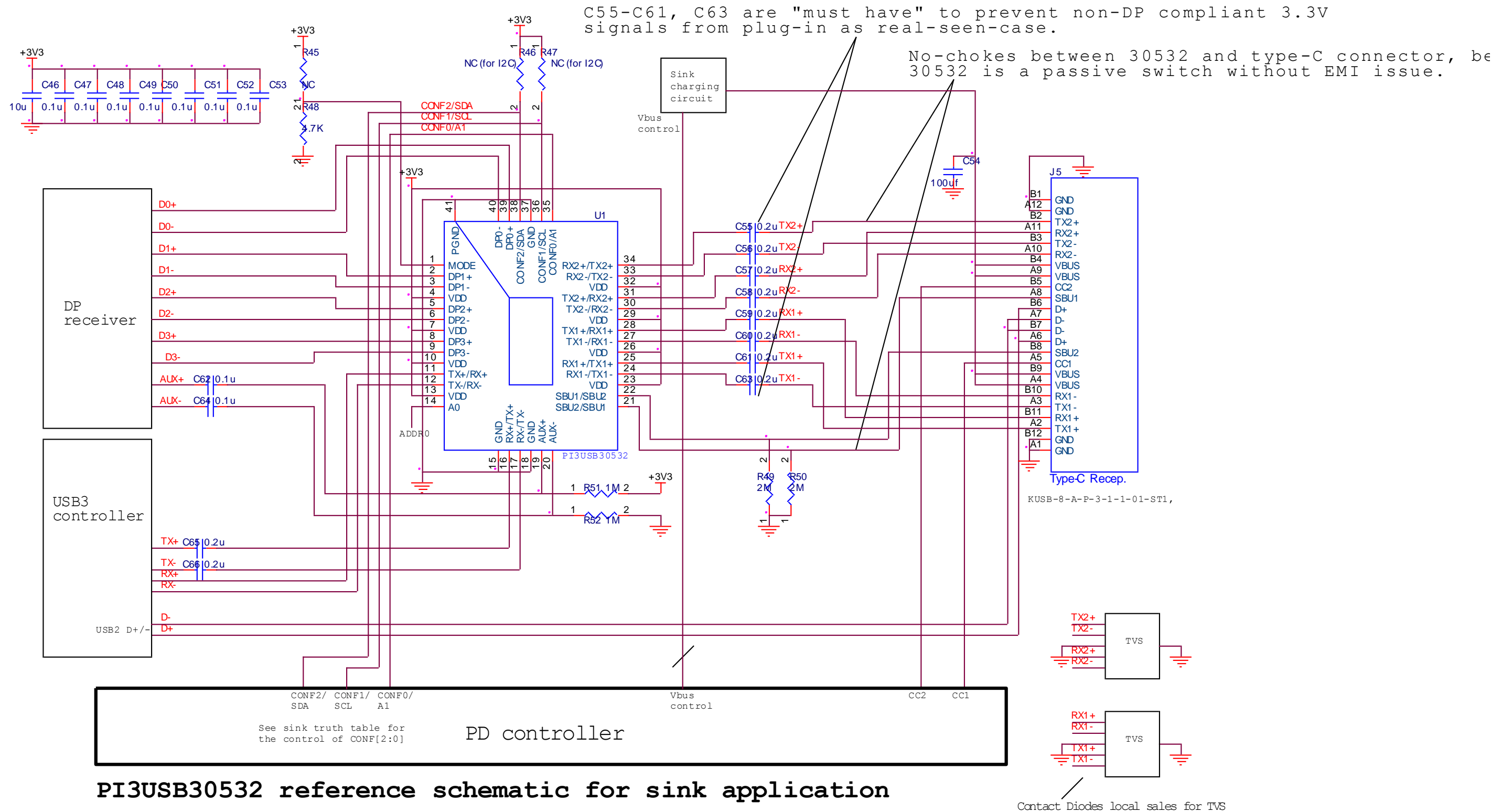
## 10 Appendix: application Reference Schematics

C76-C83 are "must have" to prevent non-DP compliant 3.3V signals from plug-in as real-seen-case.

No-chokes between 30532 and type-C connector, because 30532 is a passive switch without EMI issue.



PI3USB30532 DFP-source reference schematic for type-C PD/DP/ALT application

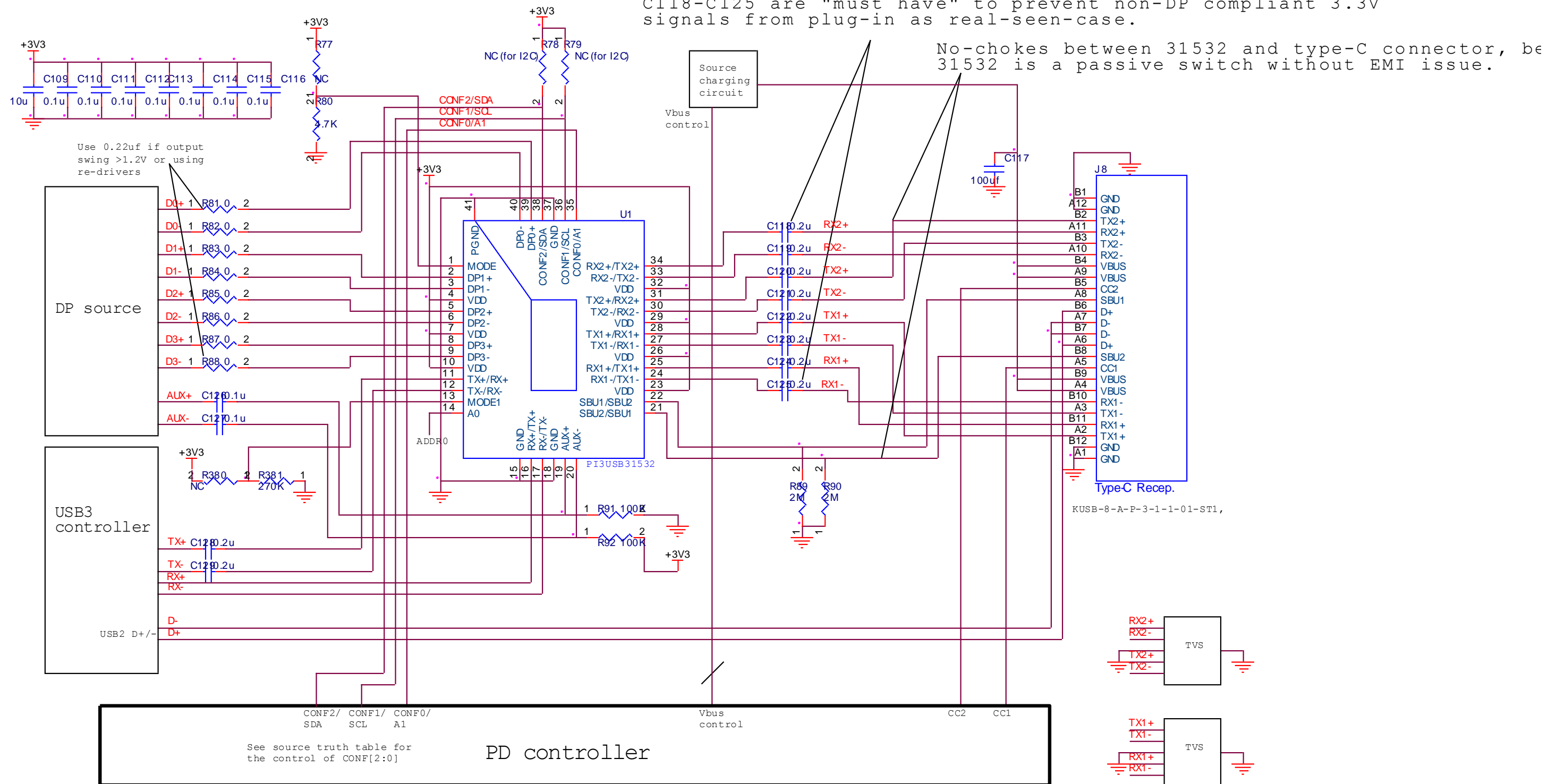


PI3USB30532 UFP-sink reference schematic for type-C PD/DP/ALT application



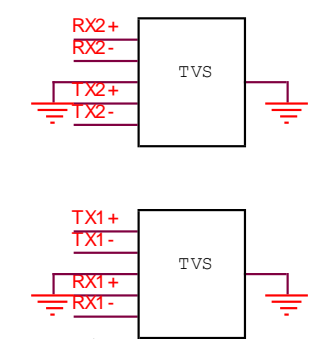
C118-C125 are "must have" to prevent non-DP compliant 3.3V signals from plug-in as real-seen-case.

No-chokes between 31532 and type-C connector, because 31532 is a passive switch without EMI issue.



## PI3USB31532 reference schematic for source application

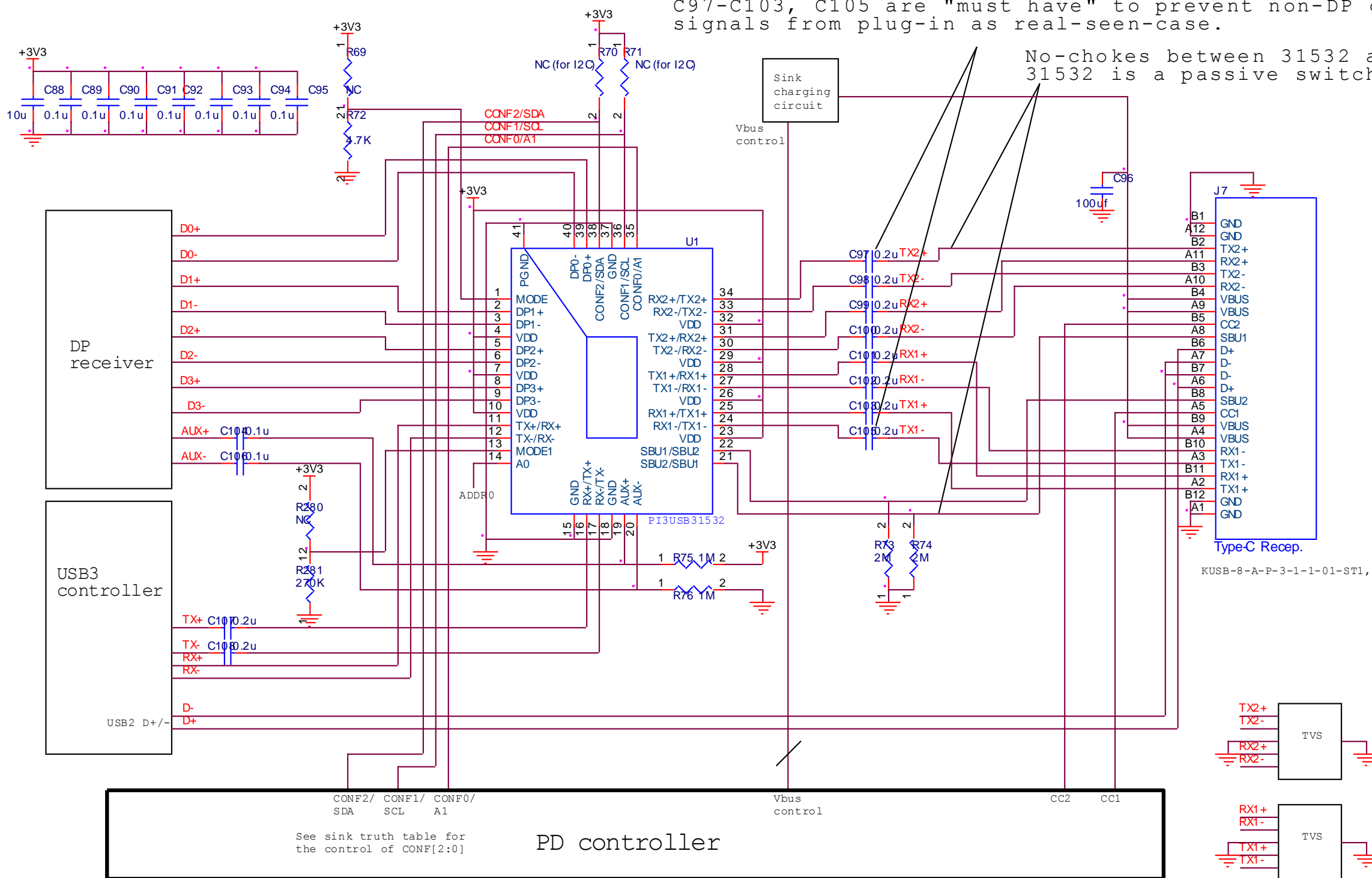
PI3USB31532 DFP-source reference schematic for type-C PD/DP/ALT application



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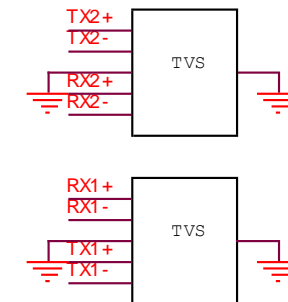
C97-C103, C105 are "must have" to prevent non-DP compliant 3.3V signals from plug-in as real-seen-case.

No-chokes between 31532 and type-C connector, because 31532 is a passive switch without EMI issue.



## PI3USB31532 reference schematic for sink application

PI3USB31532 UFP-sink reference schematic for type-C PD/DP/ALT application



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