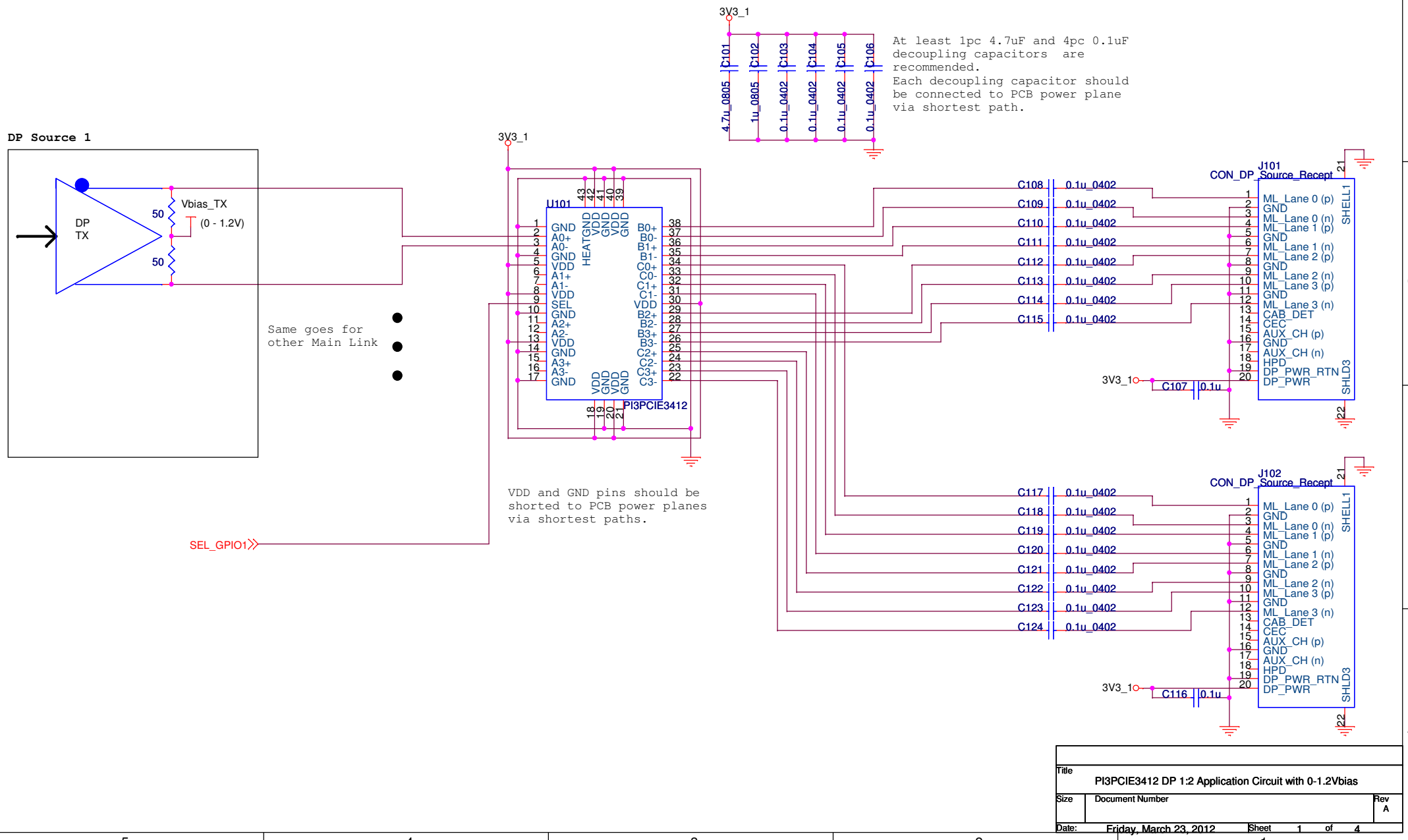
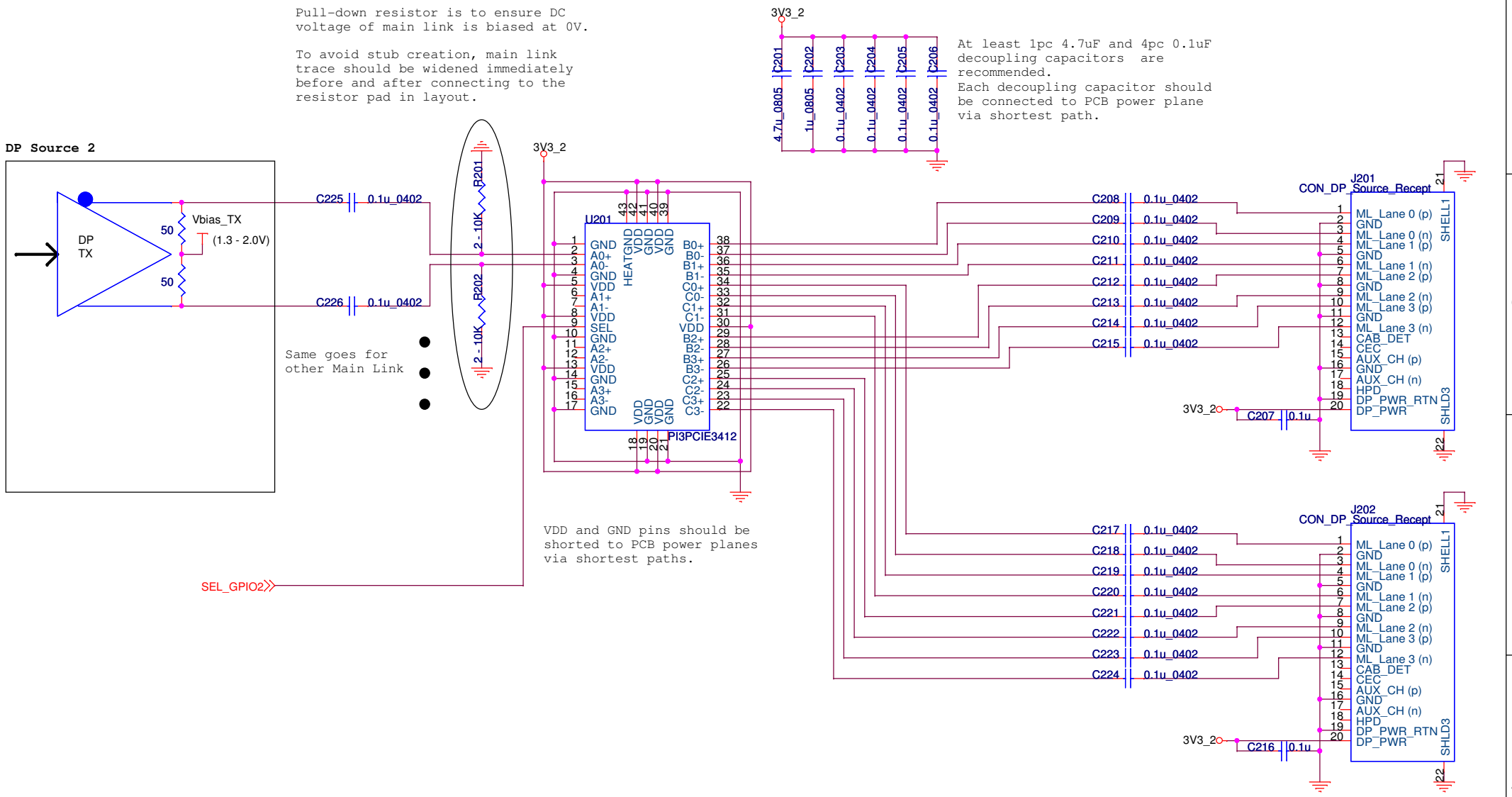
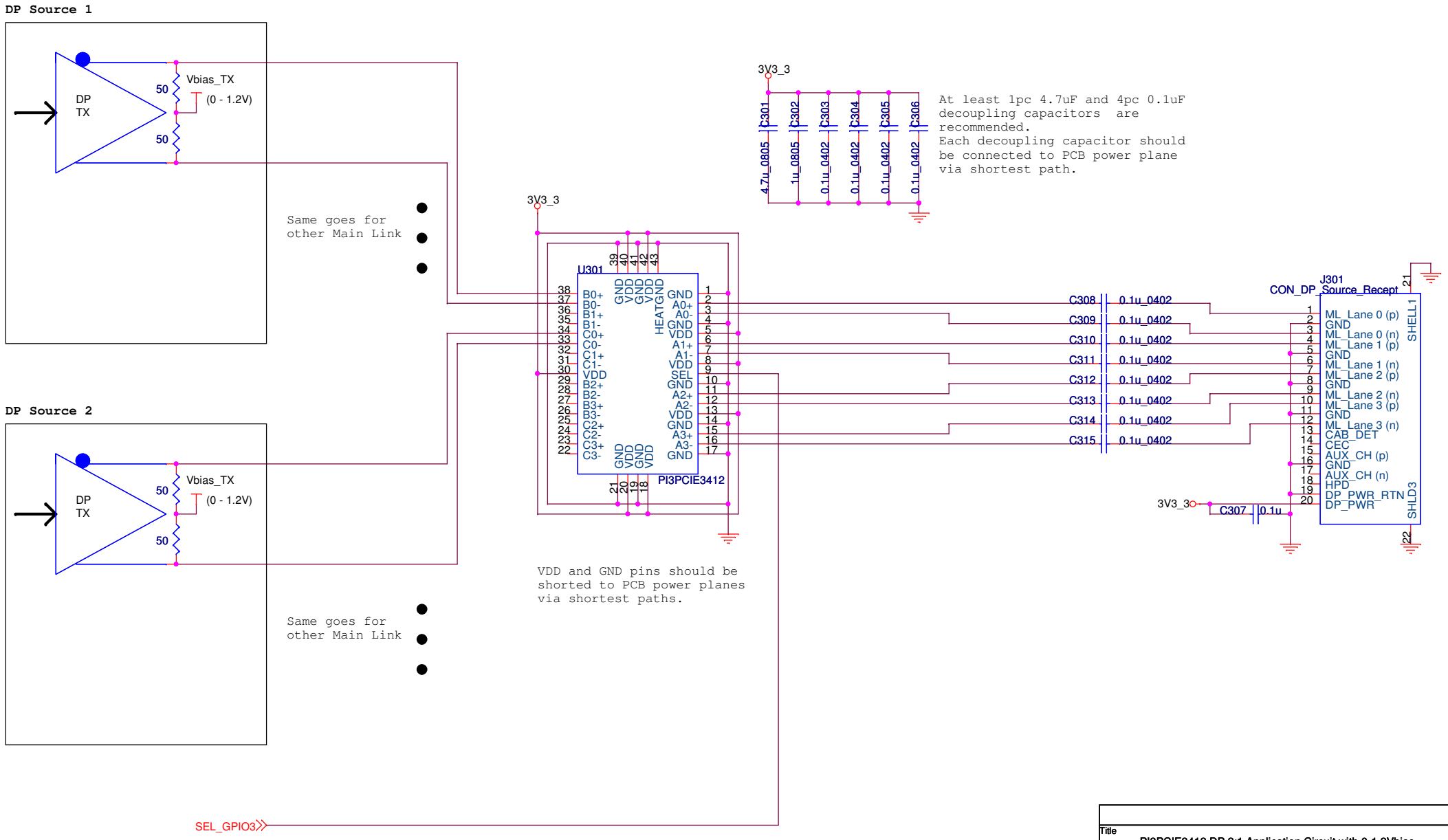


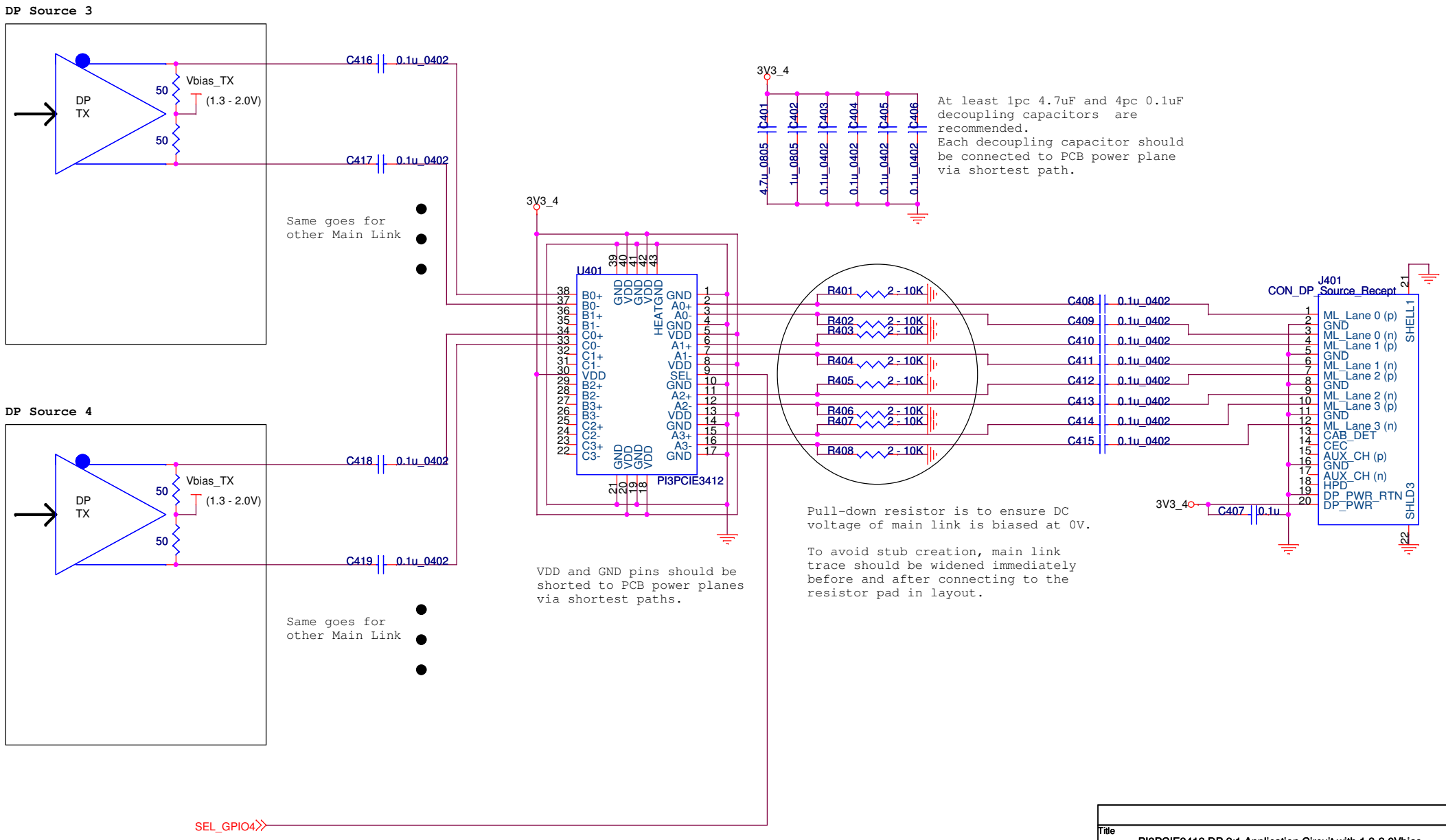
Title	PI3PCIE3412 DP 1:2 Application Circuit with 0-1.2Vbias	
Size	Document Number	Rev A
Date: Friday, March 23, 2012	Sheet 1 of 4	



Title	PI3PCIE3412 DP 1:2 Application Circuit with 1.3-2.0Vbias	
Size	Document Number	Rev A
Date: Wednesday, March 21, 2012	Sheet 2 of 4	



Title	PI3PCIE3412 DP 2:1 Application Circuit with 0-1.2Vbias	
Size	Document Number	Rev A
Date: Wednesday, March 21, 2012	Sheet 3 of 4	


DP Source 3
DP
TX
Vbias_TX
(1.3 - 2.0V)
50
50
C416 0.1u_0402
C417 0.1u_0402
Same goes for
other Main Link
DP Source 4
C418 0.1u_0402
C419 0.1u_0402
Same goes for
other Main Link
SEL_GPIO4
3V3_4
U401
PI3PCIE3412
VDD and GND pins should be
shorted to PCB power planes
via shortest paths.
C401 4.7u_0805
C402 1u_0805
C403 0.1u_0402
C404 0.1u_0402
C405 0.1u_0402
C406 0.1u_0402
At least 1pc 4.7uF and 4pc 0.1uF
decoupling capacitors are
recommended.
Each decoupling capacitor should
be connected to PCB power plane
via shortest path.
R401 2 - 10K
R402 2 - 10K
R403 2 - 10K
R404 2 - 10K
R405 2 - 10K
R406 2 - 10K
R407 2 - 10K
R408 2 - 10K
Pull-down resistor is to ensure DC
voltage of main link is biased at 0V.
To avoid stub creation, main link
trace should be widened immediately
before and after connecting to the
resistor pad in layout.
C408 0.1u_0402
C409 0.1u_0402
C410 0.1u_0402
C411 0.1u_0402
C412 0.1u_0402
C413 0.1u_0402
C414 0.1u_0402
C415 0.1u_0402
J401
CON_DP_Source_Recept
ML_Lane 0 (p)
GND
ML_Lane 0 (n)
ML_Lane 1 (p)
GND
ML_Lane 1 (n)
ML_Lane 2 (p)
GND
ML_Lane 2 (n)
ML_Lane 3 (p)
GND
ML_Lane 3 (n)
CAB_DET
CEC
AUX_CH (p)
GND
AUX_CH (n)
HPD
DP_PWR_RTN
DP_PWR
SHELL1
SHLD3
3V3_4
C407 0.1u
Title
PI3PCIE3412 DP 2:1 Application Circuit with 1.3-2.0Vbias
Size
Document Number
Rev
A
Date: Wednesday, March 21, 2012
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