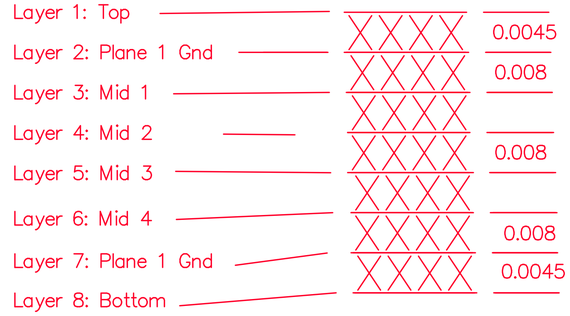
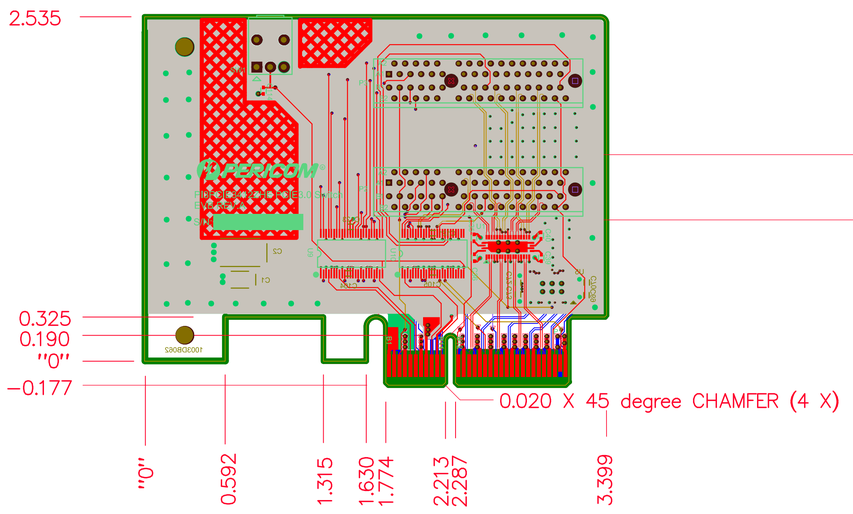
LAYER STACK-UP:

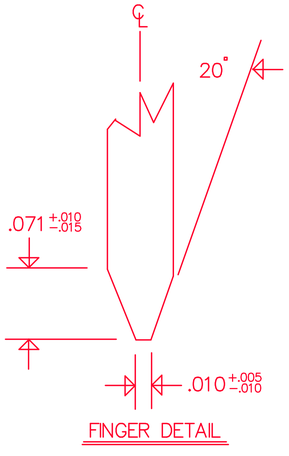


	Trace/Gap/Trace Design (Finished)	Diff IMPEDANCE REQUIRED/CAL	
Layer 1: Top	6.5/7/6.5 or 6/6/6	85	7.5 SE 43
Layer 2: Plane 1 Gnd			
Layer 3: Mid 1	6.5/9/6.5 or 6/7/6	85	7.5 SE 43
Layer 4: Mid 2			
Layer 5: Mid 3			
Layer 6: Mid 4	6.5/9/6.5 or 6/7/6	85	7.5 SE 43
Layer 7: Plane 1 Gnd			
Layer 8: Bottom	6.5/7/6.5 or 6/6/6	85	7.5 SE 43

Notes: Copper thickness .5oz all layers, external finished to 1.0 oz
Total requested thickness = 0.062"

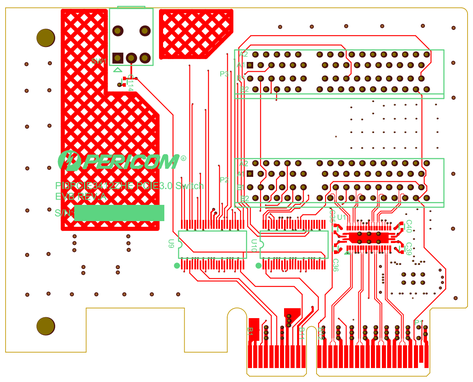
1. Material : EPOXY GLASS, NEMA GRADE FR-4 (SHALL MEET UL94V-0) COPPER CLAD 1OZ./SQ.FT. INNER AND OUTER LAYERS. TOTAL THICKNESS .057/.067.
2. CIRCUITRY AND PLATED THRU HOLES SHALL BE ELECTROPLATED COPPER .001 TO .002 THICK. PLATING IN HOLES .001 MIN. THICK.
3. SOLDERMASK BOTH SODES WITH HYSOL SR-1000 (LIQUID PHOTO-IMAGEABLE[LPI] FOR SURFACE MOUNT) OR EQUIVALENT. HOLES, EDGE CONNECTOR AND TERMINAL AREAS SHALL BE FREE OF SOLDERMASK.
4. ALL UNDIMENSIONED HOLES SHALL BE LOCATED WITHIN .003 IN. TRUE POSITION DIAMETER.
5. SILKSCREEN LEGEND OVER SOLDERMASK ON BOTH SIDES OF PCB USING WHITE EPOXY INK.
6. LAYER TO LAYER REGISTRATION TO BE WITHIN +/- .003.
7. LAYERS SHALL BE BONDED WITH GLASS CLOTH THERMOSETTING ADHESIVE SYSTEM COMPATIBLE WITH THE BASE MATERIAL.
8. FINISHED CONDUCTOR WIDTH SHALL BE +/- 10% OF THE ORIGINAL FILM MASTER.
9. 12 MICRO INCHES OF FULL BODY GOLD ON BOTH SIDES
10. IMPEDANCE CONTROL OF ALL TRACES ON TOP AND BOTTOM LAYER FOR 50 OHMS



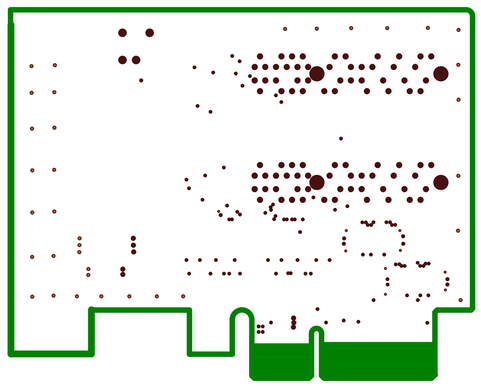


FINGER DETAIL

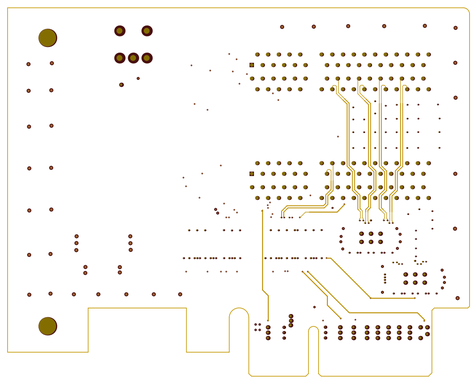
Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE	[illegible] LAYER		
SHEET NUMBER	1	OF	10



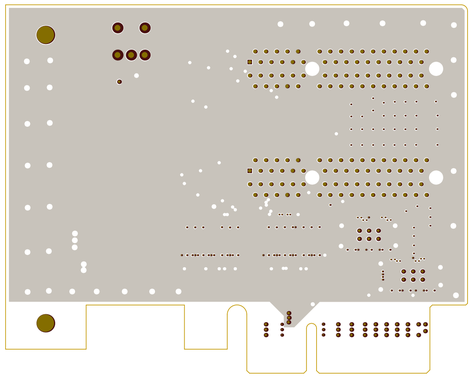
Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE	TOP SILKSCREEN LAYER		
SHEET NUMBER	$ OF 10		



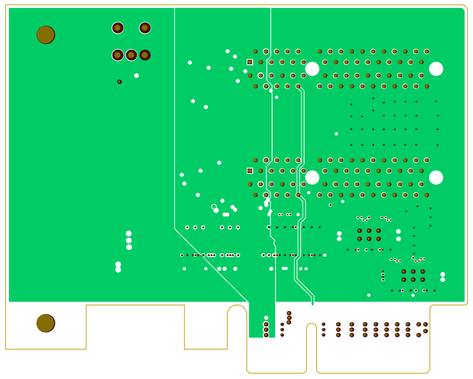
Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE	POWER PLANE LAYER		
SHEET NUMBER	2 OF 10		



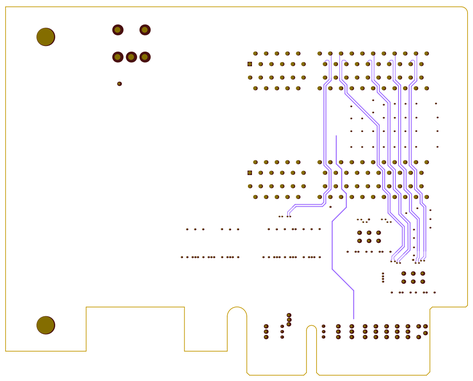
Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE			
SHEET NUMBER	OF 10		



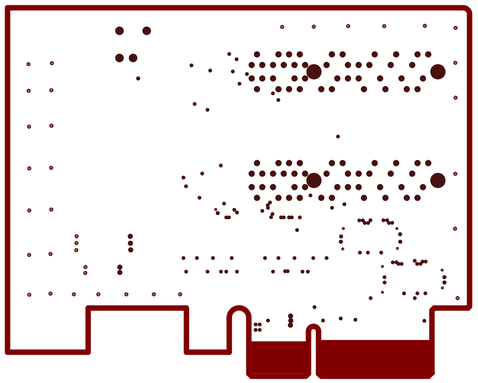
Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE			
SHEET NUMBER	OF 10		



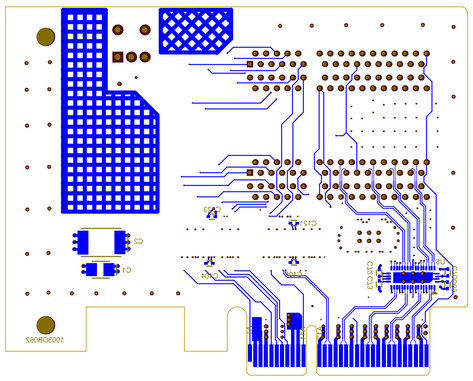
Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE			
SHEET NUMBER	OF 10		



Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE			
SHEET NUMBER	OF 10		



Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE	GND PLANE LAYER		
SHEET NUMBER	3 OF 10		



Pericom			
PCB NAME	PI3PCIE3412ZHE PCIE3.0 SW EVB		REV.A
DATE	1/26/2010	Drawn by	Haojie Ci
TITLE	BOTTOM SILKSCREEN LAYER		
SHEET NUMBER	6	OF	10