Verification of PI3HDX412BD IBIS model

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Data: 01/23/2014

1. Introduction:

To verify the correlation between the ibis model and hspice model, we need to do some simulations:

a) For pin SEL_OUT (model OUTPUT1):
   i. Add 150ohm resistor to ground, input frequency = 100meg;
   ii. Add 150ohm resistor to VDD, input frequency = 100meg;

b) For pin EQ1_SDA_CTL (model IOopendrain):
   i. Add 500ohm resistor to VDD, input frequency = 200KHz;
   ii. Add 500ohm resistor to VDD, input frequency = 200megHz;

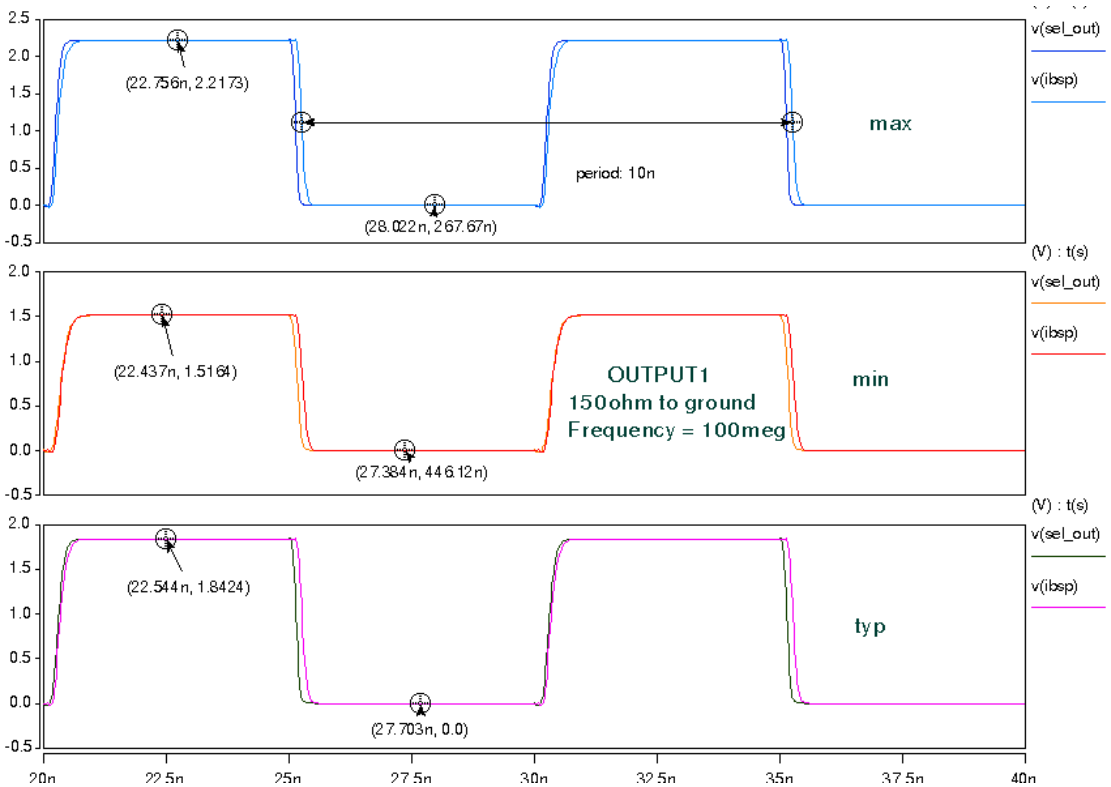
c) For pin D2P2 D2N2, etc (model OUTPUT_HS):
   i. Add 50ohm resistor to VDD, for open drain 0dB condition, input pulse 500megHz;
   ii. Add 50ohm resistor to VDD, for source termination 0dB, input pulse 500megHz;
   iii. Add 50ohm resistor to VDD, for open drain 0dB condition, input PRBS7 3.3Gbps;
   iv. Add 50ohm resistor to VDD, for source termination 0dB, input PRBS7 3.3Gbps;

2. Conclusion:

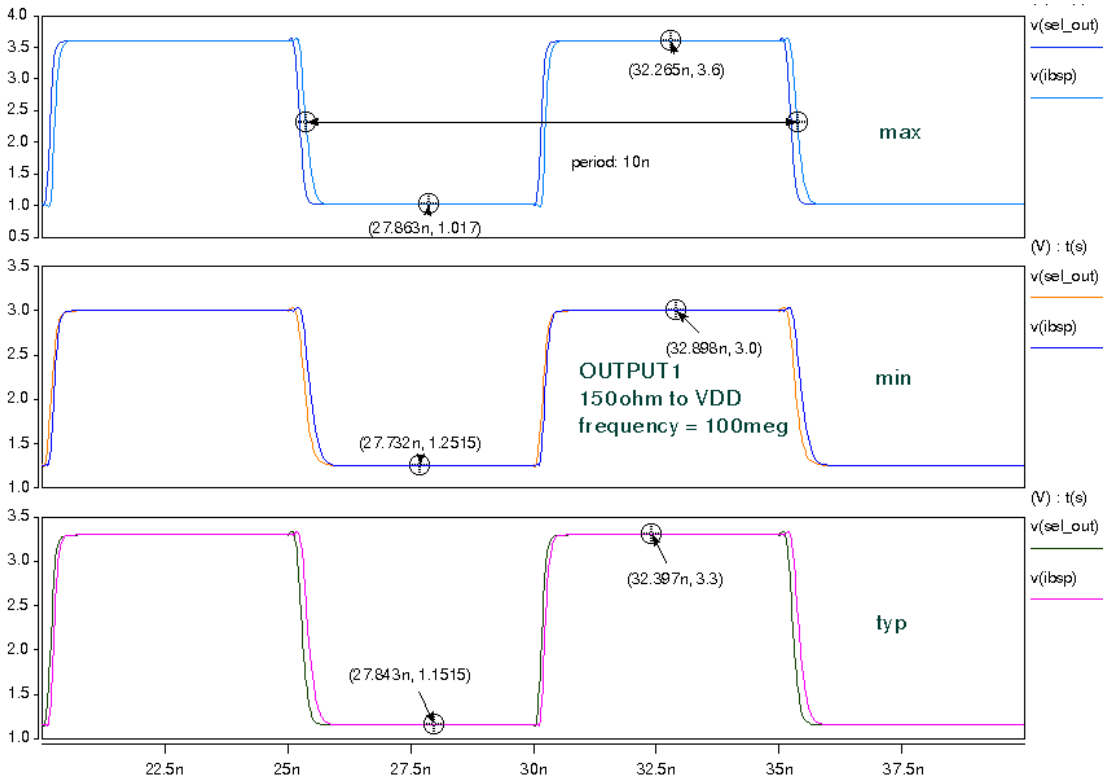
The simulated results show that the generated IBIS model can match well with the HSPICE model at different load conditions.

3. SEL_OUT (model OUTPUT1) simulation:

i. Add 150ohm resistor to ground, input frequency = 100meg:

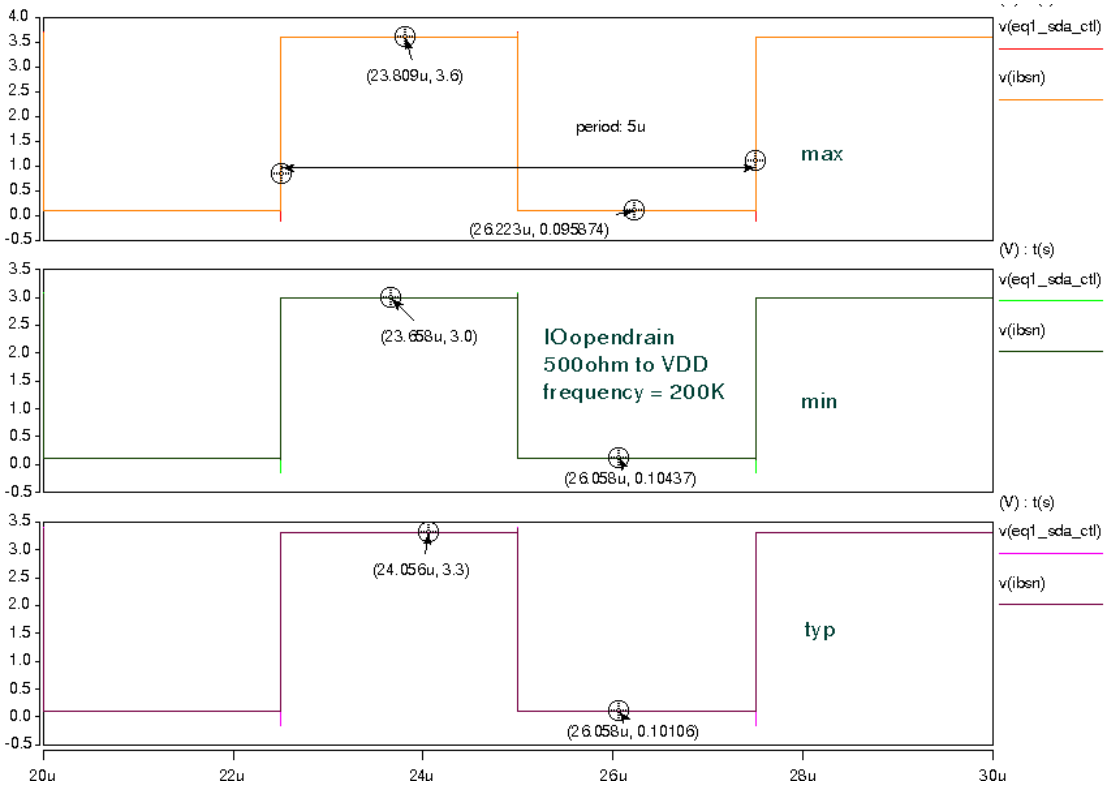


ii. Add 150ohm resistor to VDD, input frequency = 100meg;

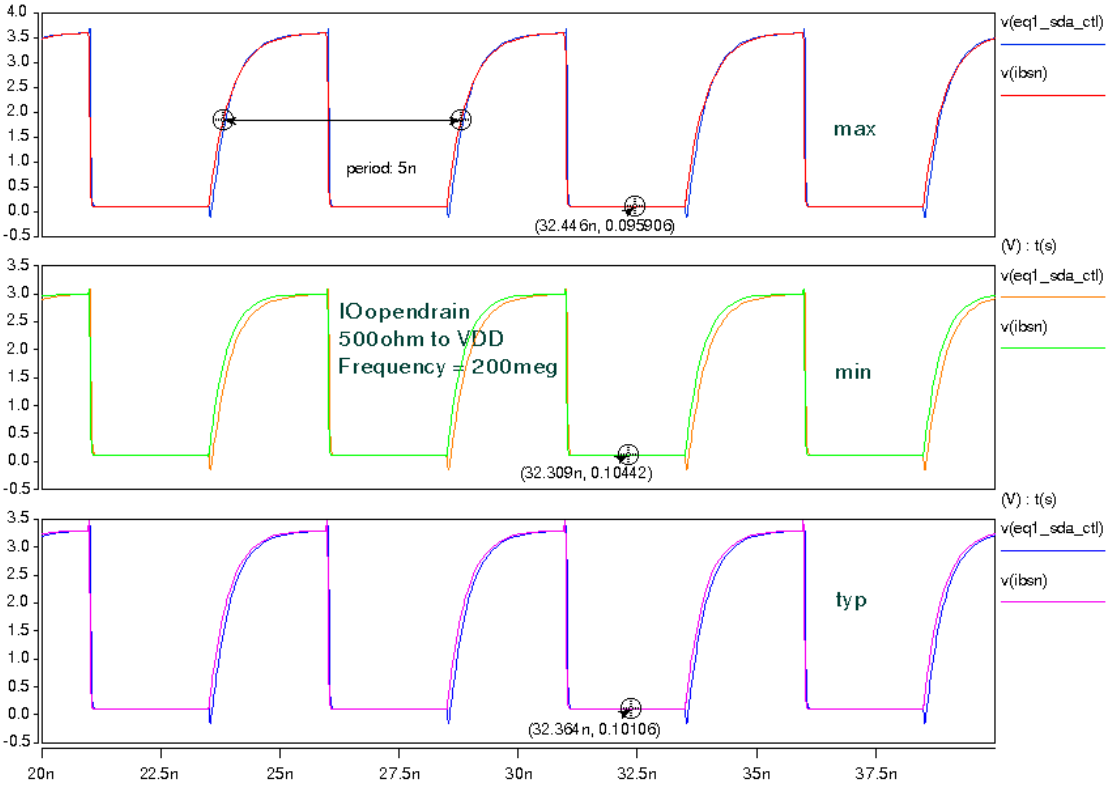


4. EQ1_SDA_CTL (model IOopendrain) simulation:

i. Add 500ohm resistor to VDD, input frequency = 200 KHz;

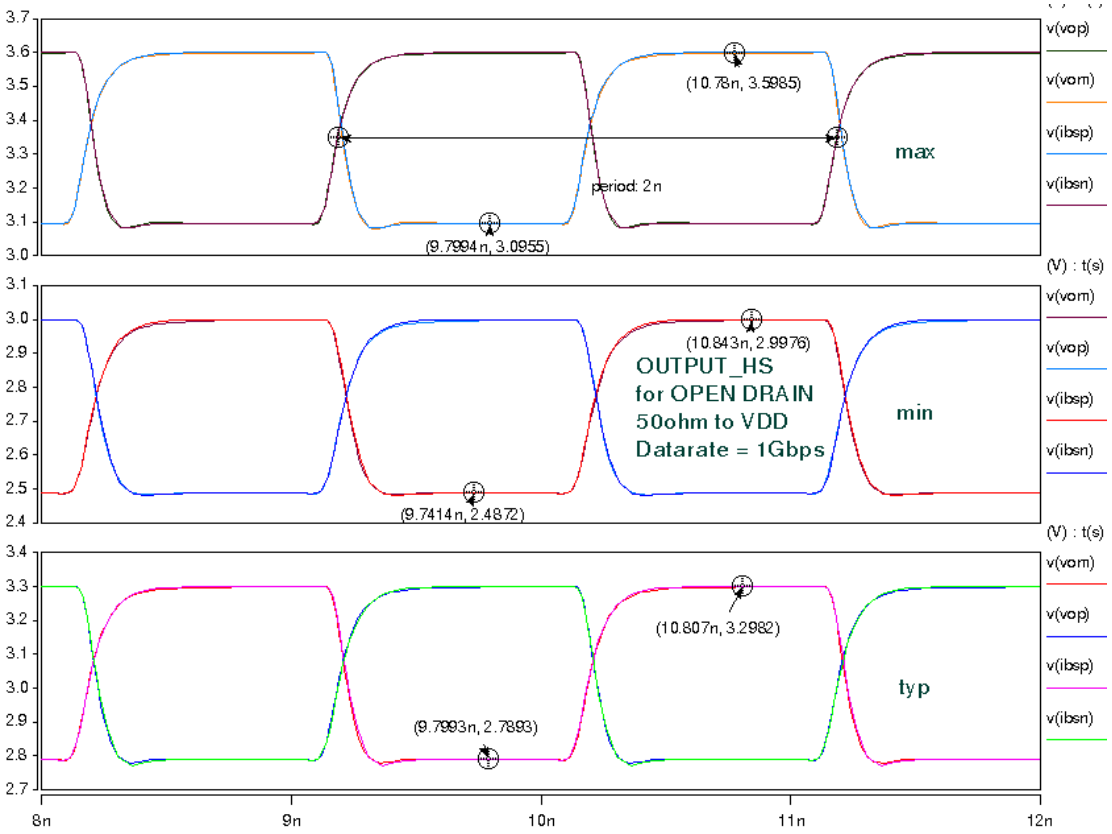


ii. Add 500ohm resistor to VDD, input frequency = 200megHz;

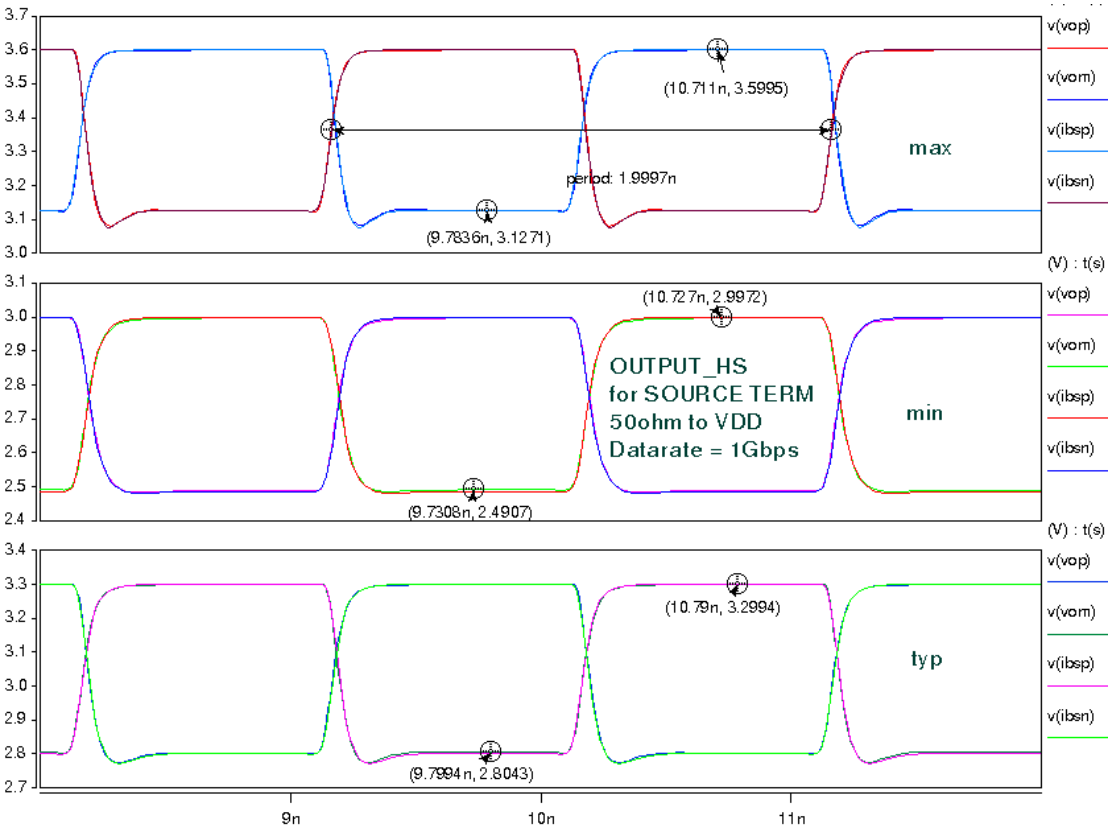


5. D2P2, D2N2,etc (model OUTPUT_HS) simulation:

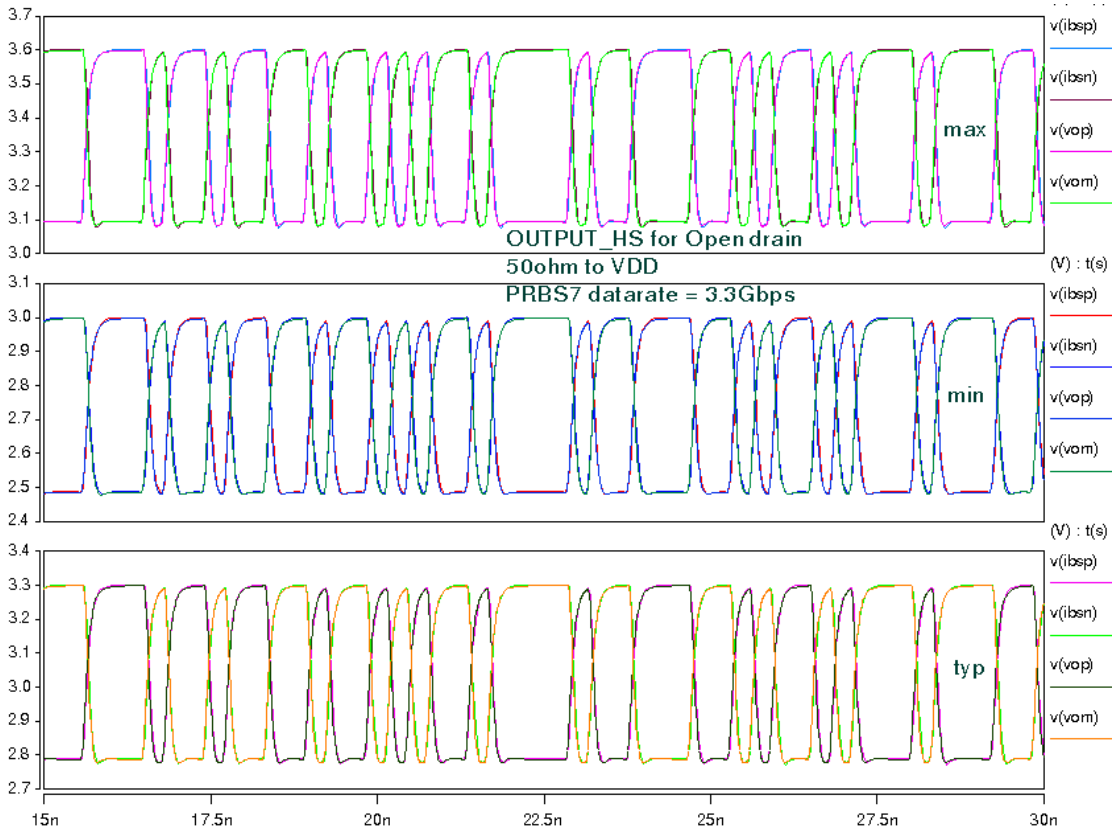
i. Add 50ohm resistor to VDD, for open drain 0dB condition, pulse frequency 500megHz;



ii. Add 50ohm resistor to VDD, for source termination 0dB, pulse frequency 500megHz;



iii. Add 50ohm resistor to VDD, for open drain 0dB condition, input PRBS7 3.3Gbps;



iv. Add 50ohm resistor to VDD, for source termination 0dB condition, PRBS7 3.3Gbps;