PERICOM Enabling Serial Connectivity

Application Note

PI3EQXxxxxx
Pericom ReDriver I2C Master Mode AppNote
Mar. 15, 2016

General Introduction
This document is mainly for Pericom ReDriver with I2C master mode feature. The user should follow it for system application with external EEPROM for Pericom ReDriver register data.

It supports Pericom Redrivers in list below.

- ✓ ***PI3EQX1204-C***
- ✓ ***PI3EQX12908A***
- ✓ ***PI3EQX8908A***
- ✓ ***PI3EQX8904***
- ✓ ***PI3EQX10908A***
- ✓ ***PI3EQX10964A***

Control pins for I2C master mode
All of these listed redrivers have the control pins below for I2C master mode and should be noted in system application.

- **ENI2C** pin, when it is HIZ or FLOAT, the redriver register setting will be configured from external EEPROM that means redriver as Master Mode.

ENI2C	I	I^2C Enable Pin. The pin is tied internally to $V_{DD}/2$. When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I^2C bus. When FLOAT, data is accesses from external EEPROM (Master Mode).

- **AD[3…0]** pins, they will decide I2C address byte.

AD[0:3]	I	I^2C programmable address bits. AD[0:2] have internal 100K-Ohm pull-up. AD[3] is internally tied to $V_{DD}/2$.

- **I2C_RESET#** pin, it will reset register setting when it goes to low.

I2C_RESET#	I	Reset Pin for I^2C. When, reset the registers to default states.

- **All_DONE** pin, it will output valid register load complete status.

ALL_DONE	O	Valid Register Load Status Output. When LOW, the external EEPROM load has failed. When HIGH, the external EEPROM load is successful.

- **SCL/SDA** pins, they're I2C bus signal lines.

SCL	I/O	I^2C SCL clock input/output. This pin becomes clock output when loading from EEPROM. (ENI2C = FLOAT)
SDA	I/O	I^2C SDA data input/output.

ReDriver Register Data location in external EEPROM

When a system is designed for using the external EEPROM, the external EEPROM address byte must be 0xA0h and capable of 400 kHz operation at 3.3V supply. And the user needs to set the AD[3:0] inputs for I2C address byte. Table below is the relation of EEPROM data starting location vs ReDriver address.

ReDriver Address Pins	External EEPROM
AD3, AD2,AD1,AD0	Data Starting Location
0000	00h
0001	10h
0010	20h
0011	30h
0100	40h
0101	50h
0110	60h
0111	70h
1000	80h
1001	90h
1010	A0h
1011	B0h
1100	C0h
1101	D0h
1110	E0h
1111	F0h

Note: ReDriver address pins setting should be suitable for external EEPROM size. Maximum ReDrivers on I2C bus are sixteen.

Single Redriver Application at I2C master mode

Figure1 is single ReDriver application circuit sample only for control pins at I2C master mode.

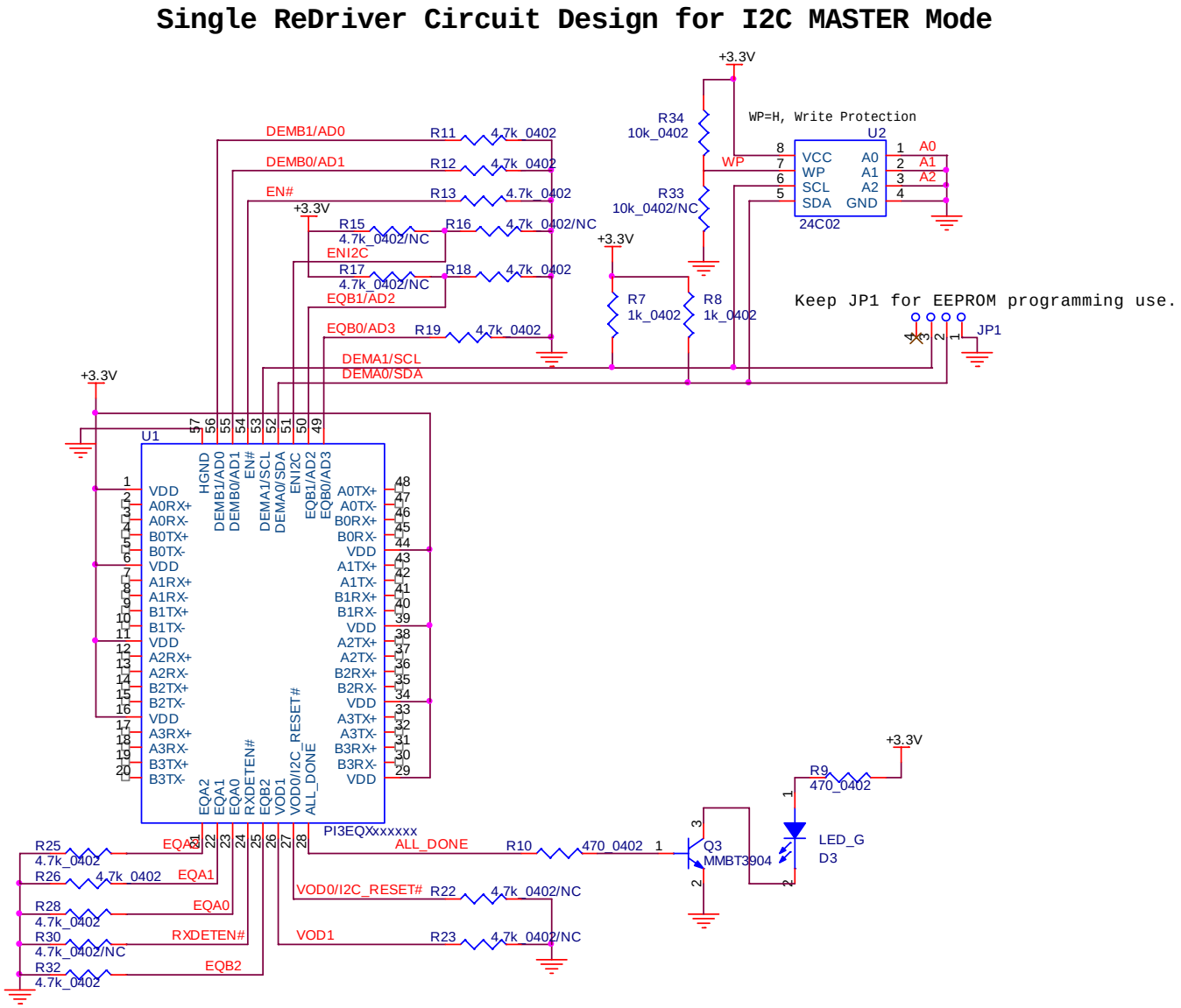

Figure1 Single ReDriver Application Circuit Sample

In this design sample, all the ReDriver address pins are pulled low, so the ReDriver register data will be loaded from 0x00h of external EEPROM.

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for ReDriver setting. RED **Bold** fonts are register data from Byte0 to Byte15 for ReDriver in first line for this single ReDriver application.

:1000**00**00**000000FF0000FFFFFFFFFF0000FF6201**77
:10001000000000000000000000000000000000E0
:10002000000000000000000000000000000000D0
:10003000000000000000000000000000000000C0
:10004000000000000000000000000000000000B0
:10005000000000000000000000000000000000A0

```
:10006000000000000000000000000000000000000090
:10007000000000000000000000000000000000000080
:10008000000000000000000000000000000000000070
:10009000000000000000000000000000000000000060
:1000A000000000000000000000000000000000000050
:1000B000000000000000000000000000000000000040
:1000C000000000000000000000000000000000000030
:1000D000000000000000000000000000000000000020
:1000E000000000000000000000000000000000000010
:1000F000000000000000000000000000000000000000
:00000001FF
```

Figure2 is the reading waveform on I2C bus when single ReDriver is working at I2C master mode based on the setting above.

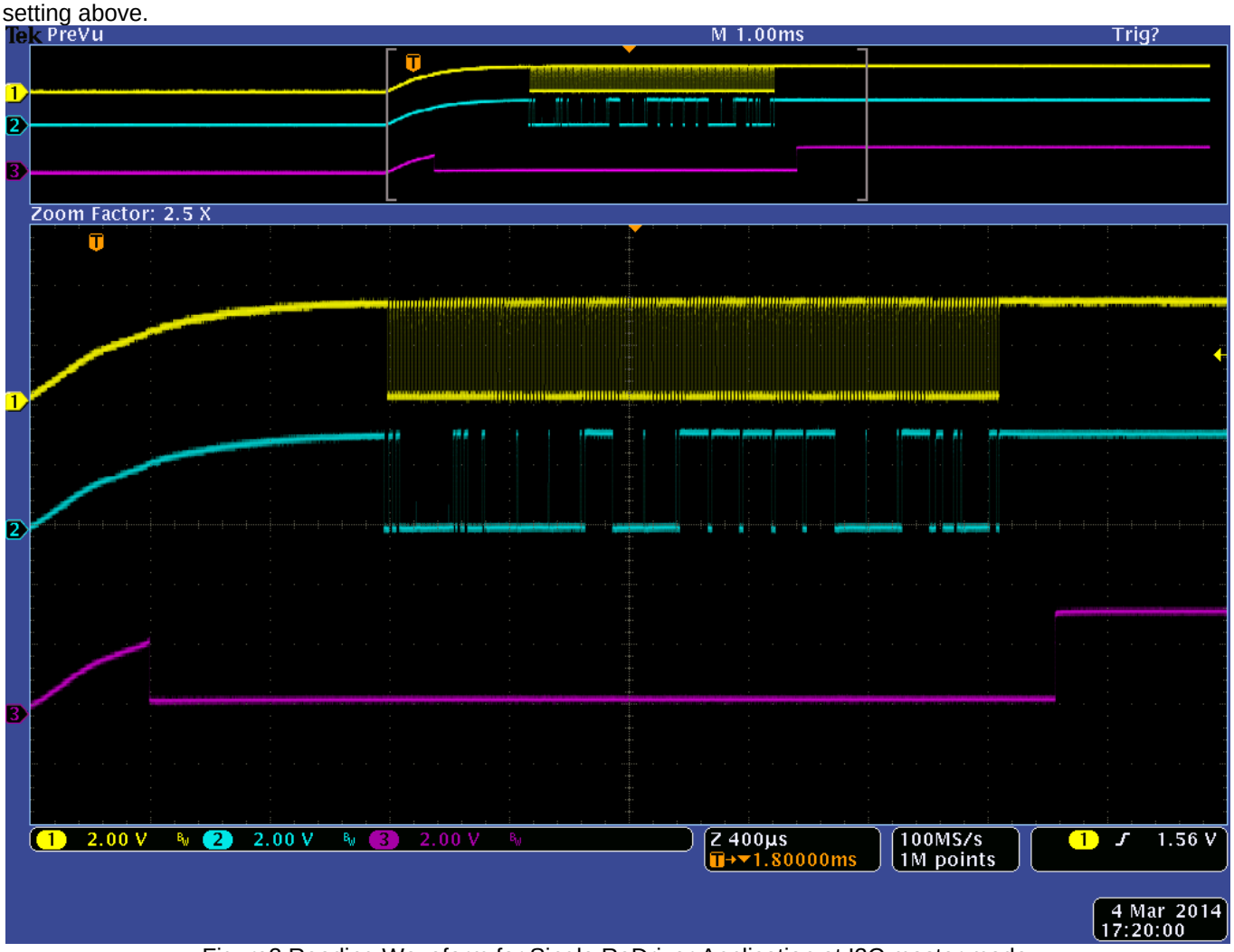

Figure2 Reading Waveform for Single ReDriver Application at I2C master mode

Multiple ReDrivers Application at I2C master mode

When multiple ReDrivers are connected to I2C bus for master application, the user should follow the guidelines below to configure the devices.

- Example below is for 4 devices. The first device in the sequence must be address 0x00h; subsequent devices must follow the address order listed below.
  - U1: AD[3:0] = 0000 = 0x00h,
  - U2: AD[3:0] = 0001 = 0x10h,
  - U3: AD[3:0] = 0010 = 0x20h,
  - U4: AD[3:0] = 0011 = 0x30h
- Use a pull-up resistor on SDA and SCL; value = **1Kohms**
- Daisy-chain I2C_RESET# and ALL_DONE from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie ALL_DONE of U1 to I2C_RESET# of U2
  2. Tie ALL_DONE of U2 to I2C_RESET# of U3
  3. Tie ALL_DONE of U3 to I2C_RESET# of U4
  4. Optional: Tie ALL_DONE output of U4 to a LED to show the devices has been loaded successfully.

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for 4pcs ReDrivers device. RED Bold fonts are register setting from Byte0 to Byte15 for each device in each line.

:1000**00**00**000000FF0000FFFFFFFFFF0000FF6201**94
:1000**10**00**000000FFFF0000FFFFFFFF0000FF6201**84
:1000**20**00**000000FFFFFF0000FFFFFF0000FF6201**74
:1000**30**00**000000FFFFFFFF0000FFFF0000FF6201**64
:10004000000000000000000000000000000000B0
:10005000000000000000000000000000000000A0
:1000600000000000000000000000000000000090
:1000700000000000000000000000000000000080
:1000800000000000000000000000000000000070
:1000900000000000000000000000000000000060
:1000A00000000000000000000000000000000050
:1000B00000000000000000000000000000000040
:1000C00000000000000000000000000000000030
:1000D00000000000000000000000000000000020
:1000E00000000000000000000000000000000010
:1000F00000000000000000000000000000000000
:00000001FF

Figure3 is multiple Redrivers application circuit sample only for control pins in I2C master mode.

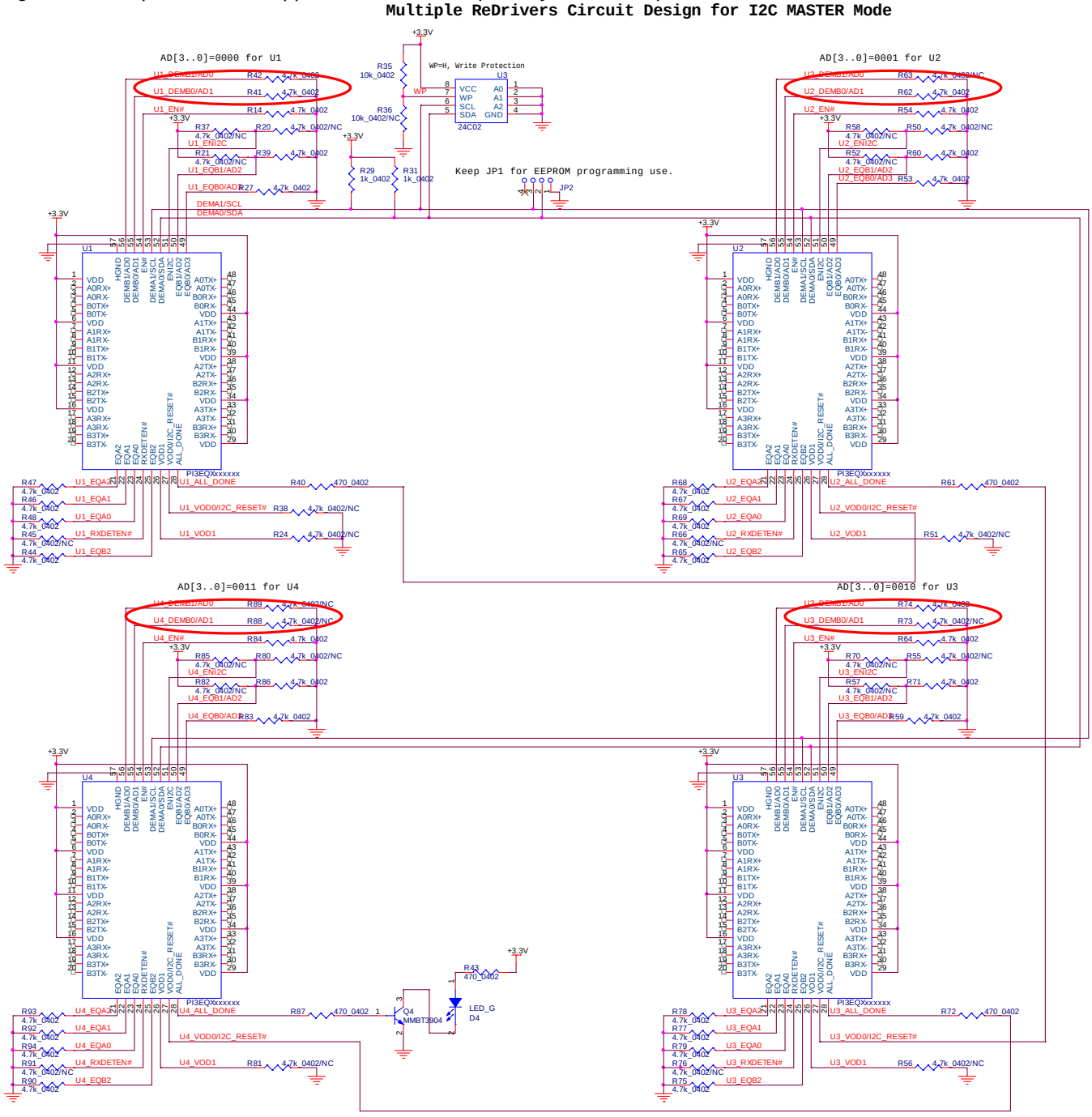

Figure3 Four ReDrivers Application Circuit Sample

Figure4 is the reading waveform on I2C bus when Multiple ReDrivers is working at I2C master mode based on the setting above.

Figure4 Reading Waveform for Multiple ReDriver Application at I2C master mode

Power –on Sequencing

Proper power-on sequencing should be taken care for I2C master reading. The customer system power-on sequence should make sure that the I2C reading action MUST complete before all of high speed protocol training link like PCIE or SATA/SAS.

Caution: If the reading action is delayed to process of high speed training link, the protocol connection may have the fail because the redriver setting is not ready.

History

Version 1.0	Original Version	Feb. 14, 2014
Version 1.1	Updated Version	Nov. 17, 2015
Version 1.2	Updated Version	Mar. 15, 2016