USB3.0 ReDriver PI3EQX7741AI\_PI3EQX7841 co-design and Application Note

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Rev B

**Introduction**

In Server/Workstation/PC/embedded application customer, the stability and performance quality margin will be the most important point to their product. Therefore Pericom provide the different USB3.0 redriver solution for different kind of application area to meet customer’s requirement. **Suggest to use PI3EQX7741AI / PI3EQX7841 co-design to optimize the compensation setting for performance and get better margin for system.**

* **(A) Example why use Pericom PI3EQX7741AI/PI3EQX7841 USB3.0 ReDriver in Server/Workstation Application (Include with USB3.0 MUX application)**
* **(B) Different EQ vs same insertion lose**
* **(C) Pericom PI3EQX7741AI/PI3EQX7841 USB3.0 redriver co-design guide**
* **(D) USB3.0 SuperSpeed USB Layout Guideline**

1. **Example why use Pericom PI3EQX7741AI/PI3EQX7841 USB3.0 ReDriver in Server/Workstation Application**
2. **For USB3.0 long distance(maximum 20db lose) design Vth function benefit of PI3EQX7741AI/PI3EQX7841**



**Figure 1 Vth function Block Diagram of PI3EQX7741AI/PI3EQX7841**

1. **PI3EQX7841 OS(output swing) set to 1200mV to get better performance margin**

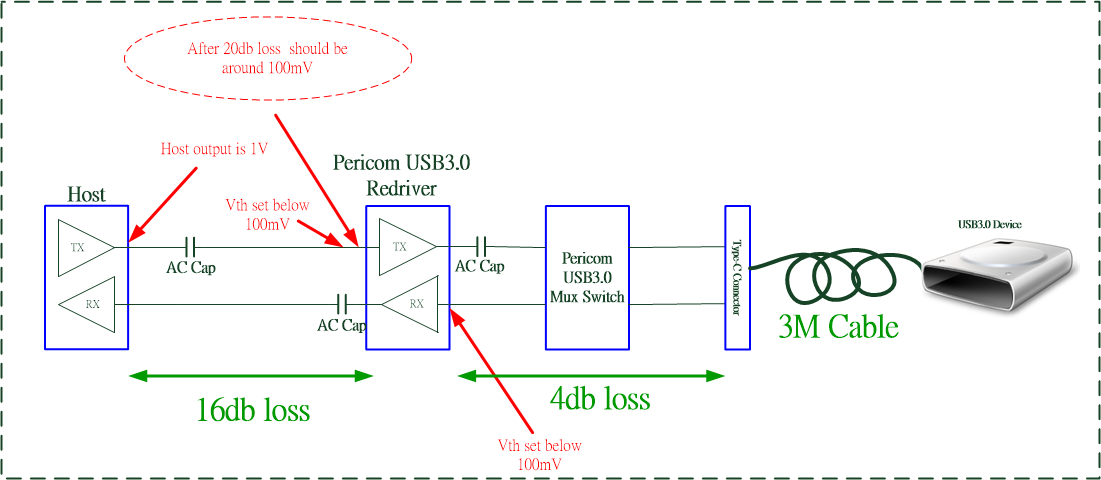


**Figure 2 Output Swing improve Block Diagram of PI3EQX7841**

1. **PI3EQX7741/PI3EQX7841 with USB3.0 MUX insertion loss limit and placement suggestion application**

Before Re-driver the maximum redriver insertion loss is about [16db@2.5GHZ](mailto:16db@2.5GHZ)

After Re-driver the maximum redriver insertion loss is about [4db@2.5GHZ](mailto:4db@2.5GHZ)



**Figure 3 USB3.0 Mux with Re-driver application Block Diagram of PI3EQX7841/PI3EQX7741**

1. **PI3EQX7841 can optimize EQ/DE/OS setting to meet customer’s loss compensation design**

|  |  |  |  |
| --- | --- | --- | --- |
| **Redriver Setting** | **Description** | **PI3EQX7741AI** | **PI3EQX7841** |
| **EQ\_A/B** | **Equalizer compensation** | **3-level (3/6/9 db)** | **3-level by H/W (3 / 8.3 /11.7 db)**  **16-level by I2C (0~15db)** |
| **DE\_A/B** | **De-emphasis compensation** | **3-level(0/-3.5/-6 db)** | **3-level by H/W (0/-3.5/-6 db)**  **4-level by I2C (0/-2/-3.5/-6 db)** |
| **OS\_A/B** | **Output Swing compensation** | **NA** | **3-level by H/W (900/1000/1200mV)**  **4-level by I2C (900/1000/1100/1200mV)** |

**Below table is the loss in any conditions to ref.**

|  |  |
| --- | --- |
| **PCB Conditions** | **Loss (db)** |
| **1 inch in FR4 trace** | **0.5 ~ 0.8 db (top side 7 mil is 0.5 db, internal 3.5 mil is 0.8db)** |
| **Via/AC cap** | **0.3 ~ 0.8 db (variation by via design)** |
| **Connector** | **1 ~ 2 db** |

**Measurement the relation of the loss and the 2.5GHz CP1 Vpp**

|  |  |
| --- | --- |
| **Channel loss after source** | **CP1 Vpp after the channel loss** |
| **0 db loss** | **1.0Vpp** |
| **6 db loss** | **0.5Vpp** |
| **12 db loss** | **0.25Vpp** |
| **18 db loss** | **0.125Vpp** |
| **20 db loss** | **0.1Vpp** |

**(B) Different EQ vs same insertion lose**

**Typical Eye Diagram of different EQ setting with the same input trace loss**

|  |  |  |
| --- | --- | --- |
| **RedRiver EQ and De-emphasis Setting** | **PCB Input trace loss** | **TX eye diagram Result** |
| **EQ=3db**  **DE=0db** | **10 db loss** |  |
| **EQ=6db**  **DE=0db** | **10 db loss** | Description: D:\13. Customer support\Korea\Samsung\Samsung_mobile_EQX501I\Samsung_501I FIBEQ=6_9_12\9db lose_eq6_em0\Plot.png |
| **EQ=9db**  **DE=0db** | **10 db loss** | Description: D:\13. Customer support\Korea\Samsung\Samsung_mobile_EQX501I\Samsung_501I FIBEQ=6_9_12\9db lose_eq9_em0\Plot.png |
| **EQ=12db**  **DE=0db** | **10 db loss** | Description: D:\13. Customer support\Korea\Samsung\Samsung_mobile_EQX501I\Samsung_501I FIBEQ=6_9_12\9db lose_eq12_em0\Plot.png |

**(C)Pericom PI3EQX7741AI/PI3EQX7841 USB3.0 redriver co-design guide**

PI3EQX7741AI/PI3EQX7841 is a dual channel/one port (both TX± and RX±). Each channel offers selectable equalization setting to compensate the different input trace loss. These two parts are pin compatible with each other and can be co-designed, customer can test PI3EQX7741AI first, if the performance is not good enough, can replace to PI3EQX7841 control by H/W or I2C to optimize EQ/DE/OS setting.

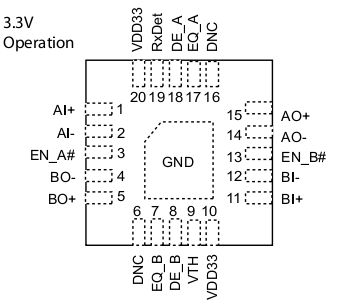
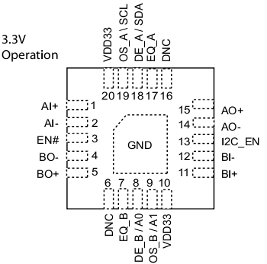
 

Figure 3-1 Pin Diagram of PI3EQX7741AI Figure 3-2 Pin Diagram of PI3EQX7841

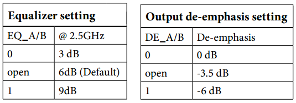


Figure 4-1 EQ/DE setting table of PI3EQX7741AI

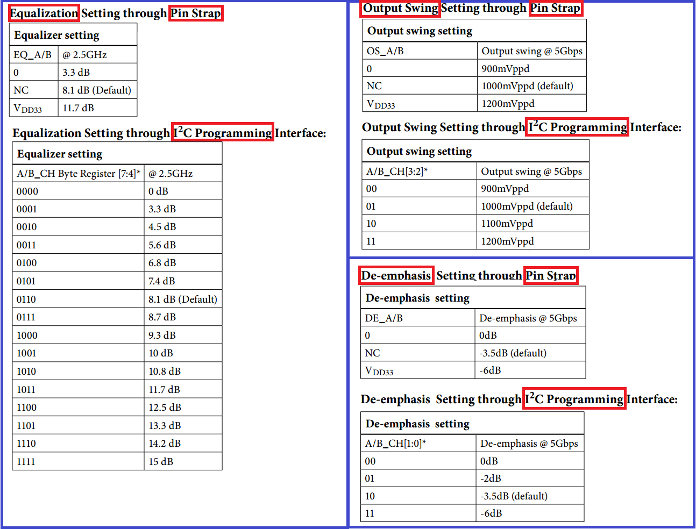


Figure 4-2 EQ/DE/OS setting table by H/W and I2C of PI3EQX7841

Reference Co-Design for PI3EQX7741AI/PI3EQX7841



**Figure 5:PI3EQX7741AI/PI3EQX7841 co-design circuit**





**Figure 6:PI3EQX7741AI Typ App circuit**



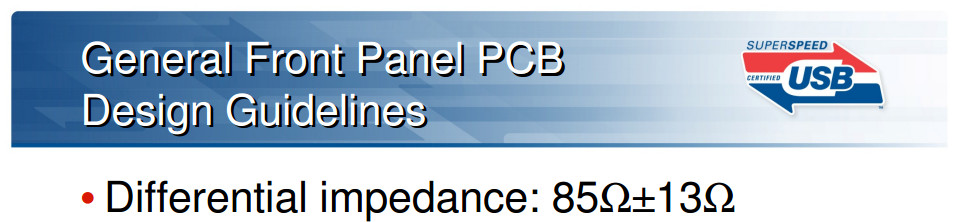


**Figure 7: PI3EQX7841 Typ App circuit**



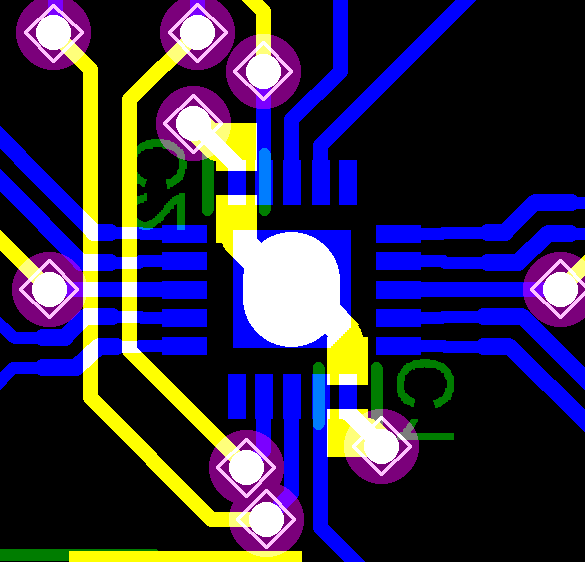
**(D)USB3.0 SuperSpeed USB Layout Guideline**

1. **PCB differential Impedance 72~98 ohm define in USB-IF**



1. **Decoupling capacitor of VDD**

It is recommended to put 0.1uF decoupling capacitor at each VDD pin of Pericom IC. Below is a layout reference of decoupling capacitor placement on a PI3EQX7741AI/PI3EQX7841 demo board. Two decoupling capacitors circled in pink below are located next to the four VDD pins (pins 10 and 20) of PI3EQX7741AI.



**Figure 8: Decoupling Capacitor Placement on PI3EQX7741ST**

1. **PCB layers**

It is recommended to use at least four layers PCB for SuperSpeed USB design. Every data signal trace should be routed entirely over the ground plane on an adjacent layer.

Recommendation on 4-layer PCB setting:

|  |  |  |
| --- | --- | --- |
| **Layer** | **Setting 1** | **Setting 2** |
| Top | Data signal, Clock | Power, Control Signal |
| 2nd | GND | Power, GND |
| 3rd | Power, GND | GND |
| Bottom | Power, Control signal | Data signal, Clock |