PI3EQX6801ZDE
PI3EQX6801 SATA ReDriver Application Note
Nov. 3, 2011

Contents

General Introduction
PI3EQX6801 SATA ReDriver™ are developed to redrive one full lane of SAS/SATA up to 6Gbps signal, they have continuous step output swing/pre-emphasis adjustment and excellent performance.

Packaging: 20-contact TQFN (4x4mm)

Main Application:
- ✓ ***Server***
- ✓ ***Desktop***
- ✓ ***Storage/Workstation***

Figure1 is typical application samples.

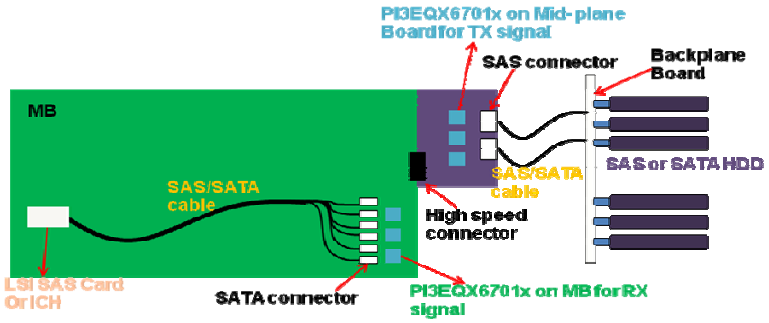


Figure1a Typical Application Sample1

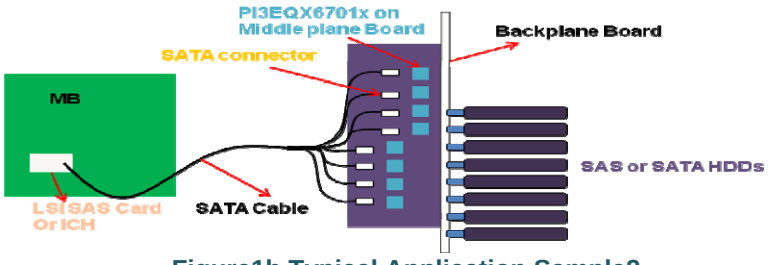


Figure1b Typical Application Sample2

How to Use Control Pins for Various Application

PI3EQX6801 has control pins such as EN, OOB, TDet_EN# AB/BB, and A_EQ/B_EQ. Table1 is the setting selection for various applications.

Table1 is selection table for various applications.

Pins	Function Description	Setting Selection
A_EN# B_EN#	Channel Enable Function w/ internal 200k pull-down resistor	High: Power-down mode Low: Normal Operation (default)
DNC	Do NOT connect Only for 3.3Vapplication	For 3.3V application, it must be not connected. For 1.5V application, it must be connected to 1.5V.
A_EM B_EM	Output Emphasis Adjustment	They allow analog resistive adjustment by the resistor to connect to GND. (Note, recommend to use under 4.0dB Pre-emphasis)
A_OS B_OS	Output Swing Adjustment	They allow analog resistive adjustment by the resistor to connect to GND. (Note, recommend to use 600mV for SATA application, 1000mV for SAS application)
A_EQ B_EQ	Input Equalizer Adjustment Tri-level control	A_EQ/B_EQ | 3GHz | Various Applications 0 | 8 dB | for 12~24 inch input trace $V_{DD}/2$ | 4 dB (Default) | for less than 12 inch input trace 1 | 16 dB | for 18~30 inch input trace

PI3EQX6801 can work at 1.5V or 3.3V power supply. Table2 is power consumption as reference.

Table2 Power consumption at 1.5V and 3.3V power

Power Supply	Power consumption (typical, mW)			
	Active (at 600mV Swing, 0db pre-emphasis)	Slumber mode	HDD unplug	Standby (Max.)
1.5V Power	162	22.5	1.5	0.089
3.3V Power	356	50	3.3	1.82

Note that PI3EQX6801 has the same pin-out definitions compared to PI3EQX6701x.
1, if the customer currently uses PI3EQX6701x under +3.3V power application and wants to upgrade to PI3EQX6801, some changes MUST be taken care.

- ✓ **Resistor values on x_EM and x_OS pins should be changed based on Page3 of PI3EQX6801 datasheet.**
- ✓ **The control on x_EQ pins of PI3EQX6801 is tri-level selection, Low/Open/High.**

		PI3EQX6701C	PI3EQX6701D	PI3EQX6701E	PI3EQX6801
A_EQ	Low	1dB	7dB	1dB	A_EQ/B_EQ | 3GHz 0 (Low) | 8 dB $V_{DD}/2$ (Open) | 4 dB (Default) 1 (High) | 16 dB
	High	4dB	11dB	4dB	
B_EQ	Low	1dB	7dB	7dB	
	High	4dB	11dB	11dB	

2, if the customer currently uses PI3EQX6701x under +1.2V power application, PI3EQX6801 is not recommended because it needs +1.5V power.

External Components Requirement

PI3EQX6801ZDE requires AC coupling capacitors for all redriver outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

- **Layout Considerations for Differential Pairs**
  - ✓ The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
  - ✓ Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
  - ✓ Target differential Zo of 100ohm ±20%
  - ✓ More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
  - ✓ It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
  - ✓ The use of vias should be avoided if possible, if vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
  - ✓ Route the differential signals away from other signals and noise sources on the printed circuit board
- **PCB Layout Trace Routings**

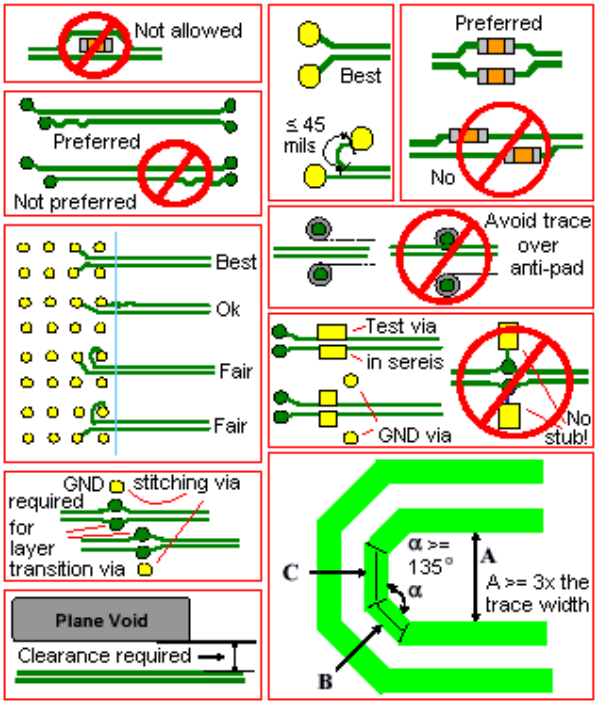


Figure2 Layout Sample for Trace Routings

Power-Supply bypass

More careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply; there are some approaches as recommendation.

- ✓ The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- ✓ The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.

- ✓ Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PI3EQX6801ZDE. Smaller body size capacitors can help facilitate proper component placement. The distance of capacitors to IC body should be <100mil.
- ✓ One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommened for all devices. Always apply GND and VDD before applying signals., especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization Setting

■ **Various Input Trace and Eye Test with different EQ setting**

Figure3 is PI3EQX6801ZDE test setup for different EQ setting, R is PI3EQX6801ZDE.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB

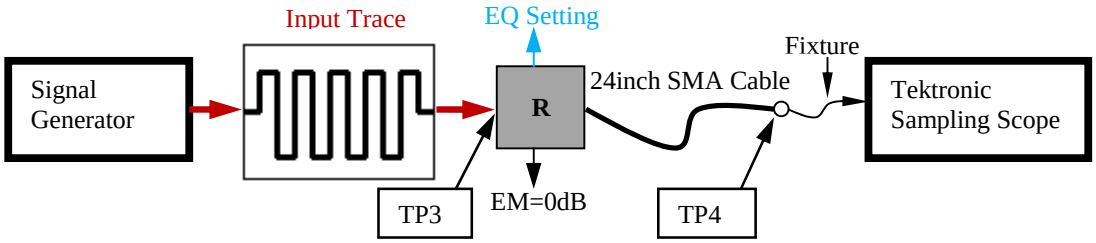


Figure3 PI3EQX6801ZDE test setup for different EQ setting

Table3 Eye Diagram vs. Input FR4 trace and EQ setting at 6Gb/s

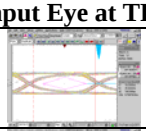
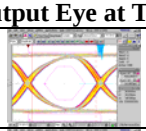
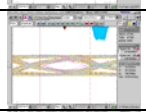
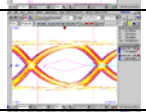
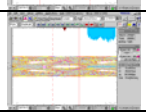
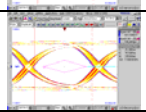
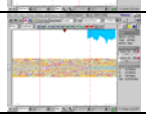
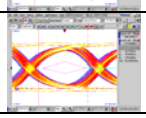
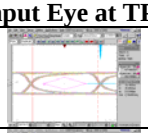
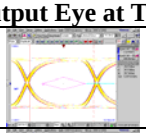
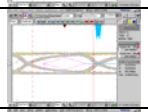
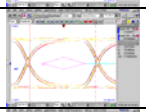
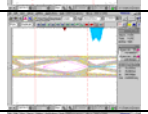
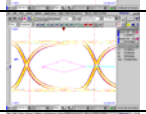
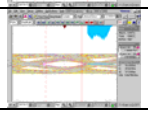
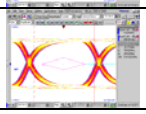
Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-2dB loss at 3GHz)	4dB (A_EQ or B_EQ =Open)		
18 inch FR4 Lab trace (-6dB loss at 3GHz)	8dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-10dB at 3GHz)	16dB (A_EQ or B_EQ =High)		
48 inch FR4 Lab trace (-16dB loss at 3GHz)	16dB (A_EQ or B_EQ =High)		

Table4 Eye Diagram vs. Input FR4 trace and EQ setting at 3Gb/s

Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	4dB (A_EQ or B_EQ =Open)		
18 inch FR4 Lab trace (-3dB loss at 1.5GHz)	8dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-5dB loss at 1.5GHz)	16dB (A_EQ or B_EQ =High)		
48 inch FR4 Lab trace (-9dB loss at 1.5GHz)	16dB (A_EQ or B_EQ =High)		

Swing Setting

Figure4 is PI3EQX6801ZDE test setup for different swing setting, R is PI3EQX6801ZDE.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

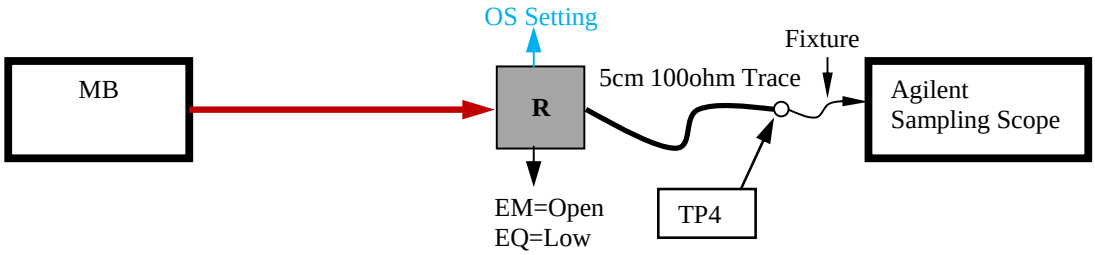
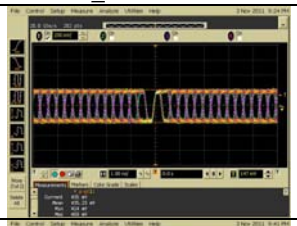
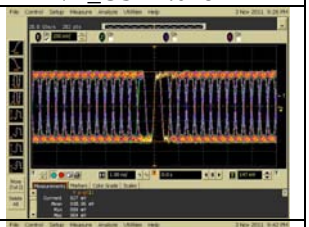
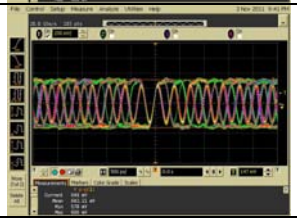
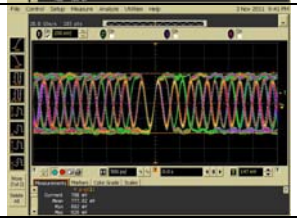


Figure4 PI3EQX6801ZDE test setup for different OS setting

Table5 Output Swing vs. OS setting at 3Gb/s and 6Gb/s for PI3EQX6801ZDE

	A/B_OS=**4.7kohm**	A/B_OS =**3.9kohm**	A/B_OS =**2.0kohm**
Output Swing at TP4 vs. OS setting at 3Gb/s			
Output Swing at TP4 vs. OS setting at 6Gb/s			

Pre-emphasis Setting

Figure5 is PI3EQX6801ZDE test setup for different pre-emphasis setting, R is PI3EQX6801ZDE.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

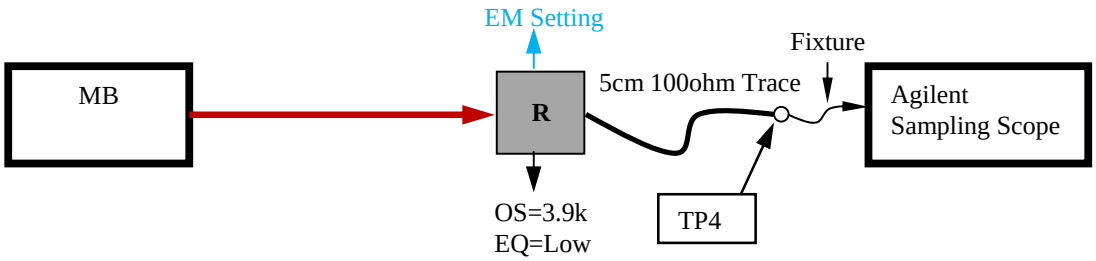
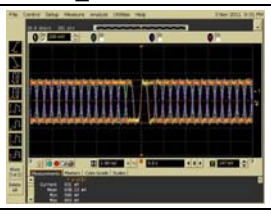
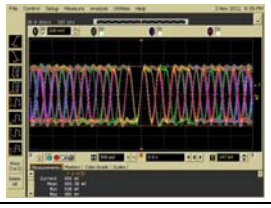
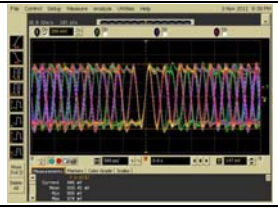


Figure5 PI3EQX6801ZDE test setup for different EM setting

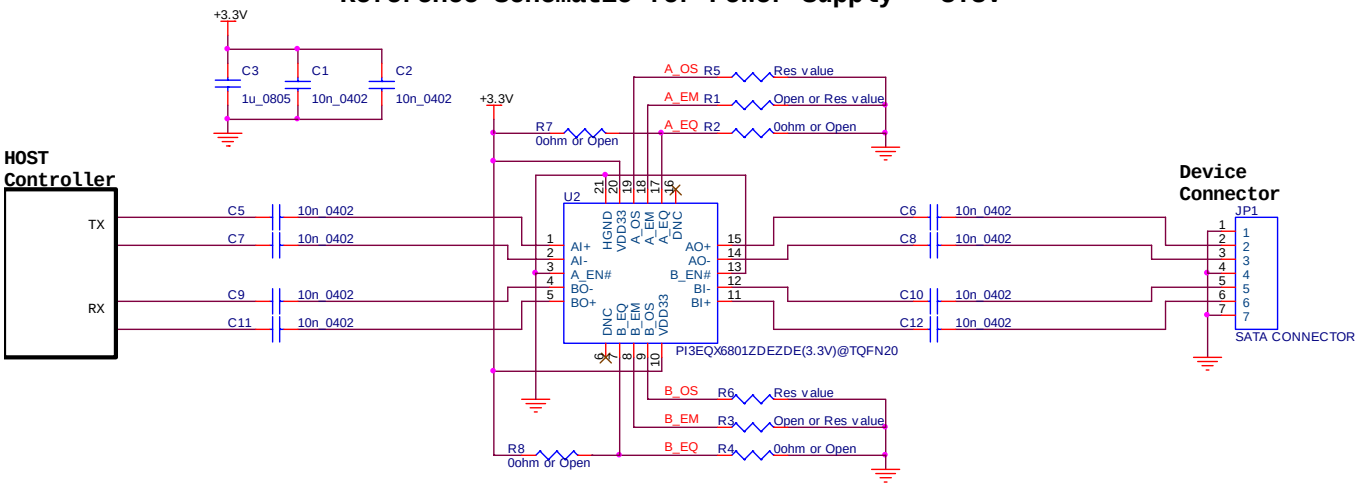
Table6 Pre-emphasis vs. EM setting at 3Gb/s and 6Gb/s for PI3EQX6801ZDE

	A/B_ EM=**15kohm**	A/B_ EM =**10kohm**	A/B_ EM =**5.6kohm**
Output Pre-emphasis at TP4 vs. EM setting at 3Gb/s			
Output Pre-emphasis at TP4 vs. EM setting at 6Gb/s			

Typical Application Circuit

Figure6 shows typical application circuit of PI3EQX6801ZDE.

Reference Schematic for Power Supply = 3.3V

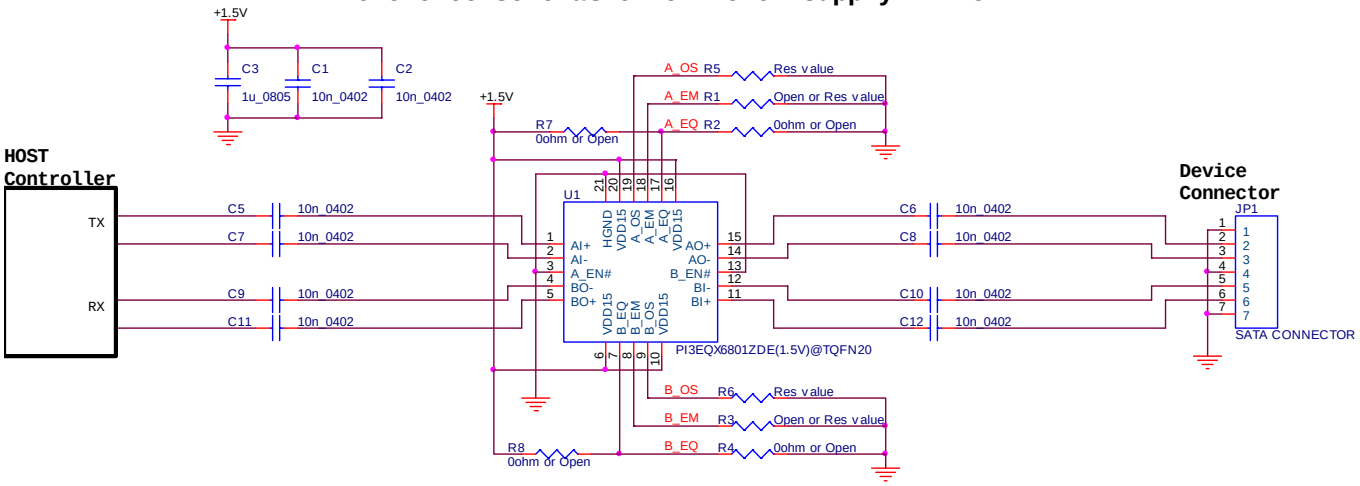


PIN CONFIGURATION for CONTROL

PIN NAME	PIN FUNCTION DESCRIPTION	Control Configuration
A_EN# B_EN#	With Internal 200k-ohm pull-down resistor Low: Normal Operation High: Power Down Mode	For real application, they could be OPEN.
A_EQ B_EQ	Input Equalization Tri-level Input	Equalization is controled by PIN7&PIN17 Input Equalization for Channel A&B Input Equalization@3.0Gb/s 0 — 8dB(A&B-CH) 1 — 16dB(A&B-CH) Vdd/2 — 4dB(A&B-CH)
A_EM B_EM	Output Emphasis Adjustment it is analog resistive adjustment. please refer to the next row table	Emphasis is controlled by PIN4&13, PIN5&12 and PIN6&11 of SW1 for Channel A, PIN4&13, PIN5&12 and PIN6&11 of SW2 for Channel B, Pre-emphasis for Channel A&B PIN4&13 is Open — 0dB PIN4&13 is short(14k RES) — +2.0dB PIN5&12 is short(10k RES) — +3.0dB PIN6&11 is short(6k RES) — +4.0dB
A_OS B_OS	Output Swing Adjustment it is analog resistive adjustment. please refer to the next row table	Swing is controlled by PIN1&16, PIN2&15 and PIN3&14 of SW1 for Channel A, PIN1&16, PIN2&15 and PIN3&14 of SW2 for Channel B, Swing Output for Channel A&B (mV, Vtx-diff-p at 6.0Gb/s) PIN1&16 is short(5k RES) — 660 PIN2&15 is short(4k RES) — 820 PIN3&14 is short(2k RES) — 1200
PIN6&16 PIN10&20	Voltage PIN	PI3EQX6801ZDE(3.3V)@TQFN20: PIN10&20=VDD33 (3.3V), PIN6&16=DNC

Figure6a Typical Application Circuit of PI3EQX6801ZDE at Power=3.3V

Reference Schematic for Power Supply = 1.5V



PIN CONFIGURATION for CONTROL

PIN NAME	PIN FUNCTION DESCRIPTION	Control Configuration
A_EN# B_EN#	With Internal 200k-ohm pull-down resistor Low: Normal Operation High: Power Down Mode	For real application, they could be OPEN.
A_EQ B_EQ	Input Equalization Tri-level Input	Equalization is controled by PIN7&PIN17 0 — 8dB(A&B-CH) 1 — 16dB(A&B-CH) Vdd/2 — 4dB(A&B-CH) (Input Equalization for Channel A&B / Input Equalization@3.0Gb/s)
A_EM B_EM	Output Emphasis Adjustment it is analog resistive adjustment. please refer to the next row table	Emphasis is controlled by PIN4&13, PIN5&12 and PIN6&11 of SW1 for Channel A, PIN4&13, PIN5&12 and PIN6&11 of SW2 for Channel B, PIN4&13 is Open — 0dB PIN4&13 is short(14k RES) — +2.0dB PIN5&12 is short(10k RES) — +3.0dB PIN6&11 is short(6k RES) — +4.0dB (Pre-emphasis for Channel A&B)
A_OS B_OS	Output Swing Adjustment it is analog resistive adjustment. please refer to the next row table	Swing is controlled by PIN1&16, PIN2&15 and PIN3&14 of SW1 for Channel A, PIN1&16, PIN2&15 and PIN3&14 of SW2 for Channel B, PIN1&16 is short(5k RES) — 660 PIN2&15 is short(4k RES) — 820 PIN3&14 is short(2k RES) — 1200 (Swing Output for Channel A&B (mV, Vtx-diff-p at 6.0Gb/s))
PIN6&16 PIN10&20	Voltage PIN	PI3EQX6801ZDE(1.5V)@TQFN20: PIN6&10&16&20=VDD15 (1.5V)

Figure6b Typical Application Circuit of PI3EQX6801ZDE at Power=1.2V

PCB Layout Sample

Figure7 shows typical layout routing of PI3EQX6801ZDE.

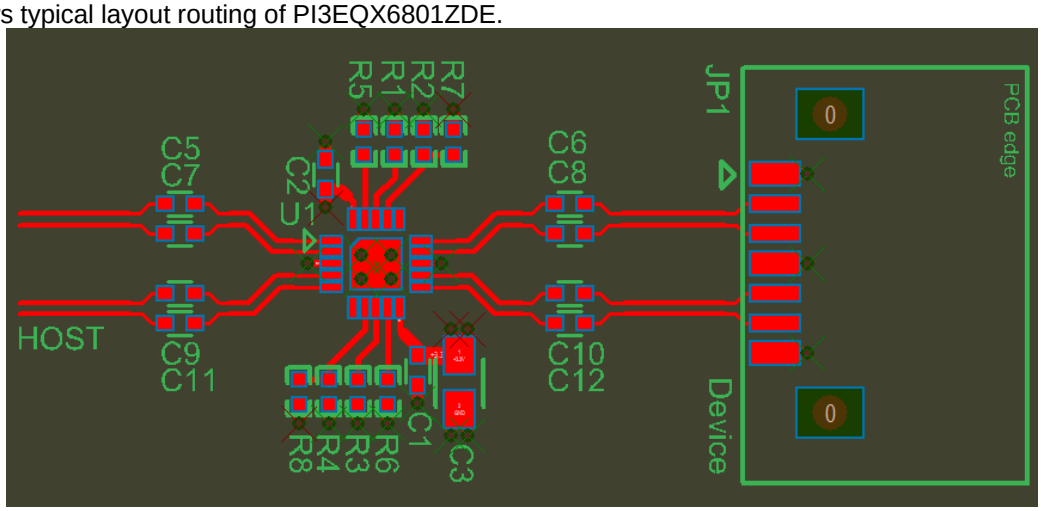


Figure7a Typical Layout Routing of PI3EQX6801ZDE at Power=3.3V

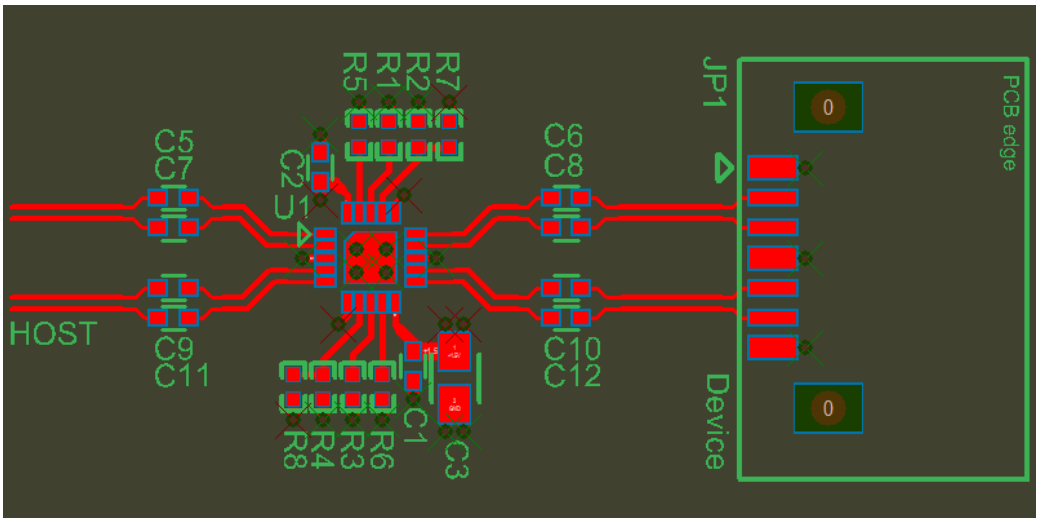


Figure7b Typical Layout Routing of PI3EQX6801ZDE at Power=1.5V

History

Version 1.0	Original Version	Nov. 3, 2011