USB3 applications using Pericom switches

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1.0 Introduction

USB3 ports become the majority ports nowadays. The demand of USB3 switches for sharing USB3 hosts is rapidly increasing. USB 3.1 at 10Gbps is on the horizon (PI3USB32212 ready).
SSIC (SuperSpeed inter chip) specification R1.01 (a supplement of USB3 specification, released in February 11 2013) utilizes the existing USB3 resources (software, hardware and protocol) to connect between chipset, SOC and modules within a system. SSIC applications also need USB3 switches since the point-to-point USB3 signals need a switch for multiple connections.

2.0 Why use Pericom USB3 switches

Pericom is the pioneer and industry leader in high speed differential switch solutions since the beginning of PCIe, HDMI, SATA, DisplayPort, Gigabit Ethernet, USB3, Thunderbolt…, in terms of:

- Innovation and patents
- First to the market (PI3USB32212 is ready for USB3 10Gbps)
- High volume shipment, market proof
- Acceptance of most tier-one companies in broad and various applications
- Leading performance
- Complete portfolio for one-stop shopping
- Global support
- On-going enhancements and cost-price reduction

3.0 Selection guide

Device	VDD	Switches channels	Applications	Signals for each group-pins
PI3USB32212	3.3V	1:2 or 2:1	USB3 10Gbps ports	Tx, Rx, D+, D-
PI3USB3102	3.3V	1:2 or 2:1	USB3 5Gbps ports	Tx, Rx, D+, D-, ID
PI3USB302	3.3V	1:2 or 2:1	USB3 5Gbps SSIC, SOC, ports (with PI3USB103)	Tx, Rx
PI2USB3212	1.5V-1.8V	1:2 or 2:1	USB3 5Gbps SSIC, SOC, ports (with PI3USB103)	Tx, Rx
PI2USB4122	1.8V	1:4 or 4:1	USB3 5Gbps SSIC, SOC	Tx, Rx

Table-1, the selection guide

4.0 Application topologies

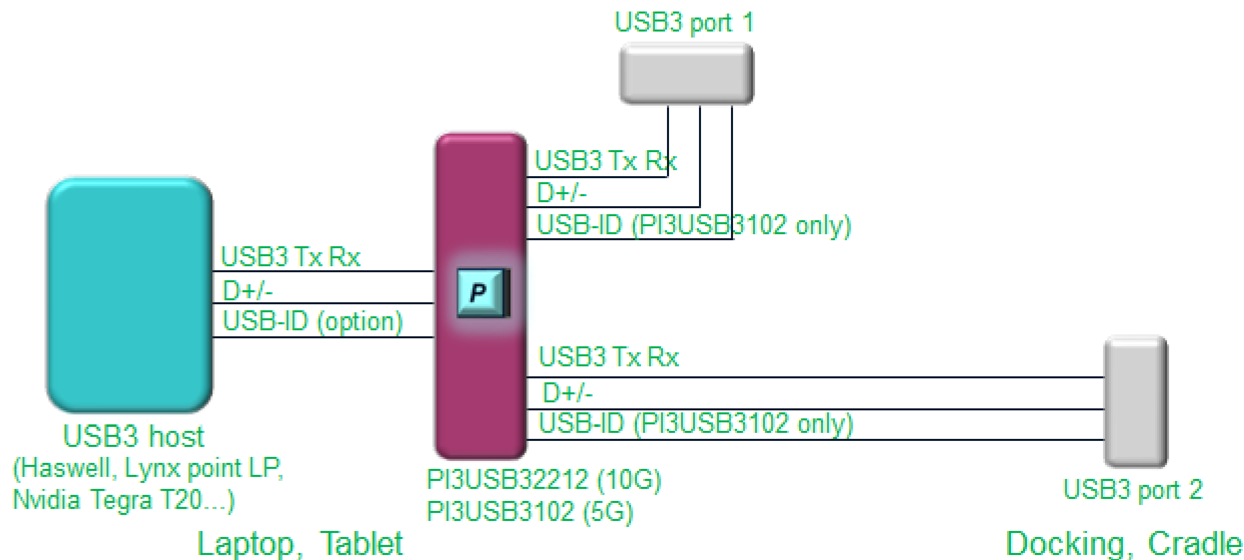

Figure 1, typical PI3USB32212 and PI3USB3102 application in laptop and docking station

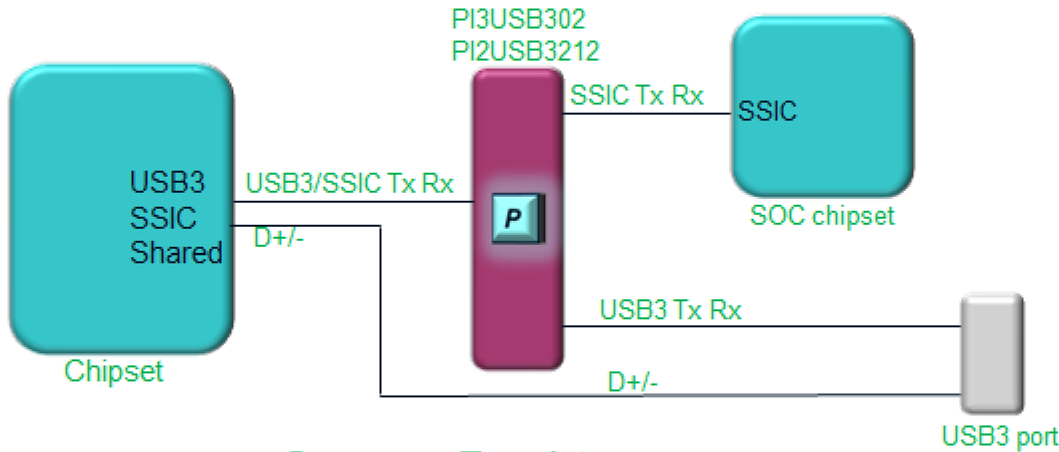

Figure 2, PI3USB302, PI2USB3212 in SSIC application

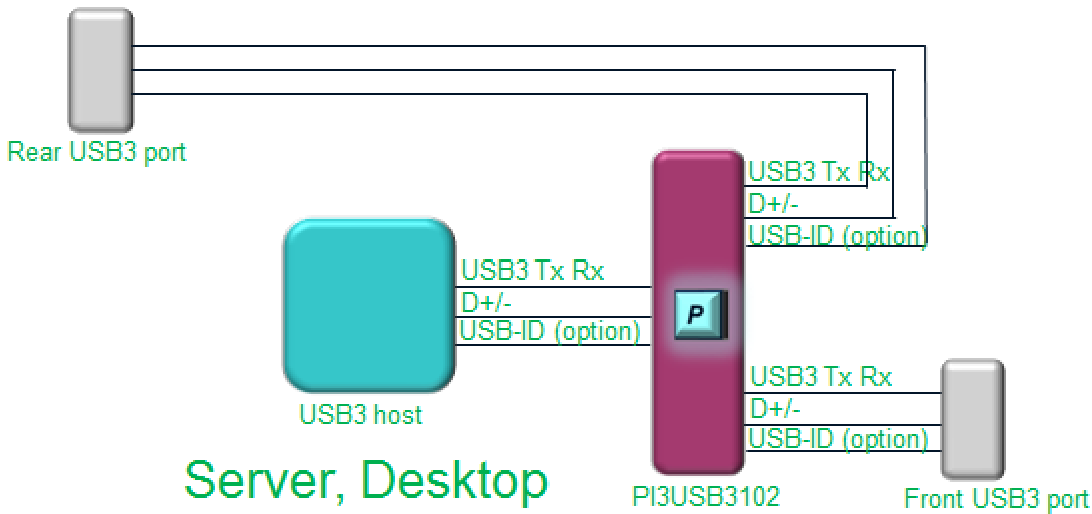

Figure 3, PI3USB3102 between front and rear USB3 ports in server desktop application

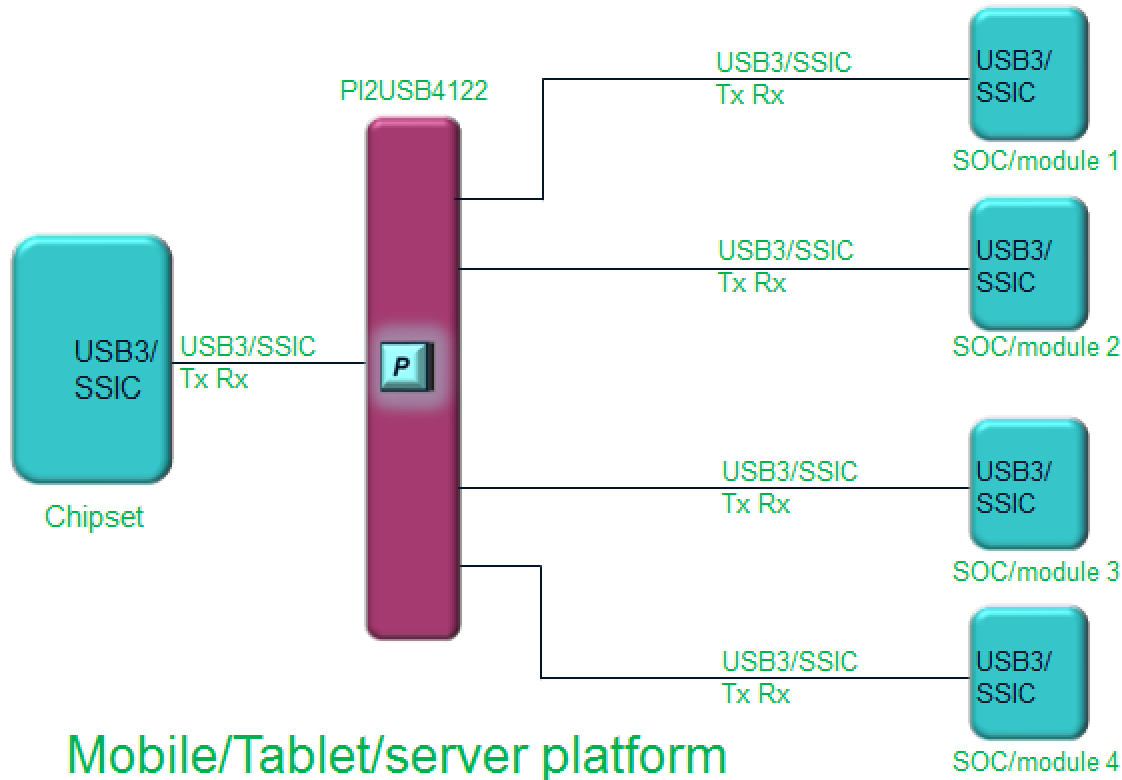

Figure 4, PI2USB4122 on mobile/Tablet/server platform for USB3/SSIC applications

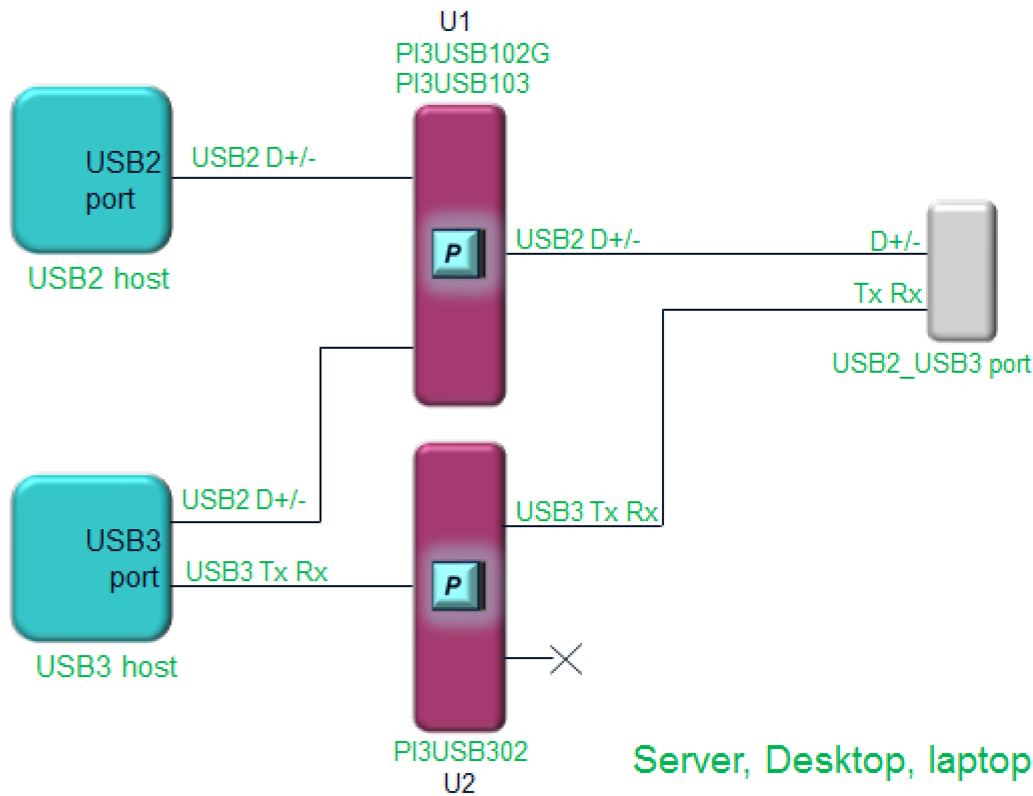

Figure 5, PI3USB302 for USB2 and USB3 hosts sharing one USB port

- When USB2 host is active and USB3 host is inactive, U1 switches USB2 host (D+/-) to USB port; U2 disconnects Tx Rx.
- When USB3 host is active and USB2 host is inactive, U1 switches USB3 host (D+/-) to USB port; U2 connects Tx Rx to USB port.

5.0 Application schematics

Figure 6, PI3USB32212 application schematic

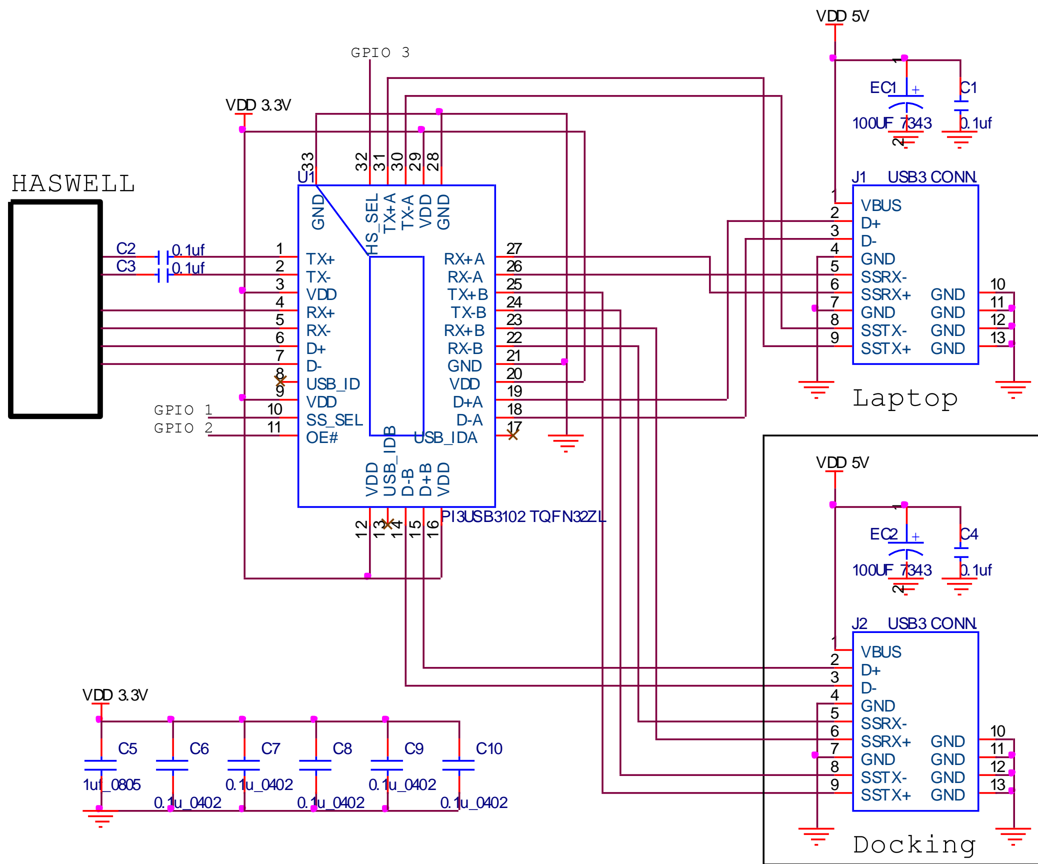

Figure 7, PI3USB3102 application schematic

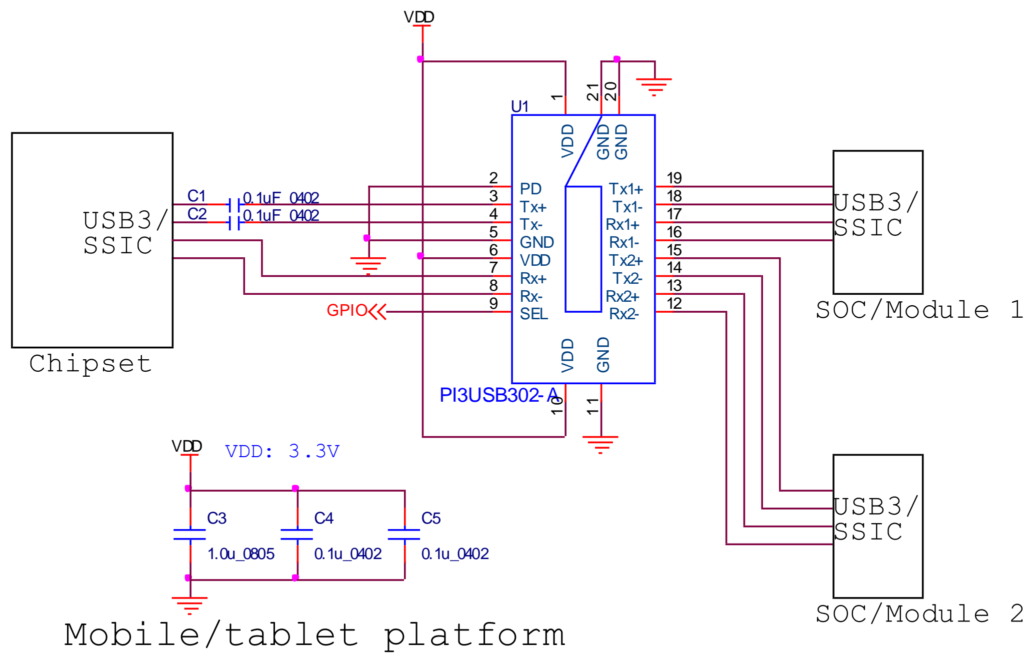

Figure 8, PI3USB302-A application schematic

6.0 Performance

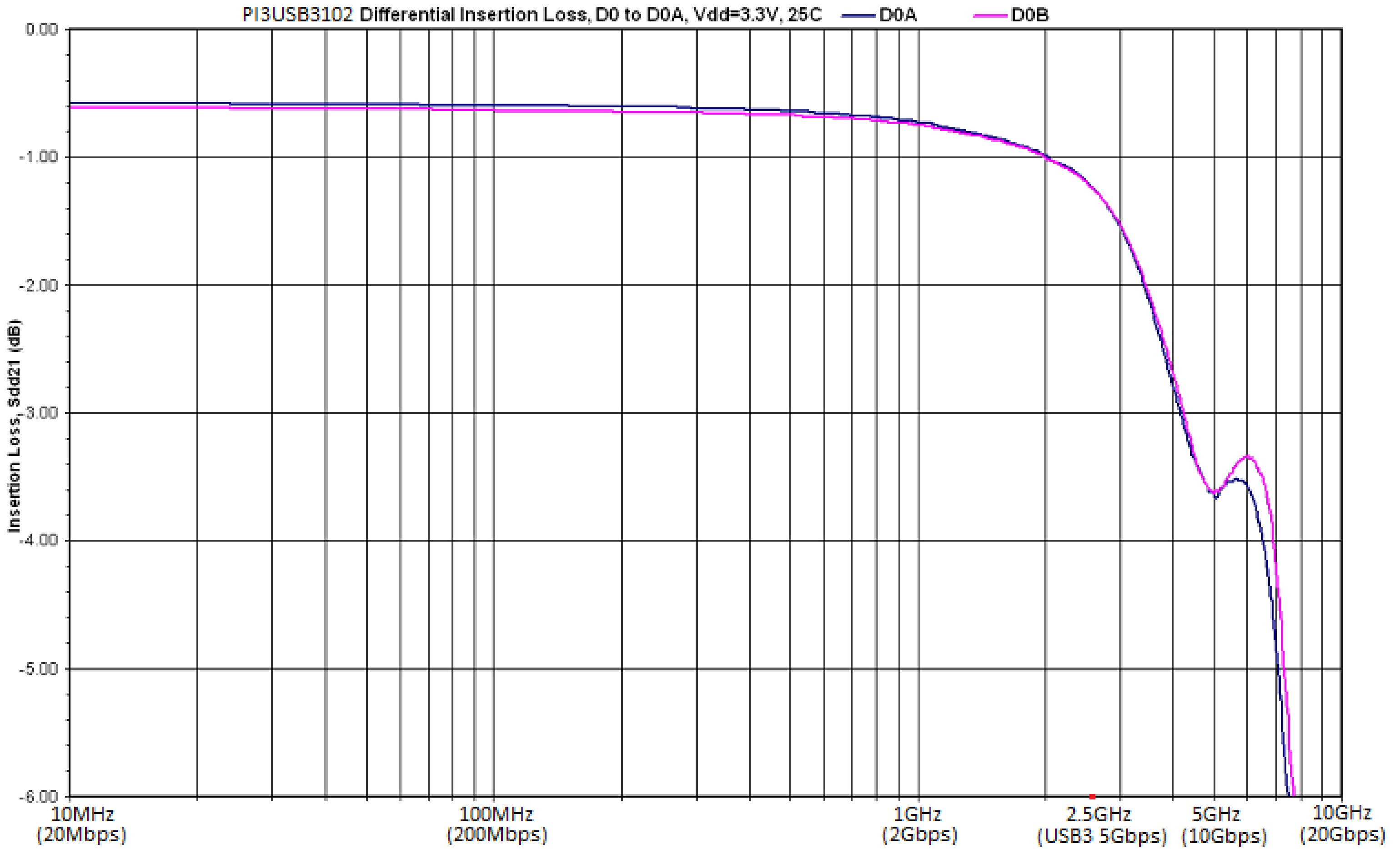

Figure 9, the insertion loss of PI3USB3102

File View Channel Sweep Calibration Trace Scale Marker System Window Help
Trigger Continuous Single Hold Restart
Sdd21
1.000dB/
0.00dB LogM
dB Sdd21
1: 308.447 kHz -0.40505 dB
2: 308.447 kHz -0.40505 dB
3: 8.427648 GHz -3.4061 dB
> 4: 4.213978 GHz -1.5264 dB
2.00
1.00
0.00
-1.00
-2.00
-3.00
-4.00
-5.00
-6.00
-7.00
-8.00
Ch1: Start 300.000 kHz
10MHz (20Mbps)
100MHz (200Mbps)
1GHz (2Gbps)
10GHz (20Gbps)
Status CH 1: Sdd21 C 4-Port Sim LCL

Figure 10, the insertion loss of PI3USB302-A

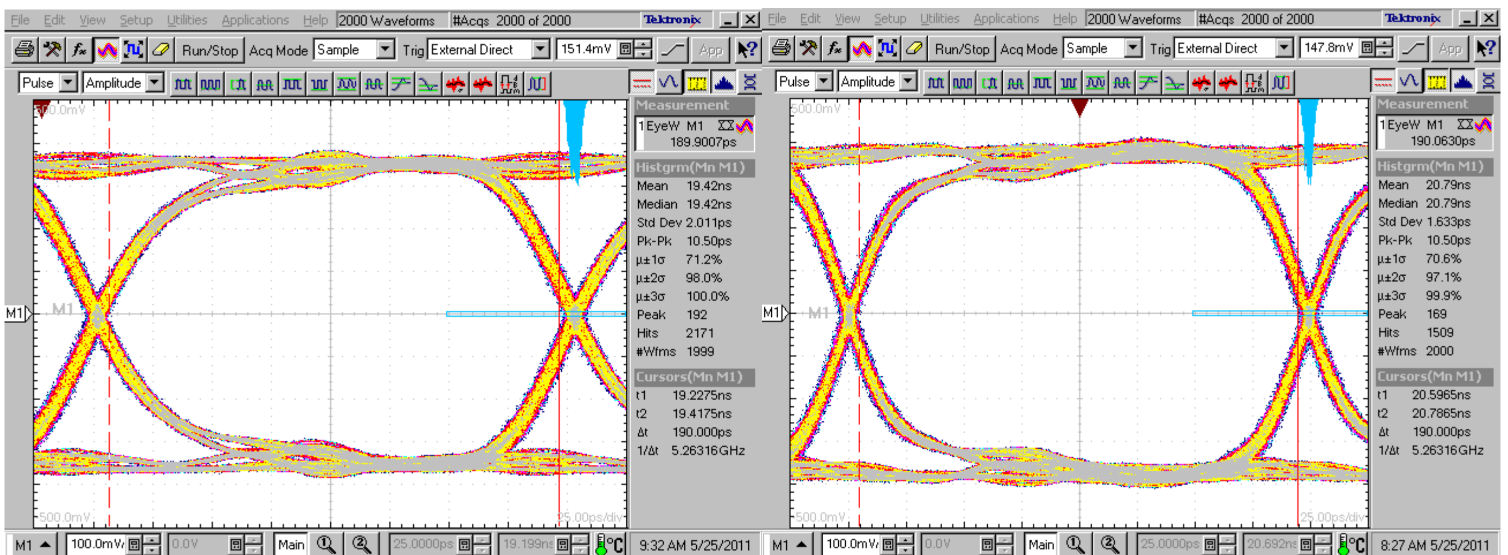

Figure 11, the eyes of with PI3USB302-A (left) and without PI3USB302-A (right, shorting PCB) at 5Gbps (2.5GHz). 1.5” input and 1.5” output traces, SMA-coaxial cable

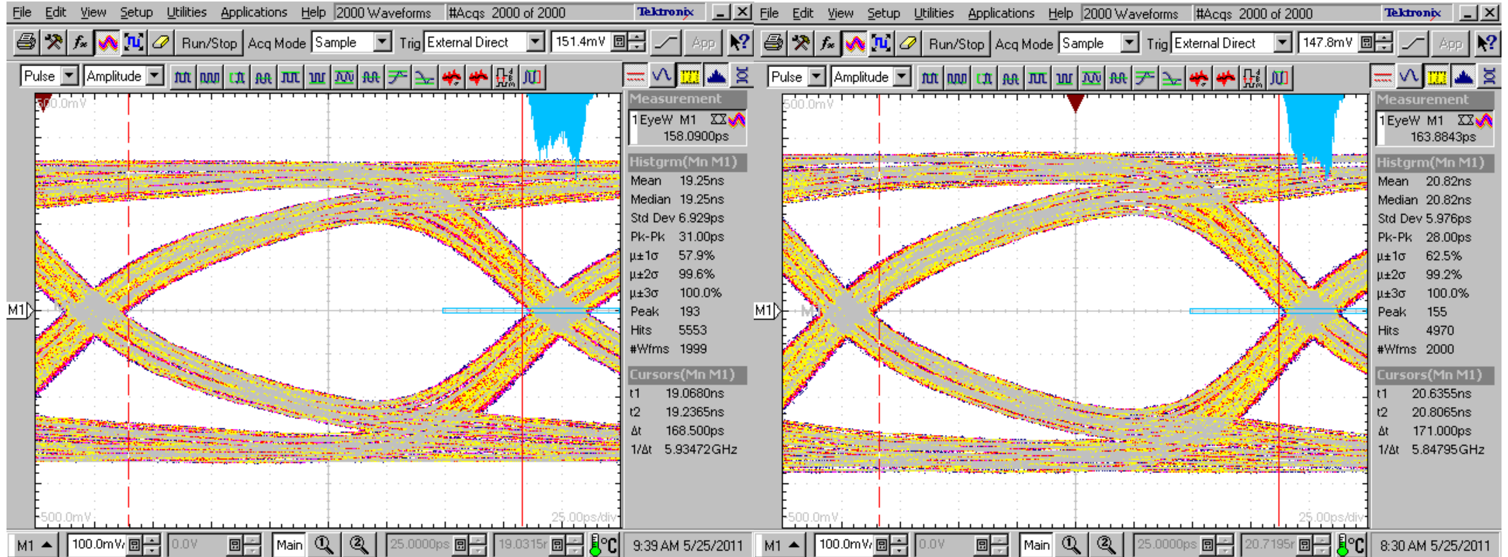

Figure 12, the eyes of with PI3USB302-A (left) and without PI3USB302-A (right, shorting PCB) at 5Gbps (2.5GHz). 12”input and 1.5” output traces, SMA-coaxial cable

7.0 Layout and power

90ohm differential impedance

Plane	Material	Thickness (mil)
Solder mask	Mask paint	1.2
Signal	Copper	1.9
Prepreg	2116	4.4
Vcc	Copper	1.4
Core		47
Vss	Copper	1.4
Prepreg	2116	4.4
Signal	Copper	1.9
Solder mask	Mask paint	1.2
Total		62.4

Table-2, the stack-up of 90ohm differential impedance

- Use 6-7-6 mils for trace-space-trace for the micro-strip lines (the traces on top and bottom layers) for 90ohm differential impedance.
- Use 6-5-6 mils for trace-space-trace for the strip-lines (the traces inside layers) for 90ohm differential impedance.
- Use FR4.
- Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro-strip lines, using ½ OZ Cu plated is ok.
- For strip-lines in 6 plus players, using 1 OZ Cu is better.
- More pair-to-pair spacing for minimal crosstalk
- Target differential Zo of 90ohm ±15ohm
- The above is only for generic reference. Impedance shall be controlled in PCB fabrication.

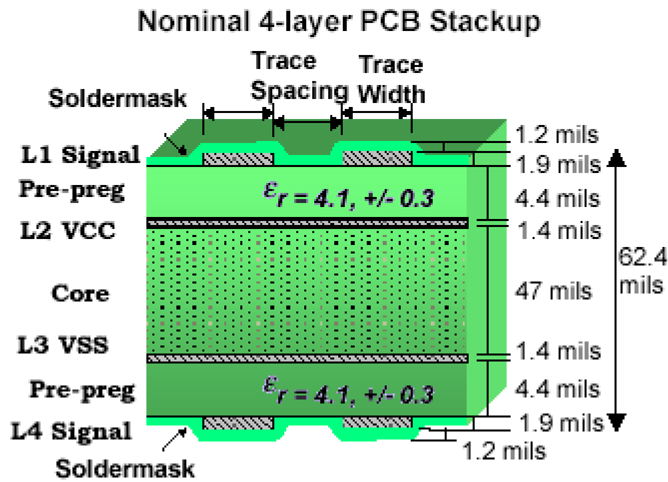

Figure 13, the PCB layers stack-up

The layout of traces

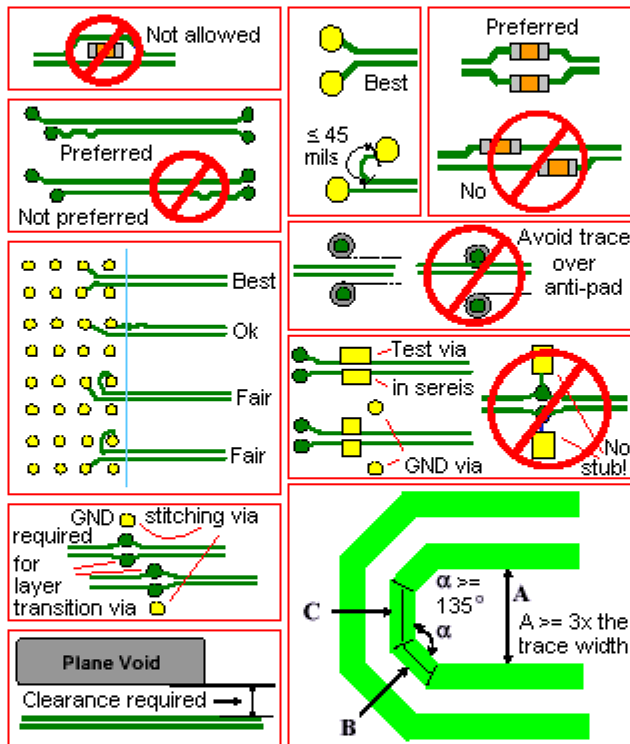

Figure 14, the layout of traces

Vdd bypass capacitance and power-ground layers

- Use 0.1uf in size of 0402 for all the Vdd (any power pins) pins of the IC device, as close to the Vdd pins as possible, within 2-3mm if feasible.
- Use dedicated Vdd and GND planes if feasible to minimize the jitters.