For the customer use only

PI2EQX6874ZFE SATAConn EvalBoard Rev.A User Guide

Introduction

Pericom Semiconductor's PI2EQX6874ZFE is a low power, SAS2, SATA, XAUI signal Re-Driver. The device provides programmable equalization, amplification, and emphasis by using 8 elect bits, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference.

PI2EQX6874ZFE supports eight 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides fl edibility with signal integrity of the signal before the re-driver, whereas the integrated emphasis circuitry provides flexibility with signal integrity of the signal after the reDriver.

In addition to providing signal re-conditioning, Pericom's PI2EQX6874ZFE also provides power management Stand-by mode operated by a Power Down pin.

This design guide describes how to use PI2EQX6874ZFE SATA ReDriver in the SATAConn EVB. Figure1 shows top view and bottom view of PI2EQX6874ZFE SATAConn EVB. This EVB is just for SATA application using SATA connector.

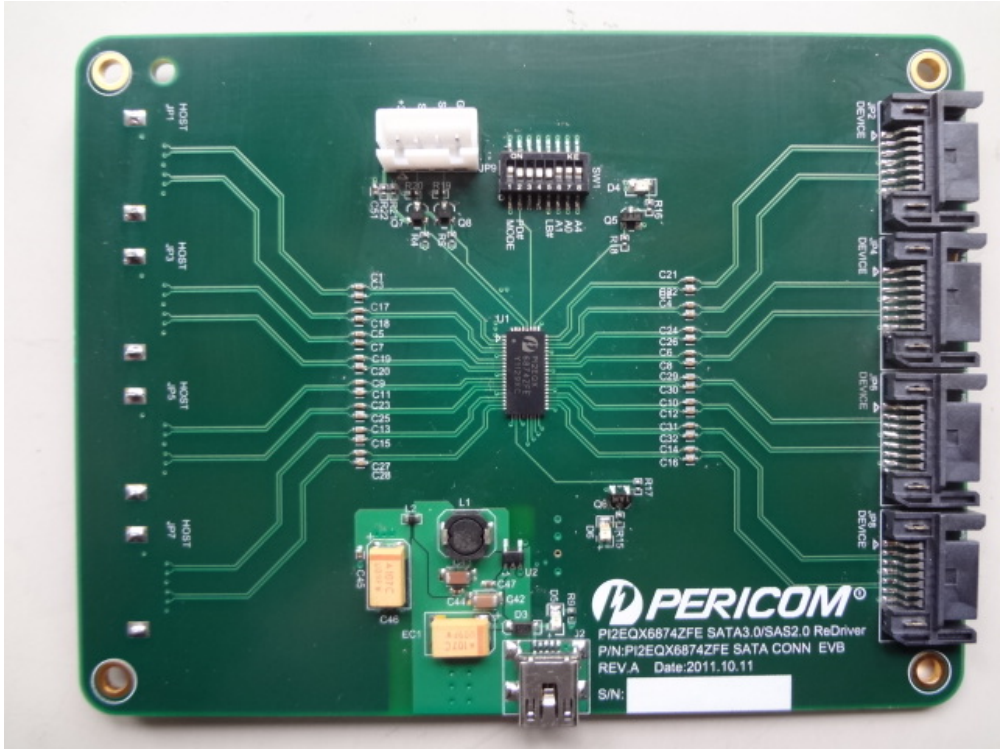


Figure1a Top View of PI2EQX6874ZFE SATAConn EVB

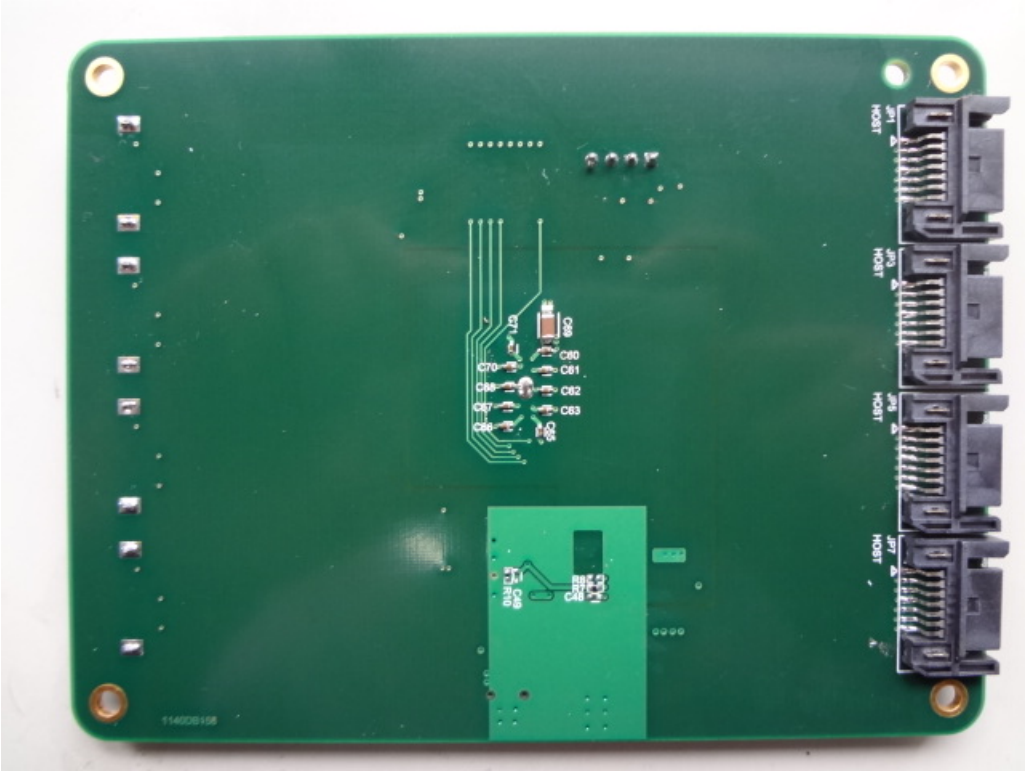


Figure1b Bottom View of PI2EQX6874ZFE SATAConn EVB

Board Operation

- **Logical Block Diagram**

Figure2 shows the logical block diagram of PI2EQX6874ZFE.

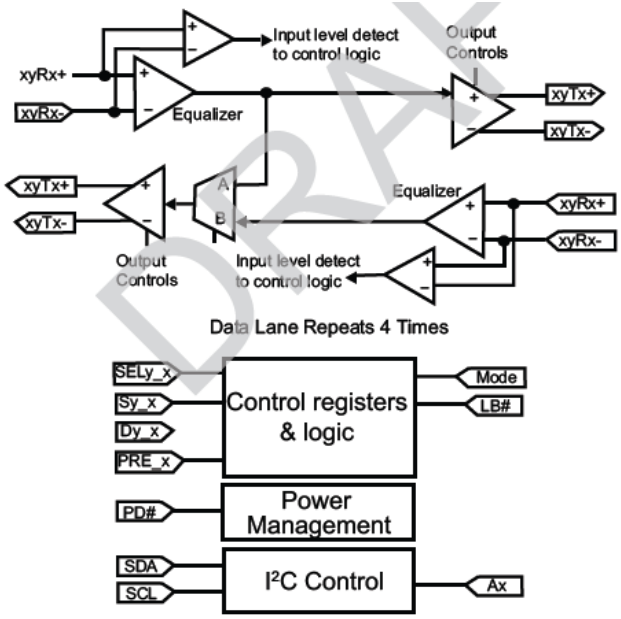


Figure2. Logical Block Diagram of PI2EQX6874ZFE

Board Circuit

1) Power Supply

On the demo board, the power supply is from one miniUSB connector (**J1**) by +5V power transforming to +1.2V for PI2EQX6874ZFE. Figure3 shows the power circuit.

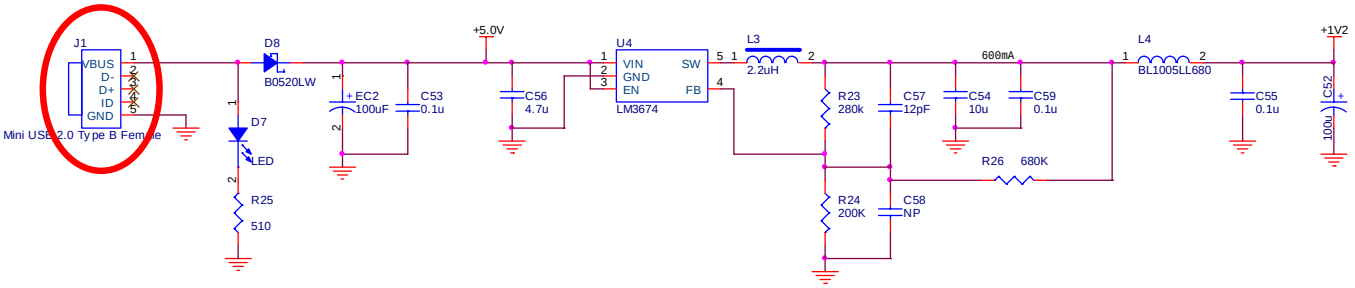


Figure3. Power Circuit for PI2EQX6874ZFE SATAConn EVB

Figure4 shows the location for **J1**.

Figure4. **J1** location on PI2EQX6874ZFE SATAConn EVB

2) Configuration Control

PI2EQX6874ZFE provides I2C configuration control depending on the state of the MODE pin input (red circle in Figure5.

When MODE is set **LOW**, reprogramming of the control registers via I2C is allowed. MODE pin has internal 100K pull-up resistor. So it should be pull down by Jumper MODE pin externally.

Figure5 shows the switch and location of these configuration control pins on the EVB.

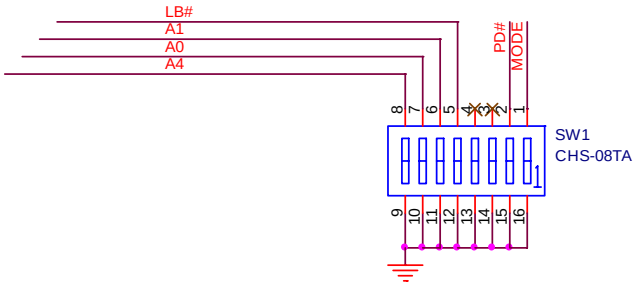


Figure5a Control Pin connecton with SW1

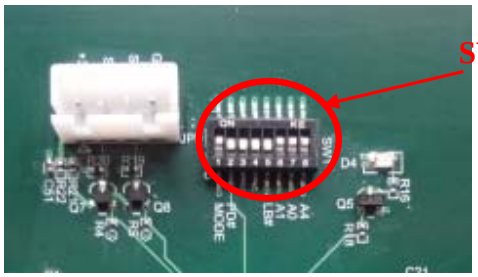


Figure5b SW1, SW2 and SW3 location on PI2EQX6874ZFE SATAConn EVB

- The integrated I2C interfaces operate as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode and LSB indication either a read or write operation as shown below. The address for a specific device is determined by **A0, A1 and A4** pins with internal **PULL-UP** resistors. So up to eight PI2EQX6874 devices can be connected to a single I2C bus. Figure4 shows A4, A1 and A0 pin header location in red circle.

Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	Program	0	0	Programmable		1=R, 0=W

- Data bytes must be 8-bits long and transferred with MSB first. Please see I2C data transfer diagram in Page16 of datasheet. For data byte definition as below, please see Page10 -12 of datasheet in detail.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RSVD	Reserved for future use
2	LBEC	Loopback and De-emphasis Control, provides for control of the loopback function and de-emphasis mode (de-emphasis or de-emphasis)
3	INDIS	Channel Input Disable, controls whether s channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable, controls whether a channel output buffer is enabled or disabled.
5	A0	Channel A0 configuration
6	B0	Channel B0 configuration
7	A1	Channel A1 configuration
8	B1	Channel B1 configuration
9	A2	Channel A2 configuration
10	B2	Channel B2 configuration
11	A3	Channel A3 configuration
12	B3	Channel B3 configuration
13	VTH	Input level threshold configuration
14	RSVD	Reserved for future use

- For I2C inputs, SCL and SDA pin are tolerant with **+3.3V power.** Figure5 is SCL and SDA pins location on EVB.

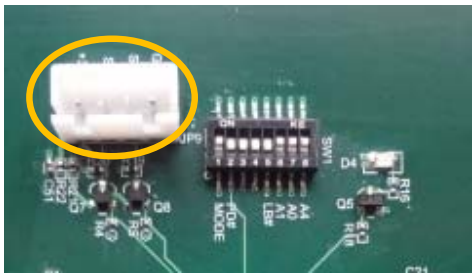


Figure5. SCL and SDA pin Header Location

NOTE: PD# and LB# should be NC if I2C mode is selected.

Figure6 shows input equalizer selection table for Channel A and B.

SEL2_[A:B]	SEL1_[A:B]	SEL0_[A:B]	@1.5GHz	@3.0GHz
0	0	0	0.8dB	1.5dB
0	0	1	1.0dB	1.9dB
0	1	0	1.5dB	3.2dB
0	1	1	2.5dB	5.2dB
1	0	0	3.5dB	6.9dB
1	0	1	4.4dB	8.3dB
1	1	0	5.9dB	10.4dB
1	1	1	8.7dB	13.8dB

Figure6 Input equalizer selection table for Channel A and B

Figure7 shows output configuration table for Channel A and B.

S1_[A:B]	S0_[A:B]	Swing (Differential)
0	0	1.1V
0	1	0.5V
1	0	0.8V
1	1	1.0V

D2_[A:B]	D1_[A:B]	De-emphasis
0	0	2.5dB
0	1	4.5dB
1	0	6.5dB
1	1	8.5dB

Figure7 Output Configuration Table for Channel A and B

- I2C Configuration Sequence

Figure8 is WRITE sequence.

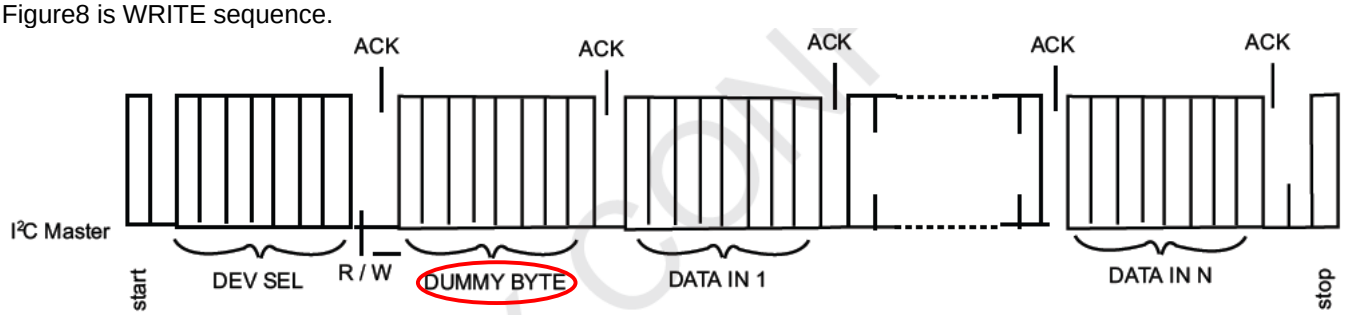


Figure8 I2C WRITE Sequence Diagram

Note: there is one DUMMY byte to be added into sequence.

Figure9 is one sample for write sequence at Address=**C0** (A4, A1, A0 are pulled down) and Data byte[0..11]=00,00,FE,00,00,FF,FF,FF,FF, FF,FF,FF,FF,EF,C0.

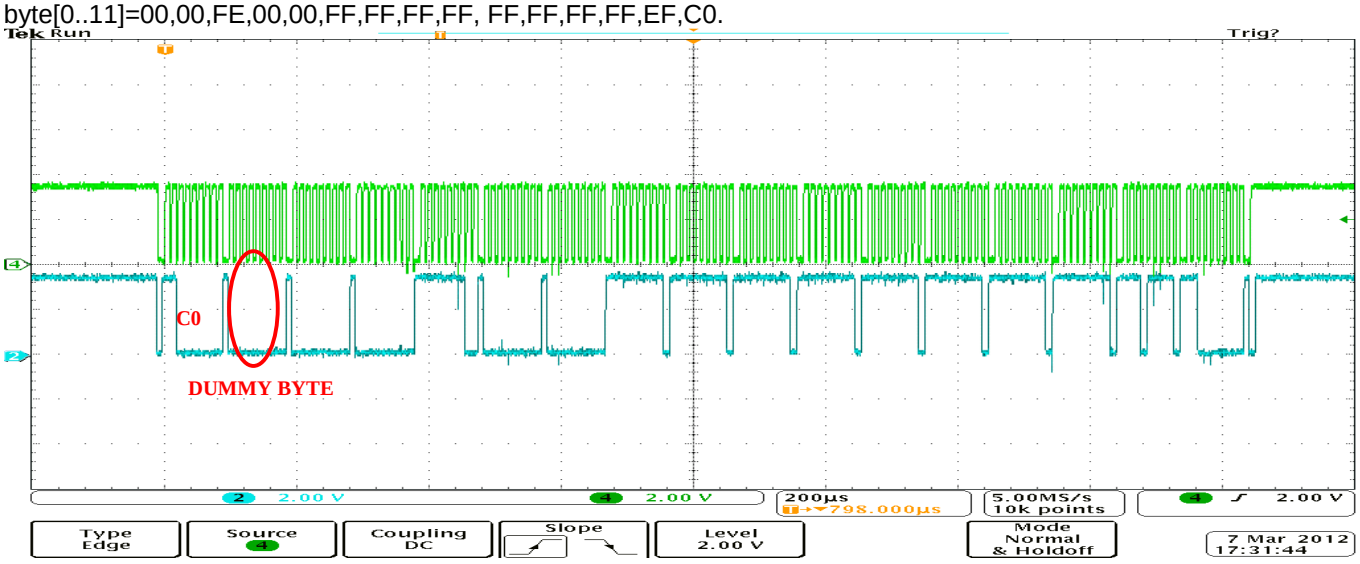


Figure9 I2C WRITE Sequence Sample

Figure10 is READ sequence.

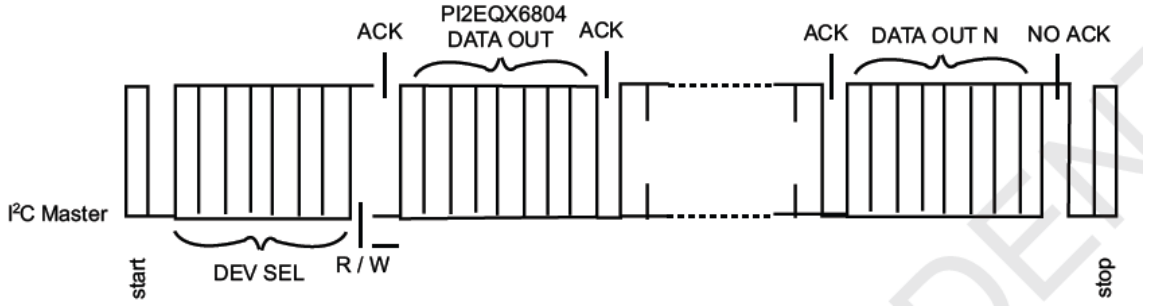


Figure10 I2C READ Sequence Diagram

Note: there is NO DUMMY byte to be added into sequence.

Figure11 is one sample for read sequence sample at Address=**C1** (A4, A1, A0 are pulled down) and Data byte[0..14]=**00**, 00,FE,00,00,FF,FF,FF,FF, FF,FF,FF,FF,EF,C0.

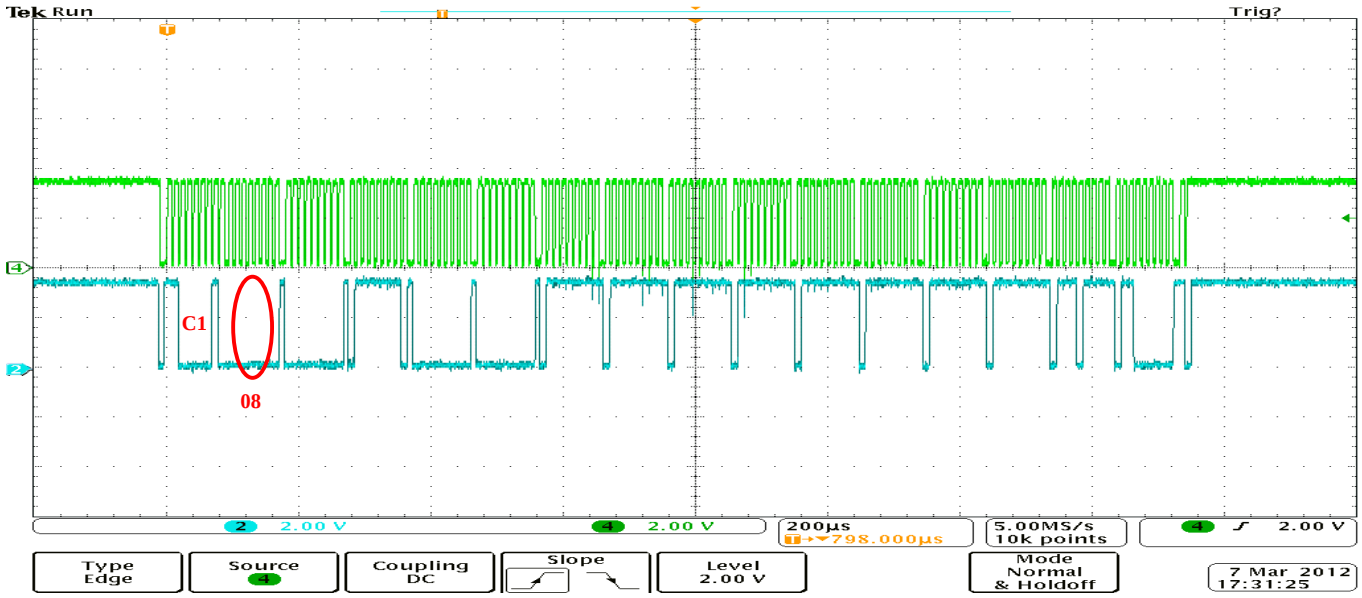
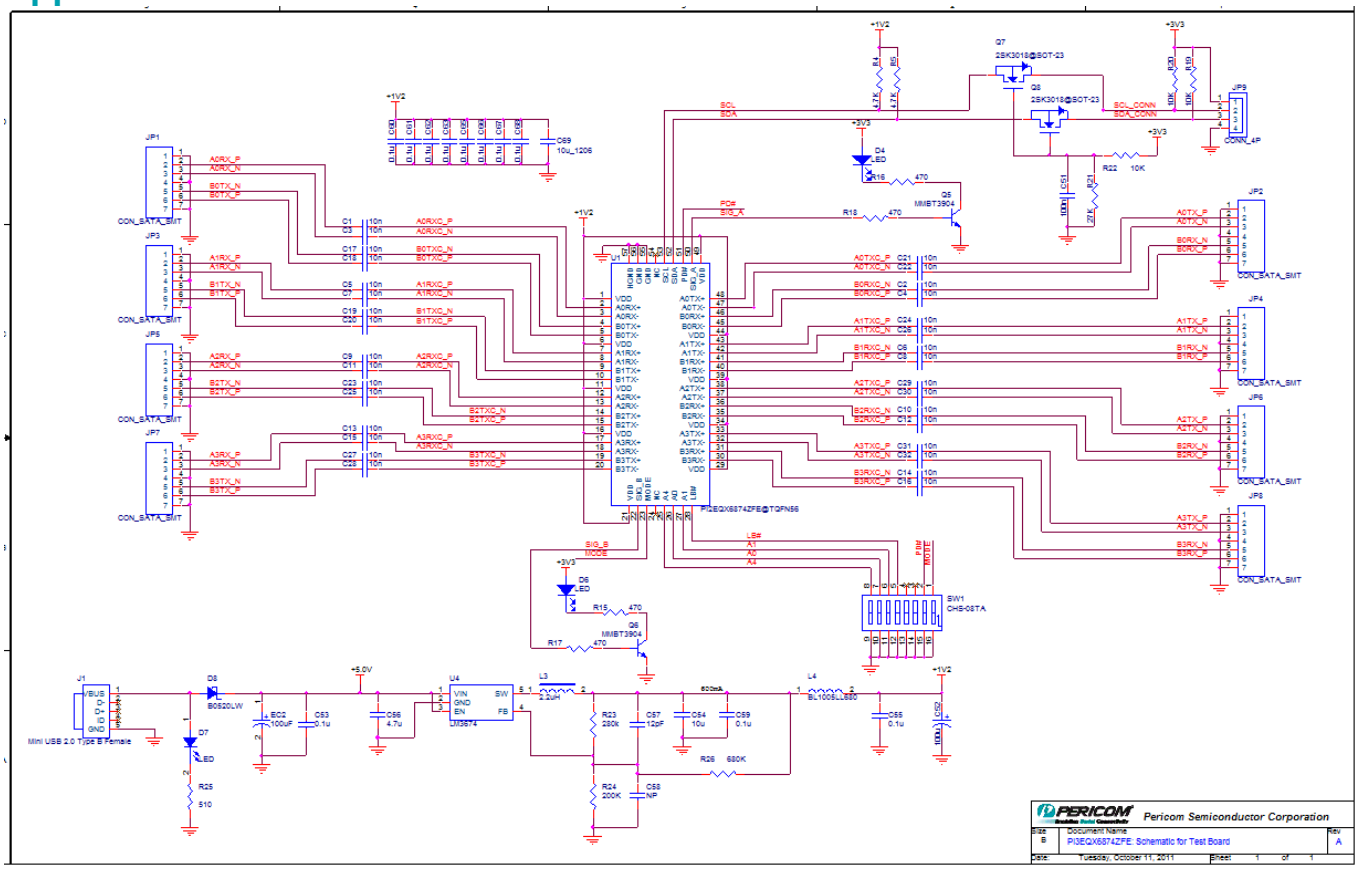


Figure11 I2C READ Sequence Sample

Note: Byte0=**00** means no channel has signal input.

Appendix A: PCB Schematic



History

Version 1.0	Original Version	Mar.7, 2012