PI2EQX6874ZFE
4-lane SAS/SATA ReDriver Application Information

Contents

General Introduction
PI2EQX6874ZFE is FOUR-Lane SAS/SATA redrivers to support up to 6Gbps signal, and they provide flexible output strength and de-emphasis controls separately on each lane to provide the optimum signal to pre-compensate for losses across long trace or noisy environments so that the receiver gets a clean with good eye opening. PI2EQX6874ZFE only provides I2C function set output swing/de-emphasis and input equalization.

Packaging: 56-contact TQFN (5x11mm) for PI2EQX6874ZFE

Main Application:
- ✓ ***Server***
- ✓ ***Desktop***
- ✓ ***Storage/Workstation***

Figure1 is typical application sample.

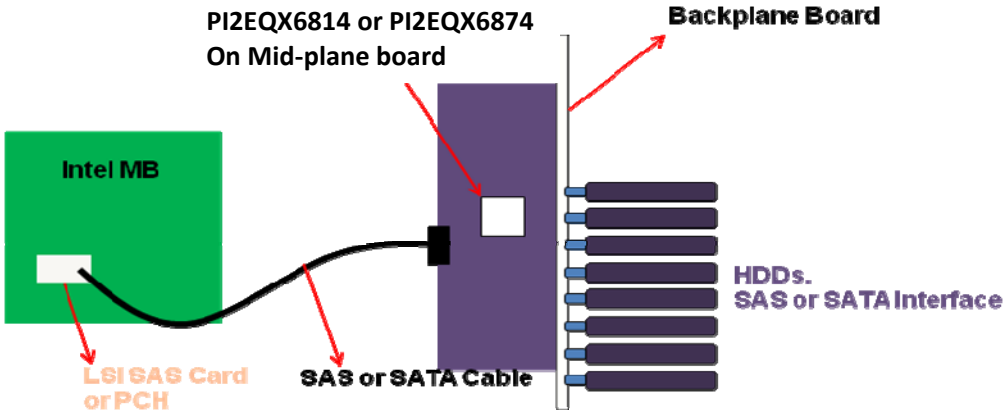


Figure1a Typical Application Sample

How to use I2C control for output swing/de-emphasis and input equalization of PI2EQX6874

For PI2EQX6874, it provides one way as below to set output swing/de-emphasis and input equalization. And the way depends on the state of the MODE pin with 100k internal pull-up resistor.

Note: Control of input/output configuration is separated for the A and B channels, so that each channel within group may have the different setting.

When MODE pin is set HIGH, the configuration only has some selection, not for all table value. So it is not recommended to use.

When MODE pin is LOW, all the internal configuration registers can be programmed by I2C function. Note that during initial power-on, the value at the configuration input pins will be latched to the configuration registers as initial startup states.

Note: Each channel is independtently controlled for input equalizer, output swing and output de-emphasis.

- The integrated I2C interfaces operate as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode and LSB indication either a read or write operation as shown below. The address for a specific device is determined by A0, A1 and A4 pins with internal pull-up resistors. So up to eight PI2EQX6874 devices can be connected to a single I2C bus.

Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	Program	0	0	Programmable		1=R, 0=W

- Data bytes must be 8-bits long and transferred with MSB first. Please see I2C data transfer diagram in Page13 of datasheet. For data byte definition as below, please see Page8 -11 of datasheet in detail.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RSVD	Reserved for future use
2	LBEC	Loopback and De-emphasis Control, provides for control of the loopback function and de-emphasis mode (pre-de-emphasis or de-emphasis)
3	INDIS	Channel Input Disable, controls whether s channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable, controls whether a channel output buffer is enabled or disabled.
5	A0	Channel A0 configuration
6	B0	Channel B0 configuration
7	A1	Channel A1 configuration
8	B1	Channel B1 configuration
9	A2	Channel A2 configuration
10	B2	Channel B2 configuration
11	A3	Channel A3 configuration
12	B3	Channel B3 configuration
13	VTH	Input level threshold configuration
14	RSVD	Reserved for future use

- For I2C inputs, SCL and SDA pin are tolerant with +3.3V power.
- For I2C configuration sequence in detail, please see Page6-7 in this file.

External Components Requirement

PI2EQX6874 require AC coupling capacitors for all redriver inputs and outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

- **Layout Considerations for Differential Pairs**
  - ✓ The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
  - ✓ Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
  - ✓ Target differential Zo of 100ohm ±20%
  - ✓ More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
  - ✓ It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
  - ✓ The use of vias should be avoided if possible, if vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
  - ✓ Route the differential signals away from other signals and noise sources on the printed circuit board

- **PCB Layout Trace Routings**

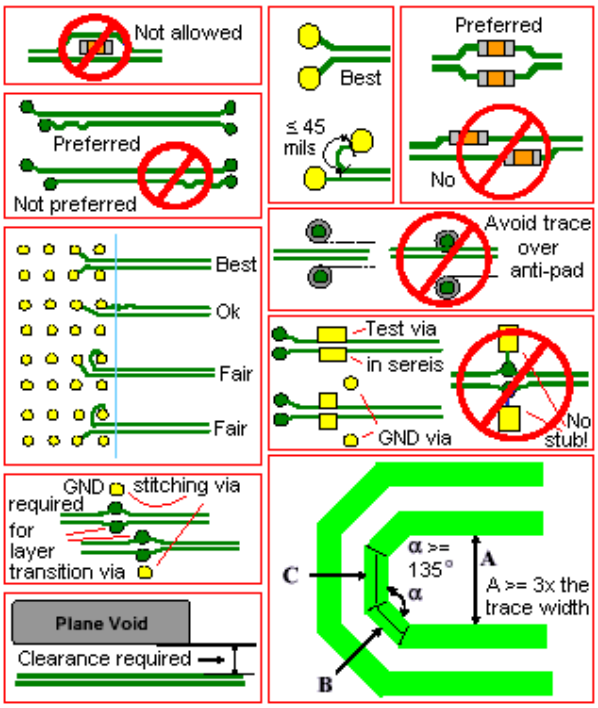


Figure2 Layout Sample for Trace Routings

Power-Supply bypass

More careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply; there are some approaches as recommendation.

- ✓ The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- ✓ The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
- ✓ Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PI2EQX6874. Smaller body size capacitors can help facilitate proper component placement. The distance of capacitors to IC body should be <100mil.

- ✓ One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommened for all devices. Always apply GND and VDD before applying signals., especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization Setting

- **Various Input Trace and Eye Test with different EQ setting**

Figure3 is PI2EQX6874 test setup for different EQ setting, R is PI2EQX6874.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB

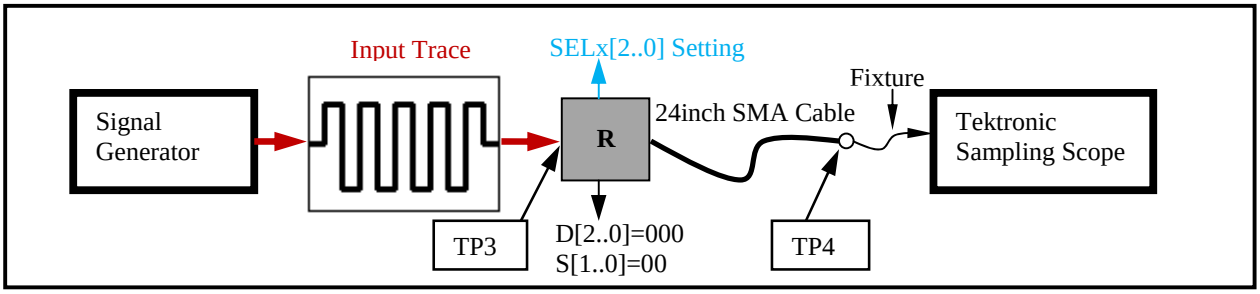
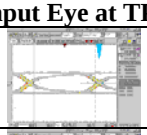
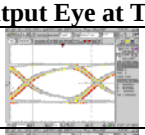
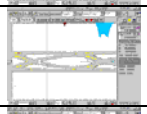
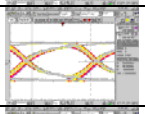
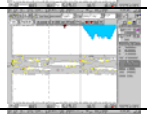
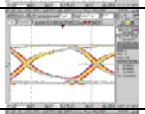
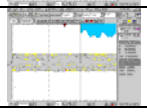
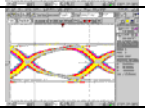


Figure3 PI2EQX6874 test setup for different equalization setting

Table1 Eye Diagram at TP4 vs. Input FR4 trace and EQ setting at 6Gb/s for PI2EQX6874

	Input Trace Length	SEL[2..0] Setting	Input Eye at TP3	Output Eye at TP4
Eye Diagram vs. EQ setting at 6Gb/s	6 inch FR4 Lab trace (-2dB loss at 6GHz)	3.2dB (SEL[2,1,0] =010)		
	18 inch FR4 Lab trace (-6dB loss at 3GHz)	6.9dB (SEL[2,1,0] =100)		
	30 inch FR4 Lab trace (-10dB at 3GHz)	10.4dB (SEL[2,1,0] =110)		
	48 inch FR4 Lab trace (-16dB at 3GHz)	13.8dB (SEL[2,1,0] =111)		

Output Swing Setting

Figure4 is PI2EQX6874 test setup for different output swing setting, R is PI2EQX6874.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

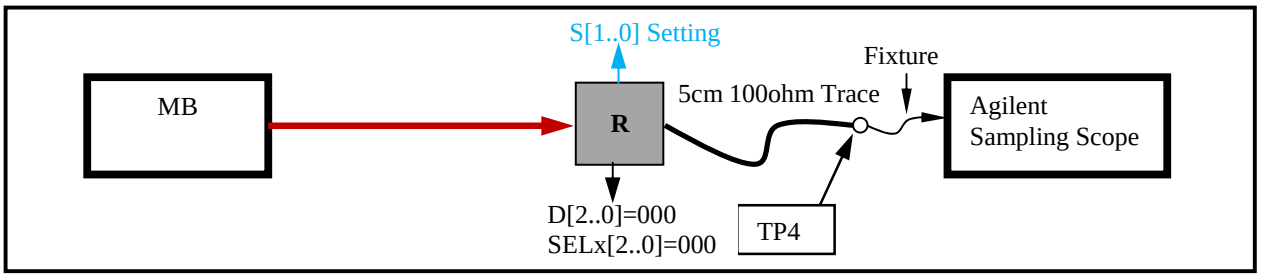
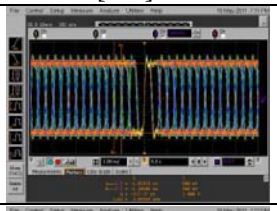
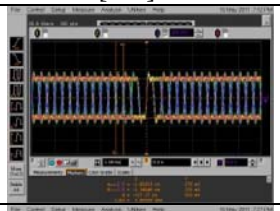
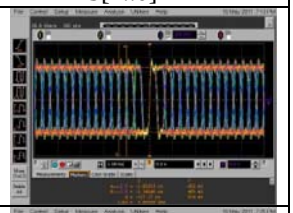
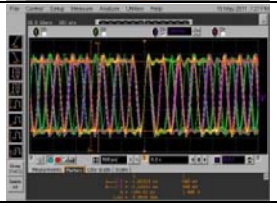
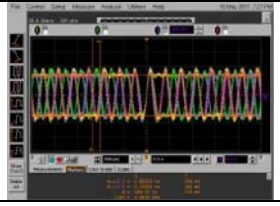


Figure4 PI2EQX6874 test setup for different output swing setting

Table2 Output Swing at TP4 vs. OS setting at 3Gb/s and 6Gb/s for PI2EQX6874

	S[1..0]=00	S[1..0]=01	S[1..0]=10	S[1..0]=11
Output Swing at TP4 vs. OS setting at 3Gb/s				
Output Swing at TP4 vs. OS setting at 6Gb/s				

De-emphasis Setting

Figure5 is PI2EQX6874 test setup for different De-emphasis setting, R is PI2EQX6874.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

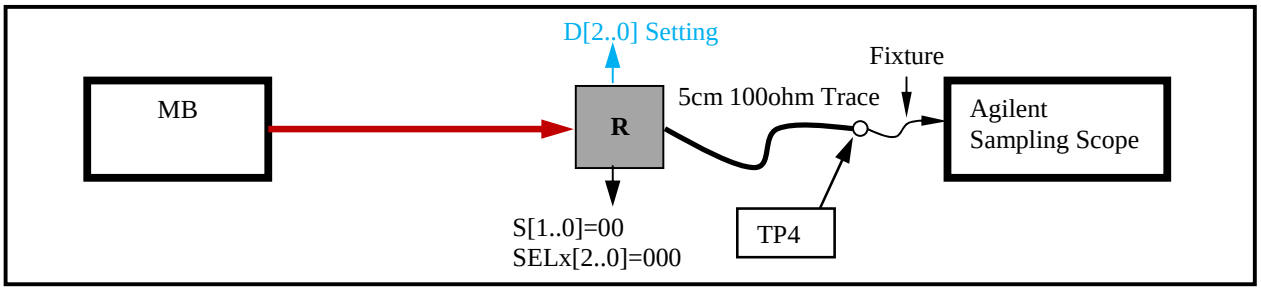
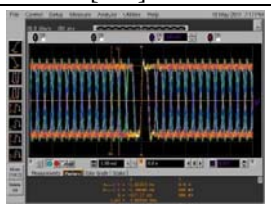
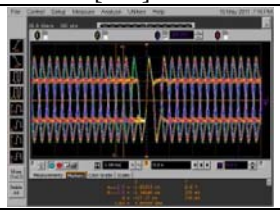
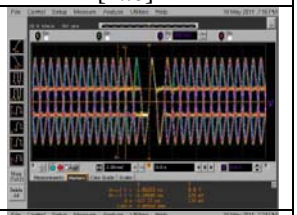
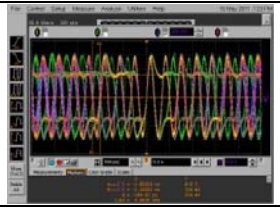
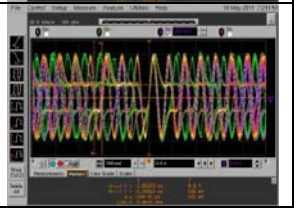


Figure5 PI2EQX6874 test setup for different De-emphasis setting

Table3 De-emphasis at TP4 vs. D[2..0] setting at 3Gb/s and 6Gb/s for PI2EQX6874

	D[2..0]=000	D[2..0]=010	D[2..0]=111
Output De-emphasis at TP4 vs. De-em setting at 3Gb/s			
Output De-emphasis at TP4 vs. De-em setting at 6Gb/s			

I2C Configuration Sequence

Figure6 is WRITE sequence.

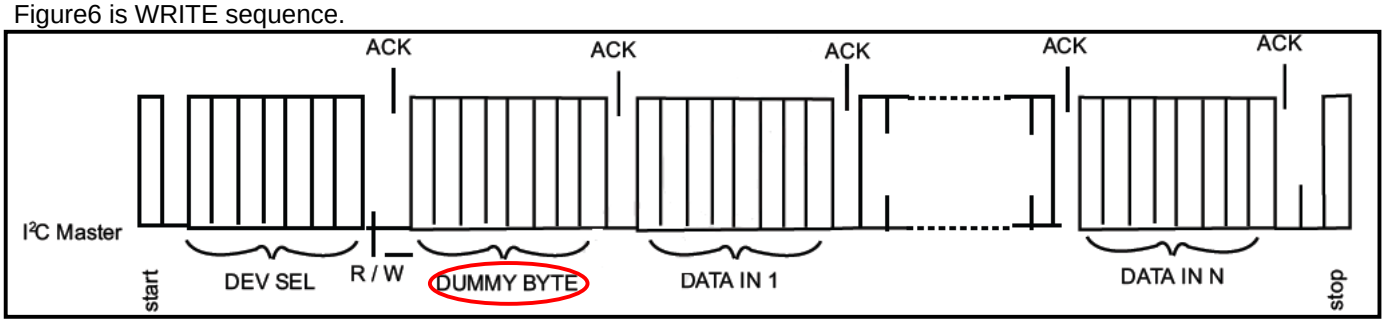


Figure6 I2C WRITE Sequence Diagram

Note: there is one DUMMY byte to be added into sequence.

Figure 7 is one sample for write sequence at Address=**C0** (A4, A1, A0 are pulled down) and Data byte[0..11]= 00 00 FE 00 00 FF FF FF FF FF FF FF FF EF 00.

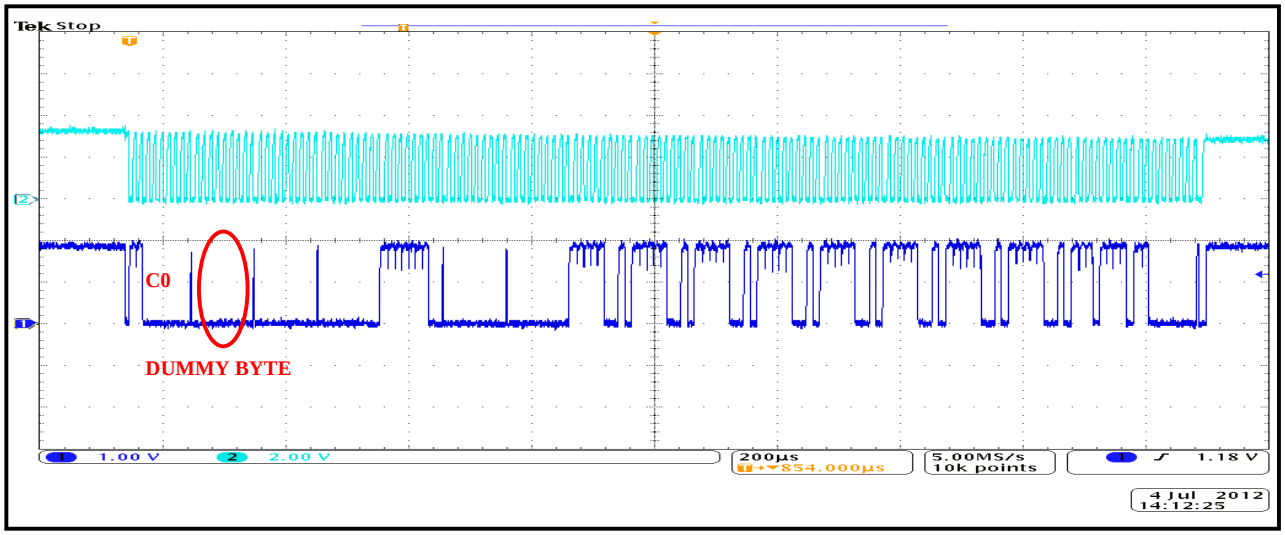


Figure7 I2C WRITE Sequence Sample

Figure8 is READ sequence.

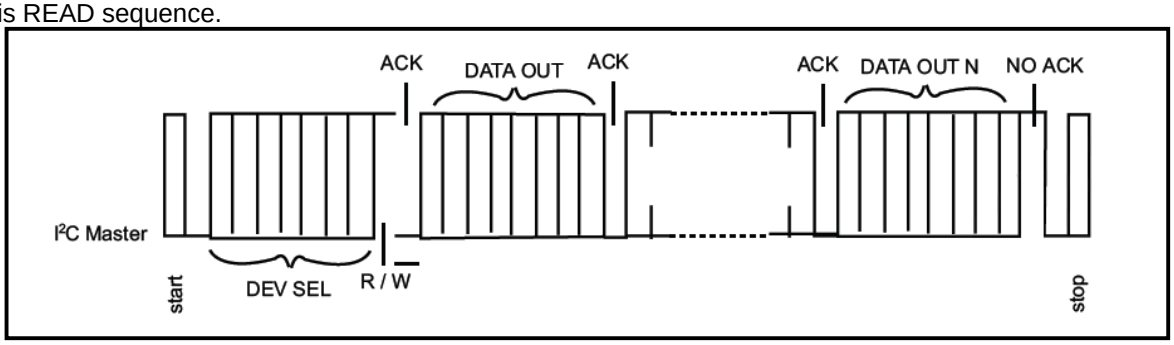


Figure8 I2C READ Sequence Diagram

Note: there is NO DUMMY byte to be added into sequence.

Figure9 is one sample for read sequence sample at Address=**C1** (A4, A1, A0 are pulled down) and Data byte[0..11]= 00 00 FE 00 00 FF FF FF FF FF FF FF FF EF 00.

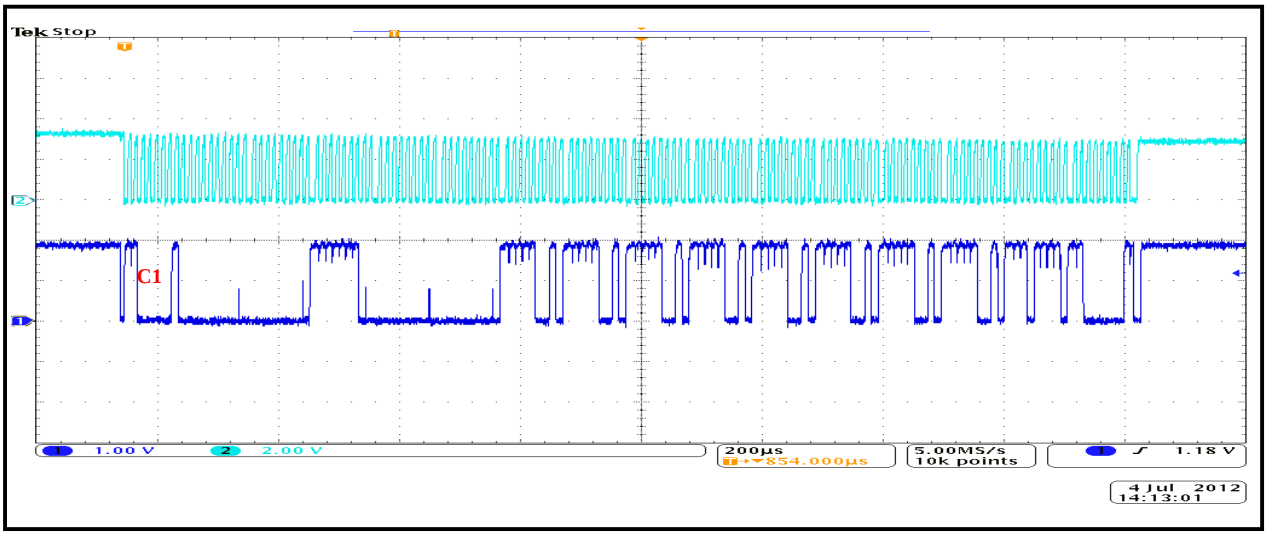


Figure9 I2C READ Sequence Sample

Note: Byte0 means Channel-A2 has signal input.

Typical Application Circuit

Figure10 shows typical application circuit of PI2EQX6874.

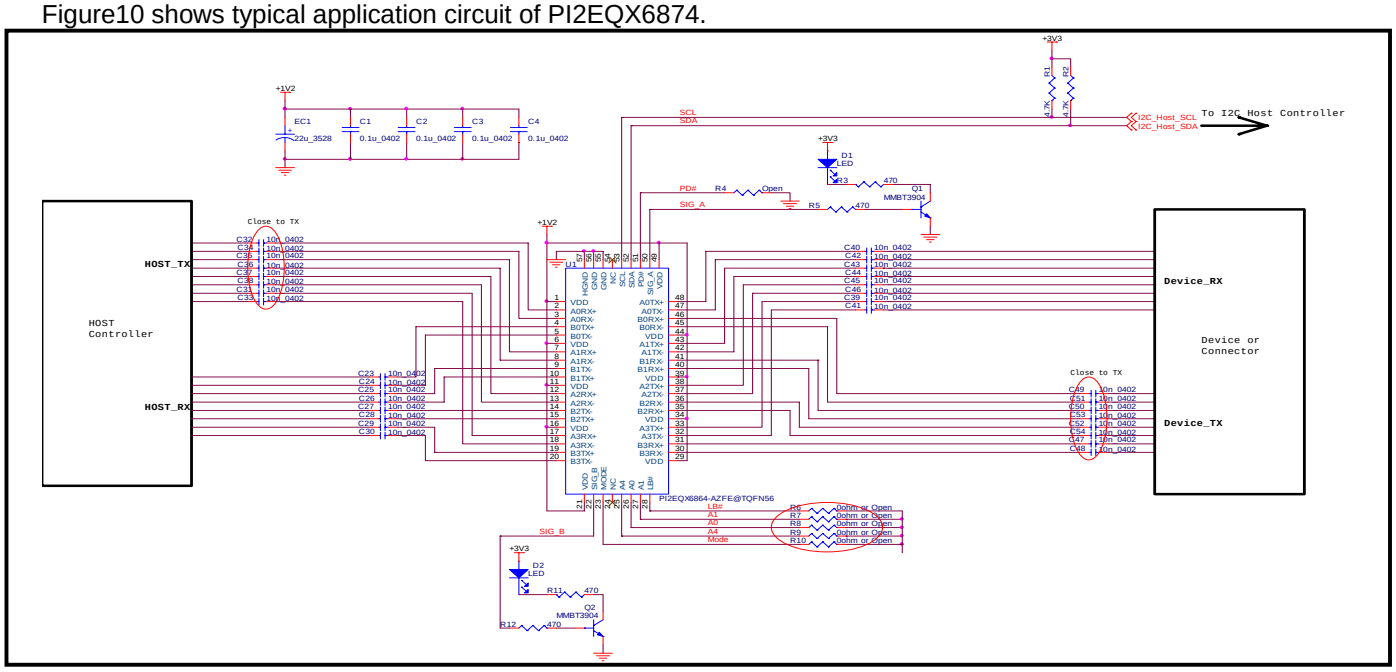


Figure10 Typical Application Circuit of PI2EQX6874

PCB Layout Sample

Figure11 shows typical layout routing of PI2EQX6874.

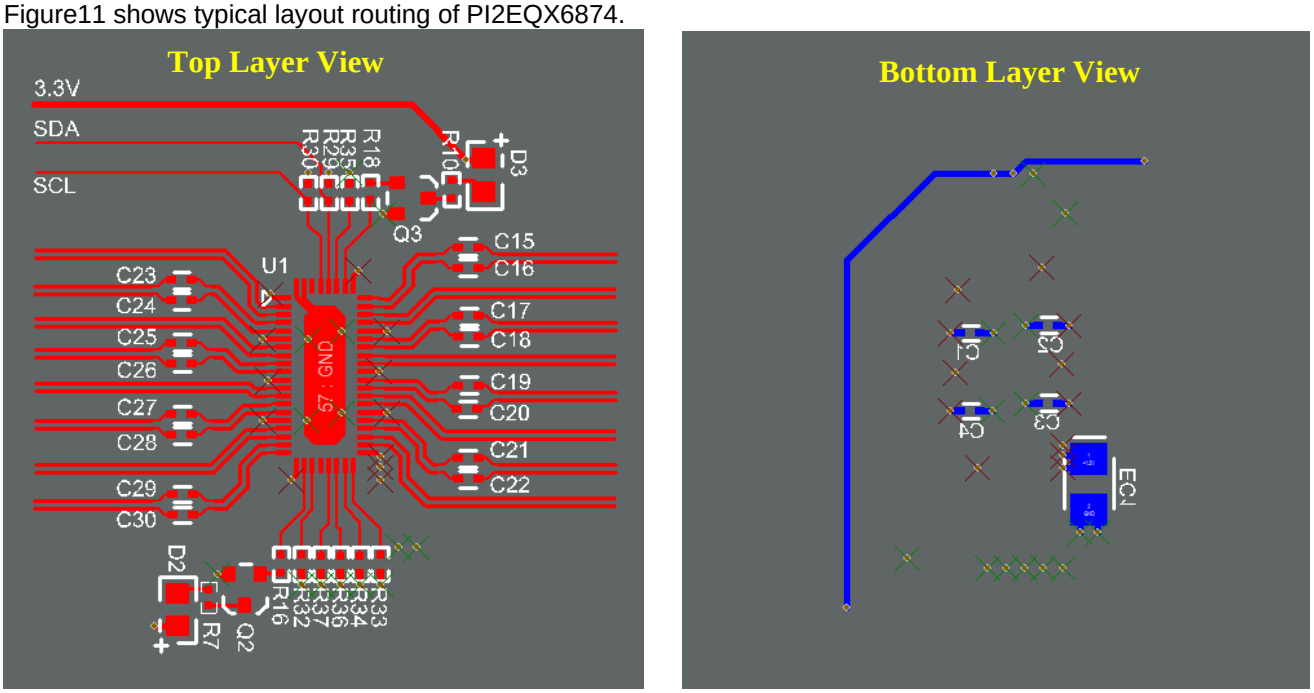


Figure11 Typical Layout Routing of PI2EQX6874

Pericom SATA/SAS ReDriver Selection Table

ReDriver P/N	Protocol	Port	Channel	Configuration Control	Power, VCC	Package	Application Area	Remark
PI3EQX6701C	SATA3/SAS2	One	TX and RX	Pin Strap (EQ, 1dB or 4dB)	1.2V +/-5% 2.5~3.3V +/-5%	TQFN20	Server/Storage, Workstation	Earlier 6G signal redriver
PI3EQX6701D	SATA3/SAS2	One	TX and RX	Pin Strap (EQ, 7dB or 11dB)	1.2V+/-5% 2.5~3.3V +/-5%	TQFN20	Server/Storage, Workstation	Earlier 6G signal redriver
PI3EQX6701E	SATA3/SAS2	One	TX and RX	Pin Strap (EQ, 1dB or 4dB at TX, 7dB or 11dB at RX)	1.2V +/-5% 2.5~3.3V +/-5%	TQFN20	Server/Storage, Workstation	Earlier 6G signal redriver
PI3EQX6801	SATA3/SAS2	One	TX and RX	Pin Strap (EQ, 4/8/16dB)	1.5V +/-5% 3.3V +/-10%	TQFN20	Server/Storage, Workstation	Pin compatible with 6701x
PI2EQX6811	SATA3/SAS2	One	TX and RX	Pin Strap (EQ, 4/8/16dB) I2C/SMBus	1.5V +/-5%	TQFN20	Desktop, Notebook, Docking Server/Storage, Workstation	16 steps EQ at I2C/SMBus
PI3EQX6741ST	SATA3	One	TX and RX	Pin Strap (EQ, 3/6/9dB)	3.3V +/-10%	TQFN20	Desktop, Notebook, Docking	Lower Power consumption
PI3EQX6741SL	SATA3	One	TX and RX	Pin Strap (EQ, 3/6/9dB)	1.05 V +/-5%	TQFN20	Desktop, Notebook, Docking	Lower VCC Lower Power consumption
PI2EQX6812	SATA3/SAS2	Two	TX and RX	I2C/SMBus	1.2V +/-5%	TQFN42	Server/Storage, Workstation	Same Performance as PI2EQX6814
PI2EQX6804-A	SATA3/SAS2	Four	TX and RX	Pin Strap, I2C/SMBus	1.2V +/-5%	LFBGA100	Server/Storage, Workstation	Same Performance (same control at I2C/SMBus for TX or RX Channel)
PI2EQX6864-A	SATA3/SAS2	Four	TX and RX	I2C/SMBus	1.2V +/-5%	TQFN56	Server/Storage, Workstation	
PI2EQX6814	SATA3/SAS2	Four	TX and RX	Pin Strap, I2C/SMBus,	1.2V +/-5%	LFBGA100	Server/Storage, Workstation	Same Performance (Channel by Channel control at I2C/SMBus for TX or RX Channel)
PI2EQX6874	SATA3/SAS2	Four	TX and RX	I2C/SMBus	1.2V +/-5%	TQFN56	Server/Storage, Workstation	

History

Version 1.0	Original Version	May. 13, 2011
Version 1.1	Add product selection table	May.29, 2013