DIODES
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ANP019

Application Note
AP1604 600KHz,1A PWM/PFM Dual Mode Step-down DC/DC Converter

Contents

ANP019 – App. Note 1

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Application Note
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1. AP1604 Specifications

1.1 Features

- Input Voltage Range: 2.2V~5.5V (V_{OUT} type)

- Oscillator Frequency: 600kHz (Typ.)

- Internal Reference: 1.0V (Typ.)

- High Efficiency: 93% (Typ.)

- Stand-by Capability: I_{STB} = 2µA (Typ.)
- Soft-start Time Set-up External Type Possible
- Current Limit and Thermal Shutdown Protection
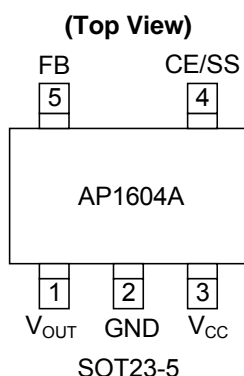- **Pb-Free** Package: SOT23-5

1.2 General Descriptions

The AP1604 series are multi-functional step-down DC/DC converters with built-in speed, low ON resistance drivers. It is possible to deliver more than 800mA output current with external connecting coil, diode and capacitor.

Output voltage is set-up by external resistors (±2.5% accuracy). AP1604 with 600kHz switching frequency can work out with smaller value external component that produces a more compact board. The device switches to and works under PFM mode with light loads. It remains at high efficiency for both light loads and large output currents. There is a soft-start capability by connecting a proper external capacitor. The stand-by current is lower than 2uA when the input voltage is below the stipulated voltage (CE/SS pin is "LOW") and the device is forced to switch off.

1.3 Pin Assignments

(Top View)

```
   FB        CE/SS
   ┌─┐       ┌─┐
   │5│       │4│
   └─┘       └─┘
  ┌─────────────┐
  │   AP1604A   │
  └─────────────┘
   ┌─┐  ┌─┐  ┌─┐
   │1│  │2│  │3│
   └─┘  └─┘  └─┘
  V_OUT  GND  V_CC
```

SOT23-5

1.4 Pin Descriptions

Pin Name	Function
V_{OUT}	Output Voltage
V_{cc}	Input Supply
GND	Ground
CE/SS	Chip Enable / Soft Start
FB	Feedback Pin

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1.5 Block Diagram
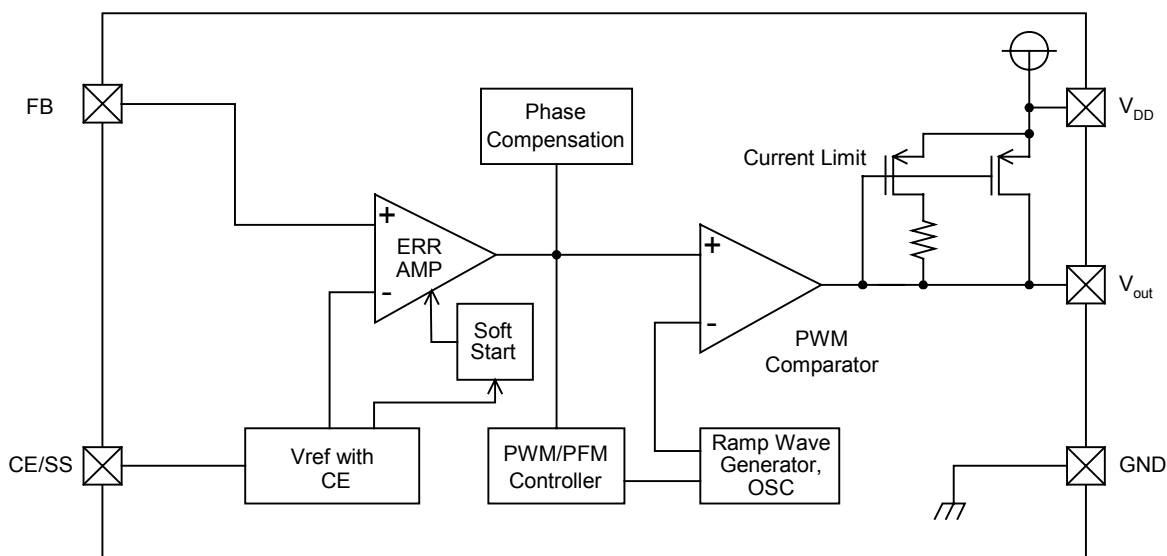
1.6 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
V_{CC}	V_{IN} Pin Voltage	-03 ~ 6.5	V
V_{OUT}	V_{OUT} Pin Voltage	-0.3 ~ V_{IN}+0.3	V
V_{FB}	FB Pin Voltage	-0.3 ~ V_{IN}+0.3	V
$V_{CE/SS}$	CE/SS Pin Voltage	-0.3 ~ V_{IN}+0.3	V
Pd	Continuous Total Power Dissipation	Internal limited	mW
Topr	Operating Ambient Temperature	-25 ~ +80	°C
Tstg	Storage Temperature	-40 ~ +125	°C

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2. Design Procedure (refer to the "Demo Board Schematic")

2.1 Parameter Statement

$V_{IN(max)}$ = Maximum Input Voltage

$V_{IN(min)}$ = Minimum Input Voltage

V_{OUT} = Converter Output Voltage

V_{RIPPLE} = Ripple Voltage (peak to peak), typical value is 1% of the Output Voltage

$I_{LOAD(max)}$ = Maximum Load Current

$I_{LOAD(min)}$ = Minimum Load Current before the circuit becomes discontinuous, typical value is 10% of
the Maximum Load Current

F = Switching Frequency (fixed at a nominal 600KHz)

2.2 Programming Output Voltage

The Output Voltage is programmed by selection of the divider R1 and R2. The designer should use resistors R1 and R2 with ±1% tolerance in order to obtain best accuracy of the Output Voltage. The Output Voltage can be calculated from the following formula: ***Vout = 1.0 x (1 + R1 / R2),*** select a value for R2 between 100K and 200KΩ. The higher resistor values minimize leakage current pickup in the feedback pin.

2.3 Inductor Selection

A. The minimum inductor $L_{(min)}$ can be calculated from the following design formula table:

Calculation	Step-down (buck) Converter
$\dfrac{T_{ON}}{T_{OFF}}$	$\dfrac{(V_{OUT}+V_F)}{V_{IN(min)}-V_{SAT}-V_{OUT}}$
$L_{(min)}$	$\dfrac{[V_{IN(min)}-V_{SAT}-V_{OUT}]\times T_{ON(max)}}{2\times I_{LOAD(min)}}$

V_{SAT} = Internal Driver dropout Voltage of the AP1604 = I_{Load} * 350mΩ

V_F = Forward voltage drop of output rectifier D1 = 0.4V

B. The inductor must be designed so that it does not saturate or significantly saturate at a DC current bias of I_{PK}.

I_{PK} = Peak inductor or switch current = $I_{LOAD(max)} + I_{LOAD(min)}$

2.4 Output Capacitor Selection

A. The Output Capacitor is required to filter the output and provide regulator loop stability. When selecting an Output Capacitor, the important capacitor parameters are the 100kHz Equivalent Series Resistance (ESR), the RMS ripples current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter. The ESR can be calculated from the following formula:

$$ESR = \left(\frac{V_{RIPPLE}}{2 \times I_{LOAD(min)}} \right)$$

B. The ESR of the output capacitor puts a zero in the loop gain which can be used to reduce excess negative phase shift. The phase margin can be system stabilized. If the phase margin is less than 30°, the loop will either oscillate or ring severely. The effects of low and high ESR on phase margin can be illustrated using the following example:

We choose the 22uF output solid tantalum capacitor. The universal usolid tantalum capacitors ESR is 0.3Ω @ 25°C (100kHz), a value that is almost perfectly centered in the stable region **(Figure 1)**. This system corresponds to a phase margin of 74°, which is extremely stable.
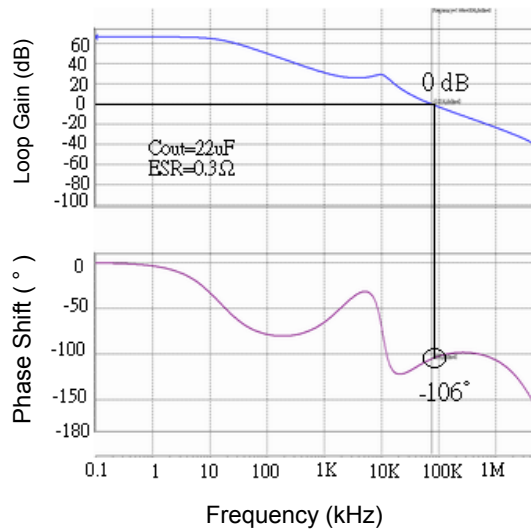

Figure 1. Usolid Tantalum Capacitor of ESR Causes Loop

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We change conditions and assume the ESR of the 22uF output capacitor is increased to 10Ω. This appears to leave a phase margin of 62° (which is stable) **(Figure 2)**, when ESR keeps increasing, the phase margin can shift more and causes the system to be unstable.
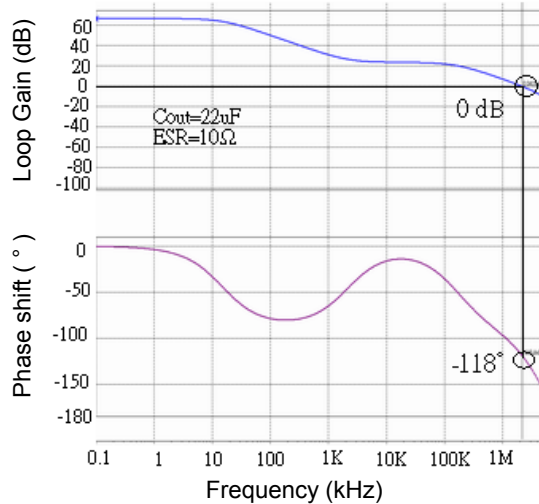

Figure 2. High ESR Causes Unstable Loop

An output capacitor with a very low ESR value can cause the system to be unstable. Generally, a multi-layer Ceramic Capacitor (MLCC) has very low ESR values (<20mΩ). Continuing the example developed in the previous section, we will reduce the ESR of the 22uF Output Capacitor to 10mΩ (Figure 3), the phase margin can be shifted to 2° and it is unstable. In case of using MLCC capacitors, a compensation circuit is required for improving stability. The compensation circuit will add a system zero pole and improve the phase margin, so the system will be extremely stable (refer to 2.5 compensation capacitor selection).
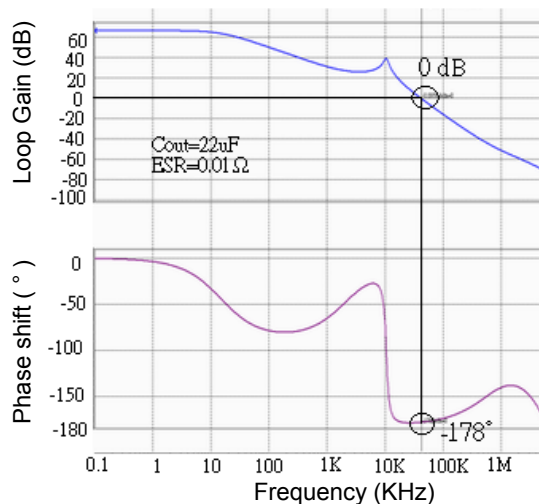

Figure 3. Low ESR Causes Unstable Loop

C. When selecting an output capacitor for AP1604, a solid tantalum capacitor is usually the best choice. It is extremely stable on AP1604.

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2.5 Compensation Capacitor Selection

The Compensation Capacitors for increasing the phase margin provide additional stability. It is required if the output capacitor is MLCC, but not for solid tantalum, because the phase margin is perfect (about 70°) on this condition **(**Figure 4). Refer to the MLCC model circuit in 4.0.4 Demo Board Schematic, a 47pF capacitor C4 in parallel with the in series RB and CB are added in between V_{out} and FB for compensation purposes. The optimum values for CB and RB are 47pF and 500K~1MΩ, respectively.
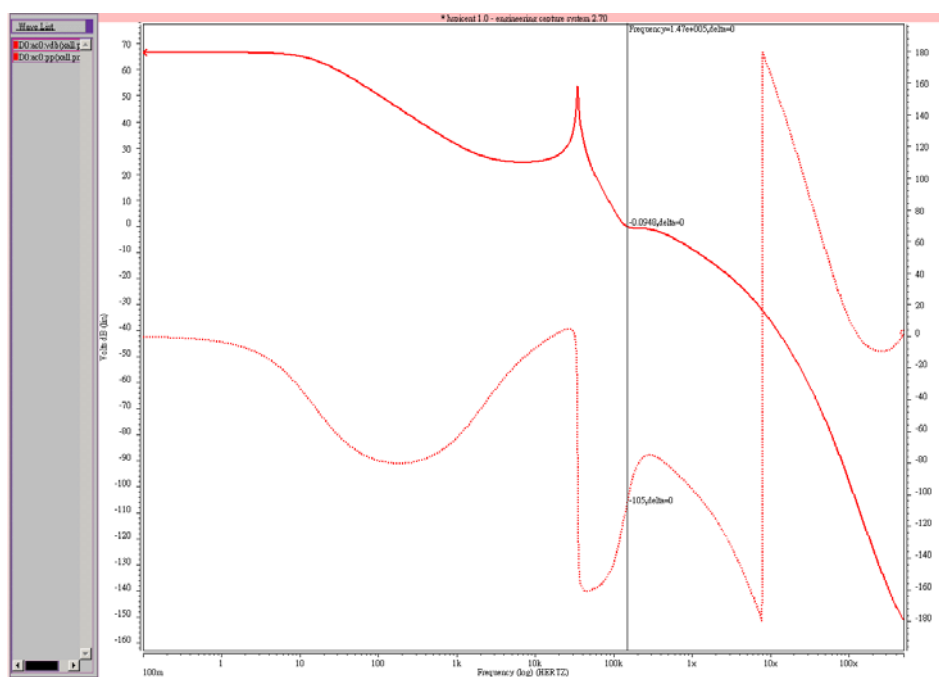

Figure 4. The addition of RB and CB Compensation Makes Loop stable

2.6 Output Rectifier Selection

A. The current of output rectifier D1 must be greater than the peak switch current I_{PK}. The reverse voltage of the output rectifier D1 should be at least 1.25 times of the maximum input voltage.

B. The output rectifier D1 must be fast (short reverse recovery time) and is located close to the AP1604 using short leads and short printed circuit traces. Because of the fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency. It should be the first choice, especially in low output voltage applications.

2.7 Input Capacitor Selection

A. The RMS current rating of the input capacitor can be calculated from the following formula table. The capacitor manufacturer's datasheet must be checked to assure that this current rating is not exceeded.

Calculation	Step-down (buck) Converter
δ	$T_{on}/(T_{on}+T_{off})$
I_{PK}	$I_{LOAD(max)} + I_{LOAD(min)}$
I_m	$I_{LOAD(max)} - I_{LOAD(min)}$
ΔI_L	$2 \times I_{LOAD(min)}$
$I_{IN(rms)}$	$\sqrt{\delta \times \left[\left(I_{PK} \times I_m \right) + \frac{1}{3} \left(\Delta I_L \right)^2 \right]}$

B. This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times of the maximum input voltage.

3. Design Example

3.1 Summary of Target Specifications

Input Power	$V_{IN(max)}$ = +5.5V; $V_{IN(min)}$ = +2.5V
Converter Output Power	V_{OUT} = +2V; $I_{LOAD(max)}$ = 1A; $I_{LOAD(min)}$ = 0.1A
Output Ripple Voltage	$V_{RIPPLE} \leq$ 50 mV peak-to-peak
Efficiency	85% minimum at full load.
Switching Frequency	f = 600kHz ± 15 %

3.2   Calculating and Components Selection

Calculation Formula	Select Condition	Component spec.
$V_{out} = V_{ref} \times ((R1/R2) + 1)$	$100K\Omega \le R2 \le 200K\Omega$	R1 = 100KΩ; R2 = 100KΩ
$$L_{(min)} \ge \frac{\left[V_{IN(min)} - V_{SAT} - V_{OUT} \right] \times T_{ON(max)}}{2 \times I_{LOAD(min)}}$$ $$I_{PK} = I_{LOAD(max)} + I_{LOAD(min)}$$	$L_{(min)} \ge 6.6UH$ $I_{rms} \ge I_{PK} = 1.1A$	Select L = 10uH / 1.2A
$$ESR = \left(\frac{V_{RIPPLE}}{2 \times I_{LOAD(min)}} \right)$$ $$V_{WVDC} \ge 1.5 \times V_{OUT}$$	$200\ m\Omega \le ESR \le 10\Omega$ $V_{WVDC} \ge 3V$	Select C5 from "Viking Tech" 68uF/6.3V*1pcs
$$V_{RRM} \ge 1.25 \times V_{IN(max)}$$ $$I_{PK} = I_{LOAD(max)} + I_{LOAD(min)}$$	$V_{RRM} \ge 6.875V$ $I_{PK} = 1.1A$	Select D1 = 40V/2A
$$I_{IN(rms)} = \sqrt{\delta \times \left[\left(I_{PK} \times I_m \right) + \frac{1}{3} \left(\Delta I_L \right)^2 \right]}$$ $$V_{WVDC} \ge 1.5 \times V_{IN(max)}$$	$I_{ripple} \ge I_{IN(rms)} = 1A$ $V_{WVDC} \ge 8.25V$	Select C1 from "Viking Tech" 68uF/16V*1pcs

3.3 Demo Board Efficiency Calculation

V_{cc} (V)	I_{cc} (mA)	V_{out} (V)	I_{out} (mA)	Efficiency (%)
3.301	6.6	1.810	10	83.06
3.306	60.9	1.807	100	89.73
3.305	122.3	1.807	200	89.39
3.303	186.2	1.808	300	88.17
3.302	254	1.809	400	86.28
3.304	322	1.810	500	85.07
3.3	395	1.810	600	83.31
3.303	469	1.810	700	81.79
5.001	7.74	3.183	10	82.22
5.002	69	3.168	100	91.77
4.999	136	3.154	200	92.78
5.005	204	3.156	300	92.73
5.001	275	3.160	400	91.89
5.005	347	3.164	500	91.08
5.001	420	3.166	600	90.44
5.007	495	3.166	700	89.42

4. Hardware

4.1 Introduction

This application note discusses simple ways to select all necessary components to implement a step-down (BUCK) DC/DC Converter and gives a design example. In this example, the AP1604 monolithic IC is used to design a cost-effective and high-efficiency miniature switching buck converter. For more complete information, pin descriptions and specifications for the AP1604 will not be repeated here, please refer to the datasheet when designing or evaluating with the AP1604.
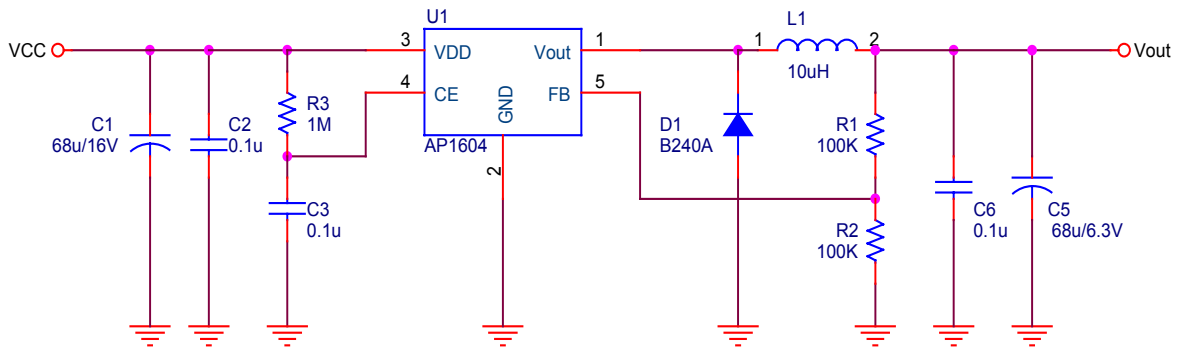
This demonstration board allows the designer to evaluate the performance of the AP1604 series buck converter in a typical application circuit. The user needs only to supply an input voltage and a load. Operation at other voltages and currents may be accomplished by proper component selection and replacement.

4.2 Demo Board Schematic

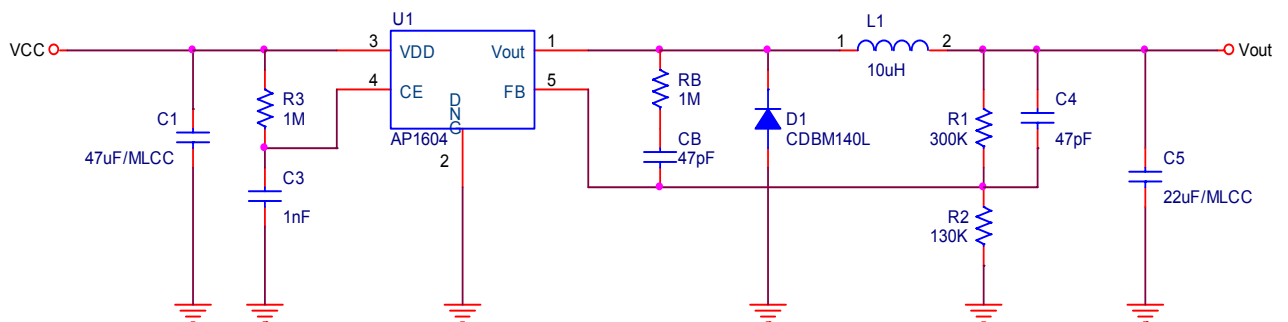### (1) Generality

$$Vout=1.0*(1+R1/R2)$$
$$R2 = 100K\sim200K$$

(2) MLCC model

$$Vout=1.0*(1+R1/R2)$$
$$R2 = 100K\sim200K$$

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4.3 Board of Materials

| Item	Value	Q'ty	Description	MFG/Dist.	Part Number
C1	68uF, 16V	1	Solid Tantalum Capacitor	Viking Tech	
	47uF, 10V	1	MLCC	Viking Tech	
C2	0.1uF, 25V	1	0805 Ceramic SMD Capacitor	Viking Tech	
C3	0.1uF, 25V	1	0805 Ceramic SMD Capacitor	Viking Tech	
	1nF, 25V				
C4	47pF, 25V	1	0805 Ceramic SMD Capacitor	Viking Tech	
C5	68uF, 6.3V	1	Solid Tantalum Capacitor	Viking Tech	
	22uF, 10V	1	MLCC	Viking Tech	
C6	0.1uF, 25V	1	0805 Ceramic SMD Capacitor	Viking Tech	
CB	47pF, 25V	1	0805 Ceramic SMD Capacitor	Viking Tech	
D1	40V, 2A	1	Schottky Diode		B240A
	40V, 1A	1			CDBM140L
L1	10uH, 1.3A	1	SMD Inductance	Wurth Elektronik	WE-TPC 744062100
U1	600kHz, 1A	1	Step-down DC/DC Converter	Anachip	AP1604
R1	100KΩ	1	1% 0805 SMD Resistor	Viking Tech	
	300KΩ				
R2	100KΩ	1	1% 0805 SMD Resistor	Viking Tech	
	130KΩ				
R3	1MΩ	1	1% 0805 SMD Resistor	Viking Tech	
RB	1MΩ	1	1% 0805 SMD Resistor	Viking Tech	

4.4 PC Board Layout
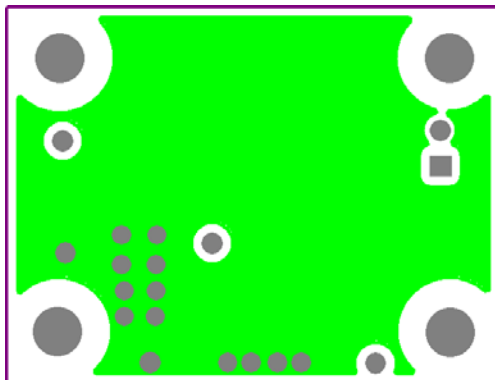
(1) Top View
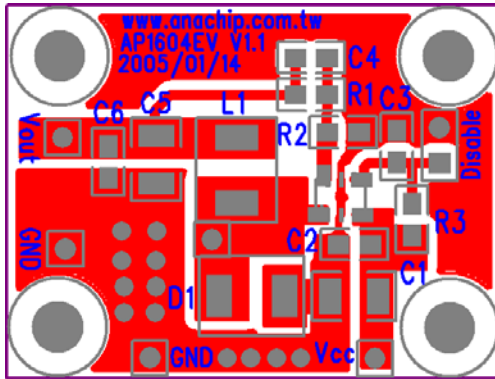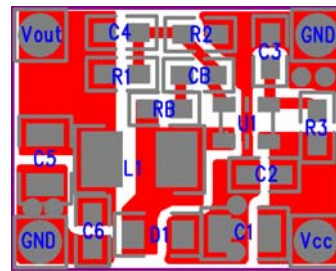
→ **General Size (36*27 mm)** ←   → **Small Size (23*18 mm)**←

(2) Bottom View

→ **General Size (36*27 mm)** ←   → **Small Size (23*18 mm)**←

4.5 PC Board Layout Guide Line

CMOS IC is sensitive to external noise. So the Component selection and PC Board Layout are more important. It is most important that Input Capacitors must be close to IC, as it can reduce ripple noise that affects IC stability. The power GND must connect directly to the input capacitor GND, to allow the system to work in a more stable manner.