**APPLICATION NOTE 1124**
**COMPACT DUAL-PHASE SYNCHRONOUS-RECTIFIED BUCK CONTROLLER**

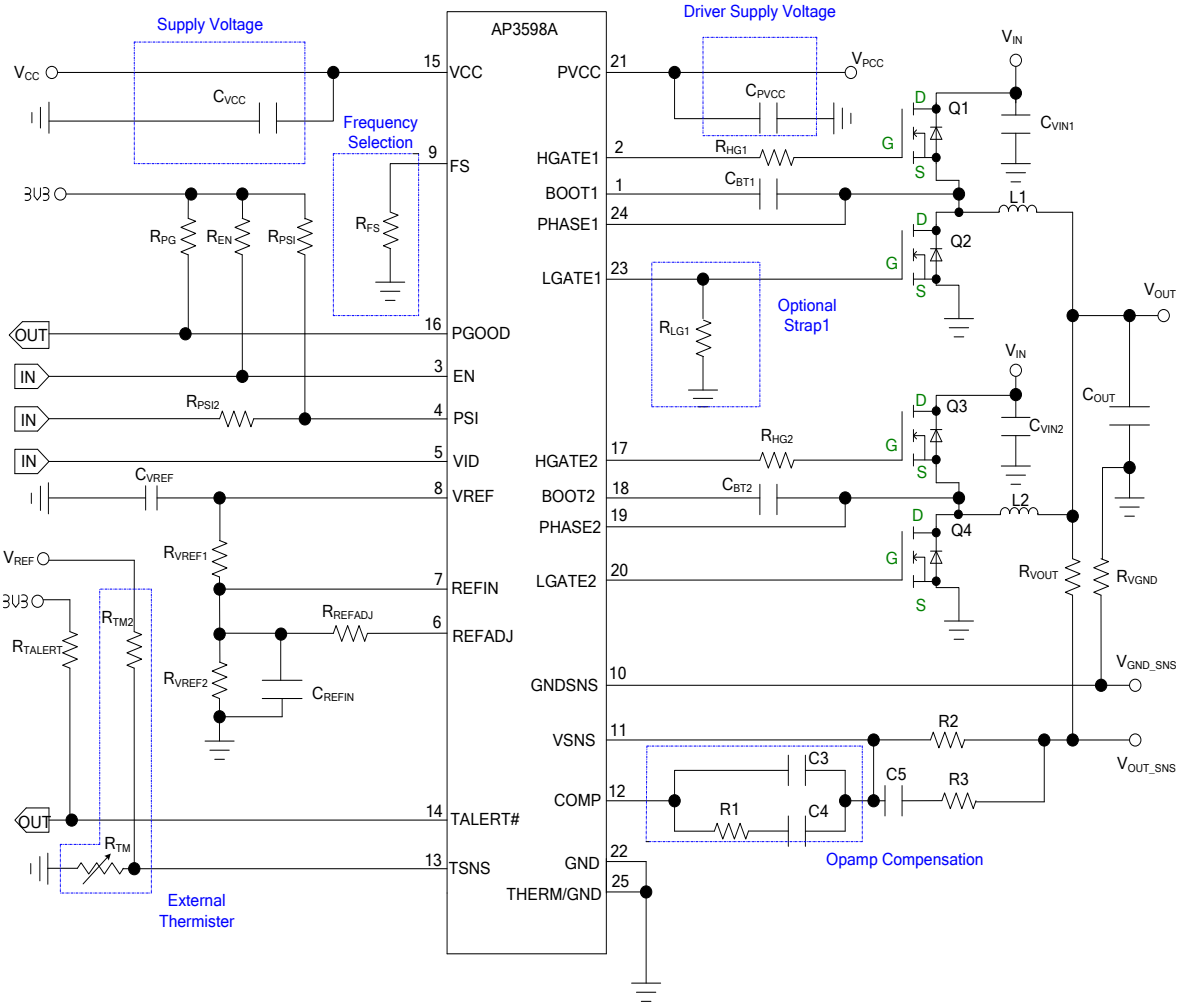
## General Description

The AP3598A is a dual-phase synchronous buck PWM controller with integrated drivers which are optimized for high performance graphic card and computer applications. The IC is capable of delivering up to 60A output current capability and supporting 12V MOSFET drivers with internal bootstrap diodes.

The dynamic output voltage could be implemented by analog method with a switching device and a resistor network. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

The AP3598A provides over current protection, input/output under voltage protection, over voltage protection and over temperature protection. Other features include adjustable soft start, adjustable operation frequency and so on. With aforementioned functions, the IC adopts U-QFN4040-24 package.

## EV Board Schematic



## Application Information

| Component | Value | Unit | Component | Value | Unit | Component | Value | Unit |
|---|---|---|---|---|---|---|---|---|
| $C_{VCC}$ | 10 | µF | $R_{TALERT}$ | 100 | kΩ | C3 | 10 | pF |
| $C_{PVCC}$ | 10 | µF | $R_{TM2}$ | TBD | kΩ | C4 | 2.2 | nF |
| $C_{VIN1}$ | 300 | µF | $R_{TM}$ | TBD | kΩ | C5 | 1.5 | nF |
| $C_{VIN2}$ | 300 | µF | $R_{HG1}$ | 0 | Ω | $C_{OUT}$ | 330*3 | µF |
| $R_{PG}$ | 100 | kΩ | $C_{BT1}$ | 100 | nF | $R_{VOUT}$ | 0 | Ω |
| $R_{EN}$ | 100 | kΩ | $R_{LG1}$ | Note 1 | Ω | $R_{VGND}$ | 0 | Ω |
| $R_{FS}$ | 33 | kΩ | $R_{HG2}$ | 0 | Ω | $C_{REFIN}$ | 0.033 | µF |
| $R_{PSI}$ | 100 | kΩ | $C_{BT2}$ | 100 | nF | Q1 | – | – |
| $R_{PSI2}$ | 0 | kΩ | R1 | 12 | kΩ | Q2 | – | – |
| $C_{VREF}$ | 1 | µF | R2 | 2.2 | kΩ | Q3 | – | – |
| $R_{VREF1}$ | 4.75 | kΩ | R3 | 560 | Ω | Q4 | – | – |
| $R_{VREF2}$ | 4.22 | kΩ | L1 | 0.36 | µH | – | – | – |
| $R_{REFADJ}$ | 6.34 | kΩ | L2 | 0.36 | µH | – | – | – |

Table 1. Component Guide

Note 1: $R_{LG1}$ are OCP setting resisters:
5k for lower OCP threshold, $I_{OCP}$=150mV/$R_{DS(ON)}$
10k for medium OCP threshold, $I_{OCP}$=250mV/$R_{DS(ON)}$
>20k for disabling OCP function

### PWM-VID Dynamic Voltage Control

PWM-VID is a single-wire dynamic voltage control circuit driven by the pulse width modulation method. This circuit reduces the device pin count and enables a wide dynamic voltage range.

The PWM-VID duty cycle determines the variable output voltage at REFIN, as shown in Figure 1. $V_{MIN}$ is the zero percent duty cycle voltage value. $V_{MAX}$ is the one hundred percent duty cycle voltage value. The resolution of each voltage step ($V_{STEP}$) is determined by the number of available steps ($N_{MAX}$) and the selection of the dynamic voltage range ($V_{MAX}$-$V_{MIN}$). N is the number of steps at a specific $V_{OUT}$. N/$N_{MAX}$ ratio is equal to the duty cycle. The dynamic voltage VID frequency ($f_{SWVID}$) is determined by the unit pulse width ($t_U$) and the available step number $N_{MAX}$ ($t_{VID}$ = $t_U$*$N_{MAX}$, $f_{VID}$ = 1/ $t_{VID}$). $t_U$ is programmable.

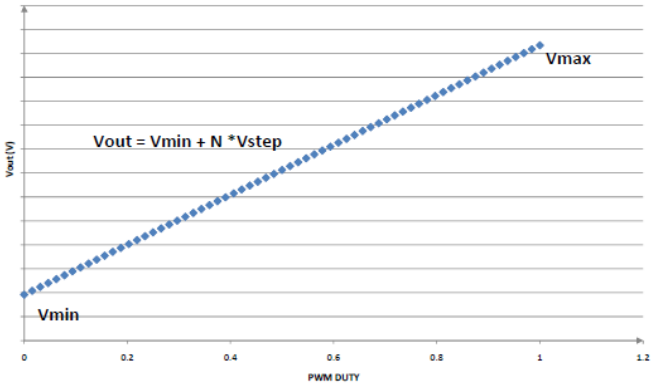



Figure 1. Dynamic Output

## Application Information (Cont.)

$V_{STEP}$, $N_{MAX}$, $V_{MIN}$, and $V_{MAX}$ are variables that determine $V_{OUT}$. $N_{MAX}$ is limited by the unit pulse width and the minimum VID frequency.

The dynamic voltage output could be implemented by the analog method with a switching device and a resistor network. A buffer is used as the switching device to create dynamic output. Resistor network sets the minimum offset voltage.

Figure 2 shows the analog circuit diagram for the PWM-VID dynamic voltage control. The buffer requires a stable, high precision voltage reference ($V_{REF}$) for the linear output. The dynamic range of the circuit is determined by the resistor selection. Resistor $R_{REFADJ}$ and capacitor $C_{REFIN}$ function as a filter for the PWM signal, and will affect the ripple voltage and the slew rate at the output (REFIN) during voltage transitions.

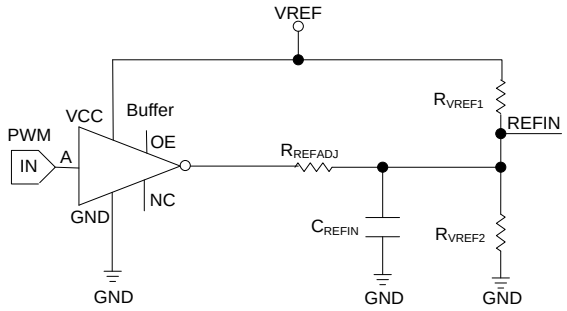



Figure 2. PWM-VID Analog Circuit Diagram

| Spec Description | Output Voltage Equation |
|---|---|
| $N_{MAX}$: Total available voltage step number | – |
| N: The step number of the specific $V_{OUT}$, $N/N_{MAX}$ ratio equals duty cycle | – |
| $V_{MAX}$: The output voltage of REFIN at one hundred percent duty cycle | $V_{REF} \times \frac{R_{VREF2}}{R_{VREF2} + (R_{VREF1} \parallel R_{REFADJ})}$ |
| $V_{MIN}$: The output voltage of REFIN at zero percent duty cycle | $V_{REF} \times \frac{R_{VREF2} \parallel R_{REFADJ}}{R_{VREF1} + (R_{VREF2} \parallel R_{REFADJ})}$ |
| $V_{STEP}$: The resolution of the voltage step | $\frac{V_{MAX} - V_{MIN}}{N_{MAX}}$ |
| $V_{OUT}$: The output voltage at REFIN | $V_{MIN} + N \times V_{STEP}$ |
| $f_{SWVID}$: The dynamic voltage VID frequency | $\frac{1}{t_U \times N_{MAX}}$ |

Table 2. REFIN Dynamic Range

There will be some ripple voltage at REFIN due to the nature of the PWM and filter. The error amplifier at REFIN will be able to tolerate a reasonable amount of Ripple Voltage.

Figure 3 shows a dynamic voltage control circuit with the integrated buffer. This defines the implementation of the VID and REFADJ functions.

## Application Information (Cont.)

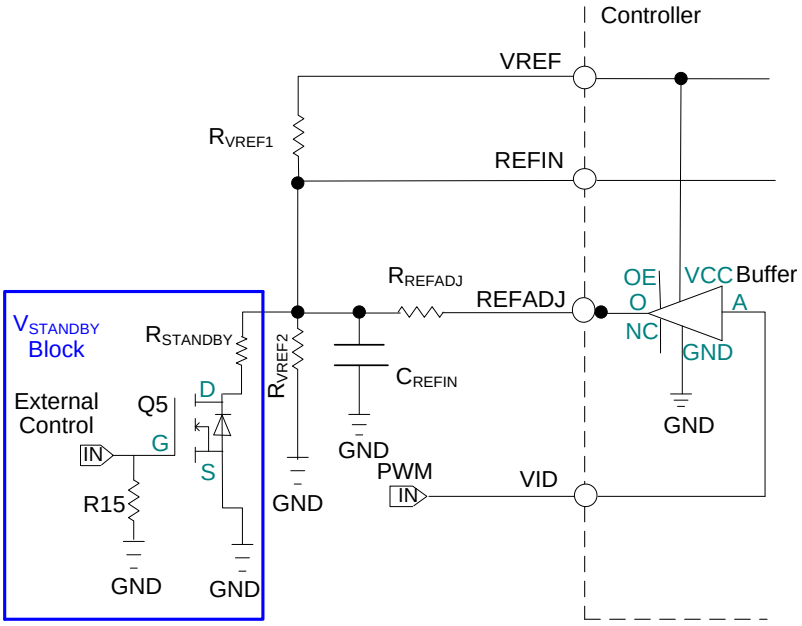



Figure 3. Integrated Buffer Circuit

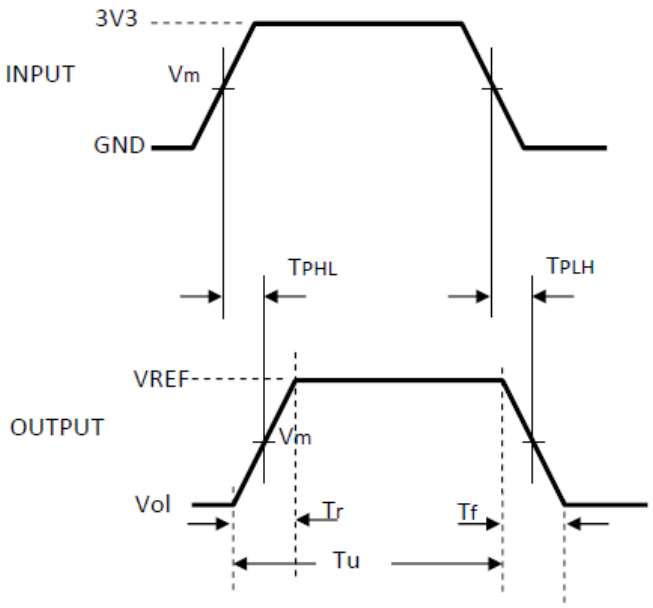



Figure 4. The Behavior of the Buffer

## Application Information (Cont.)

| Parameters | Sym | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Buffer Supply Voltage | – | – | $V_{REF}$ | – | V | – |
| Unit Pulse Width | $t_U$ | – | 27 | – | ns | Configurable |
| Buffer Output Rise Time | $t_R$ | – | 5 | – | ns | – |
| Buffer Output Fall Time | $t_F$ | – | 5 | – | ns | – |
| Rising and Falling Edge Delay | Δt | – | – | 0.5 | ns | $\Delta t=\|t_R-t_F\|$ |
| Propagation Delay | $t_{PD}$ | – | 10 | – | ns | $t_{PD}=t_{PHL}=t_{PLH}$ |
| Propagation Delay Error | $\Delta t_{PD}$ | – | – | 0.5 | ns | $\Delta t_{PD}=t_{PHL}-t_{PLH}$ |
| Upper Resister | $R_{VREF1}$ | – | 4.75 | – | kΩ | – |
| Lower Resister | $R_{VREF2}$ | – | 4.22 | – | kΩ | – |
| Filter Resister | $R_{REFADJ}$ | – | 6.34 | – | kΩ | – |
| Boot Mode Resister | $R_{BOOT}$ | – | – | – | kΩ | Project Specific |
| Standby Mode Resister | $R_{STANDBY}$ | – | 1.07 | – | kΩ | – |
| Filter Capacitor | $C_{REFIN}$ | – | 0.033 | – | μF | – |

Table 3. Electrical Characteristics

Figure 5 contains the details of the timing diagram. After VCC powers up, the controller generates the $V_{REF}$. REFIN settles at $V_{BOOT}$ before the GPU drives the VID pin. After the GPU powers up, $V_{BOOT}$ control will be pulled low by software. At the same time the VID is driven by a PWM signal, moving REFIN into the normal operating mode. When the GPU is going to standby, software will tri-state VID and $V_{BOOT}$ control, and an external control will enable $R_{STANDBY}$.

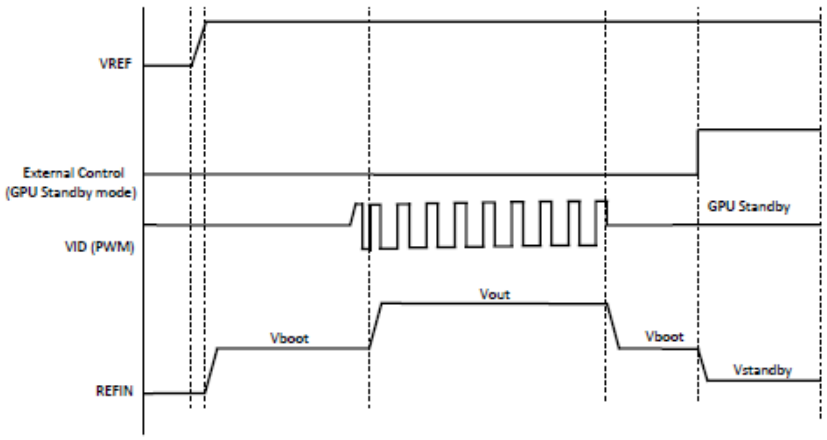



Figure 5. Time Diagram

Standby mode keeps the GPU in a low voltage state (in the range of 0.3V) for the quick recovery. As the GPU steps into the standby mode, the resistor $R_{STANDBY}$ and the switch Q6 (parallel to the $R_{VREF2}$ and $R_{BOOT}$) set the standby voltage. The accuracy of the reference voltage in the standby mode could be reduced from the normal operating mode. Refer to Figure 6 for the illustration of the standby voltage.

## Application Information (Cont.)

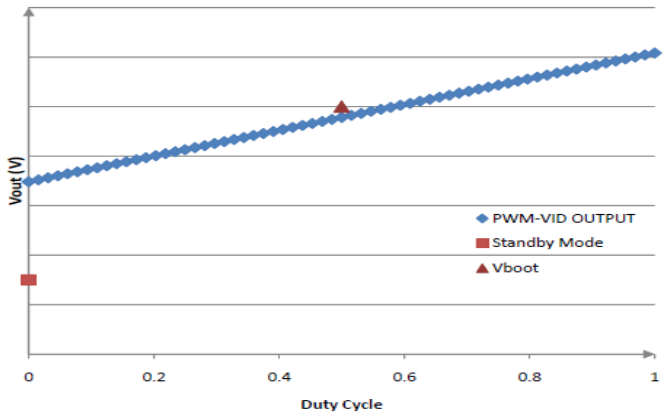



Figure 6. Illustration for Standby Mode and Adjustable $V_{BOOT}$ Setting

### PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, VSNS, and $V_{OUT}$ should be added. The compensation network is shown in Figure 10. The output LC filters consist of the output inductors and output capacitors. For two-phase convertor, when assuming that $V_{IN1} = V_{IN2} = V_{IN}$, L1 = L2 = L, the transfer function of the LC filter is given by:

$$Gain_{LC} = \frac{1 + s \times R_{ESR} \times C_{OUT}}{s^2 \times (1/2) L \times C_{OUT} + s \times R_{ESR} \times C_{OUT} + 1}$$

The poles and zero of the transfer functions are:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{(1/2) L \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

The $f_{LC}$ is the double-pole frequency of the two-phase LC filters, and $f_{ESR}$ is the frequency of the zero introduced by the ESR of the output capacitors.

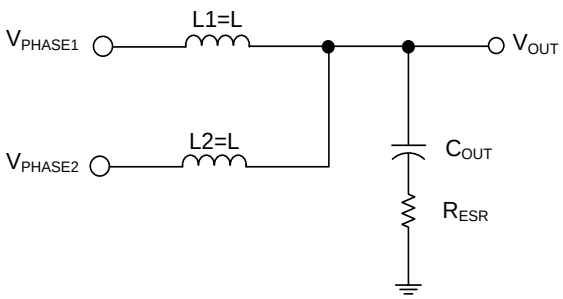



Figure 7. The Output LC Filter

## Application Information (Cont.)

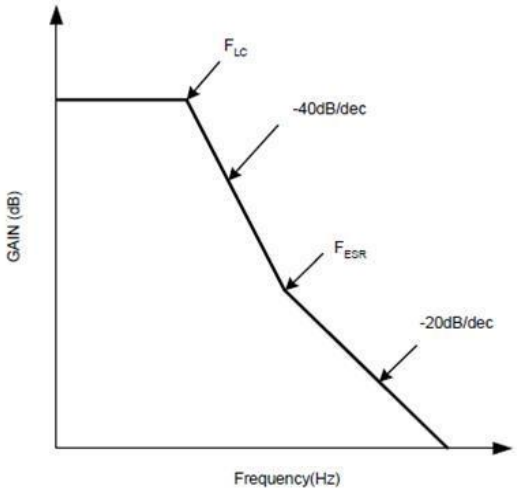



Figure 8. Frequency Response of the LC Filters

The PWM modulator is shown in Figure 9. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$Gain_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

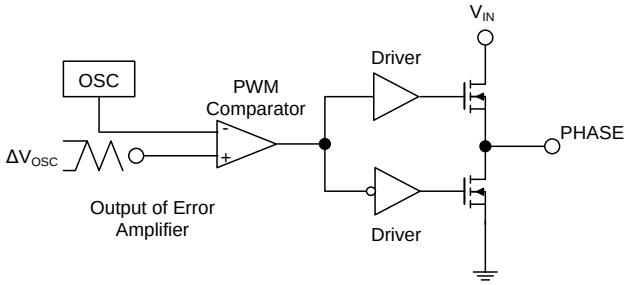



Figure 9. The PWM Modulator

The compensation network is shown in Figure 10. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$Gain_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//(R2+\frac{1}{sC2})}{R1//(R3+\frac{1}{sC3})} = \frac{R1+R3}{R1\times R3\times C1} \times \frac{(s+\frac{1}{R2\times C2})\times\{s+\frac{1}{(R1+R3)\times C3}\}}{s(s+\frac{C1+C2}{R2\times C1\times C2})\times(s+\frac{1}{R3\times C3})}$$

The pole and zero frequencies of the transfer function are:

$$f_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

## Application Information (Cont.)

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C3}$$

$$f_{P1} = \frac{1}{2 \times \pi \times R2 \times (\frac{C1 \times C2}{C1 + C2})}$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

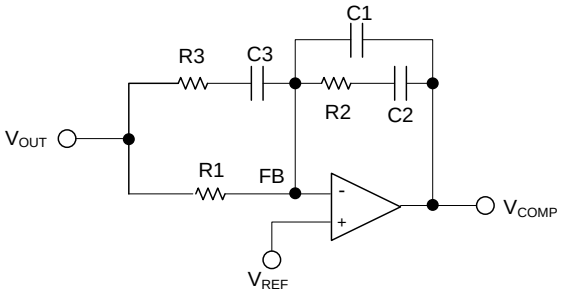



Figure 10. Compensation Network

The closed loop gain of the converter can be written as:

$$Gain_{LC} \times Gain_{PWM} \times Gain_{AMP}$$

Figure 11 shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines will give a compensation similar to the curve plotted. A stable closed loop has a -20dB/decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1kΩ and 5kΩ.

2. Select the desired zero crossover frequency.

$$f_O = (1/5 \sim 1/10) \times f_{SW}$$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{f_O}{f_{LC}} \times R1$$

3. Place the first zero $f_{Z1}$ before the output LC filter double pole frequency $f_{LC}$.

$$f_{Z1} = 0.75 \times f_{LC}$$

Calculate the C2 by the equation:

## Application Information (Cont.)

$$C2 = \frac{1}{2 \times \pi \times R2 \times f_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency $f_{ESR}$:

$$f_{P1} = f_{ESR}$$

Calculate the C1 by the following equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times f_{ESR} - 1}$$

5. Set the second pole $f_{P2}$ at the half of the switching frequency and also set the second zero $f_{Z2}$ at the output LC filter double pole $f_{LC}$. The compensation gain should not exceed the error amplifier open loop gain. Check the compensation gain at $f_{P2}$ with the capabilities of the error amplifier.

$$f_{P2} = 0.5 \times f_{SW}$$
$$f_{Z2} = f_{LC}$$

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{f_{SW}}{2 \times f_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times f_{SW}}$$

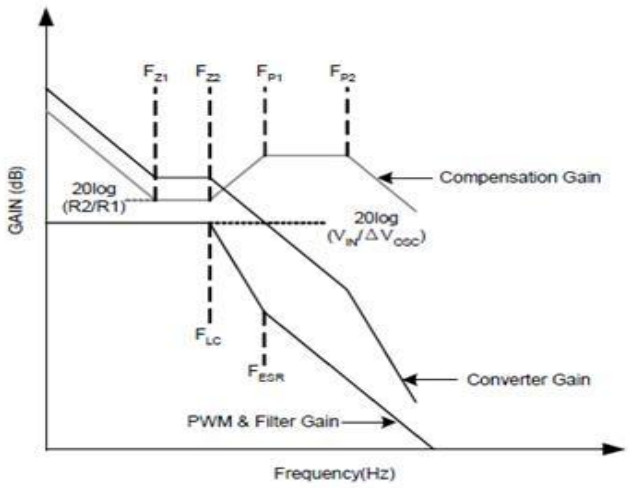



Figure 11. Converter Gain and Frequency

## Application Information (Cont.)

### Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = V_{OUT} / V_{IN}$$

For two-phase converter, the inductor value (L) determines the sum of the two inductor ripple current, $\Delta I_{P-P}$, and affects the load transient response. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - 2V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where $f_{SW}$ is the switching frequency of the regulator.

Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency ($f_{SW}$) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

### Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop $\Delta V_{COUT}$ and ESR voltage drop $\Delta V_{ESR}$ caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must be considered too.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change.

For getting same load transient response, the output capacitance of two-phase converter only needs to be around half of output capacitance of single-phase converter.

Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

## Application Information (Cont.)

### Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. For two-phase converter, the RMS current of the bulk input capacitor is roughly calculated as the following equation:

$$I_{RMS} = \frac{I_{OUT}}{2} \times \sqrt{2D \times (1-2D)}$$

For a through-hole design, several electrolytic capacitors may be needed. For surface mount design, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.

### MOSFET Selection

The AP3598A requires two N-Channel power MOSFETs on each phase. These should be selected based upon $R_{DS(ON)}$, gate supply requirements and thermal management requirements.

In high current applications, the MOSFET power dissipation, package selection, and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss.

The conduction losses are the largest component of power dissipation for both the high-side and the low-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage current transitions and do not adequately model power loss due to the reverse-recovery of the low-side MOSFET body diode. The gate-charge losses are dissipated by AP3598A and don't heat the MOSFETs. However, large gate-charge increases the switching interval $t_{SW}$, which increases the high-side MOSFET switching losses. Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{HIGH-SIDE} = I_{OUT}^2 * (1 + T_C) * R_{DS(ON)} * D + 0.5 * I_{OUT} * V_{IN} * t_{SW} * f_{SW}$$

$$P_{LOW-SIDE} = I_{OUT}^2 * (1 + T_C) * R_{DS(ON)} * (1 - D)$$

Where $I_{OUT}$ is the load current, $T_C$ is the temperature dependency of $R_{DS(ON)}$, $f_{SW}$ is the switching frequency, $t_{SW}$ is the switching interval, D is the duty cycle.

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, $t_{SW}$, is the function of the reverse transfer capacitance $C_{RSS}$. The $(1+T_C)$ term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

## PCB Layout Guidance

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator.

With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike.

Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Figure 12 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Keep the switching nodes (HGATEx, LGATEx, BOOTx, and PHASEx) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.

2. The signals going through theses traces have both high dv/dt and high dI/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (HGATEx and LGATEx) should be short and wide.

3. Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (VIN and PHASEx nodes) can get better heat sinking.

4. For experiment result of accurate current sensing, the current sensing components are suggested to place close to the inductor part. To avoid the noise interference, the current sensing trace should be away from the noisy switching nodes.

5. Decoupling capacitors, the resistor-divider, and the boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor as close as possible to the drain of the high-side MOSFET). The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads.

6. The input capacitor's ground should be close to the grounds of the output capacitors and the low-side MOSFET.

7. Locate the resistor-divider close to the VREF and REFIN pins to minimize the high impedance trace. In addition, VSNS pin traces can't be close to the switching signal traces (HGATEx, LGATEx, BOOTx, and PHASEx).

## PCB Layout Guidance (Cont.)

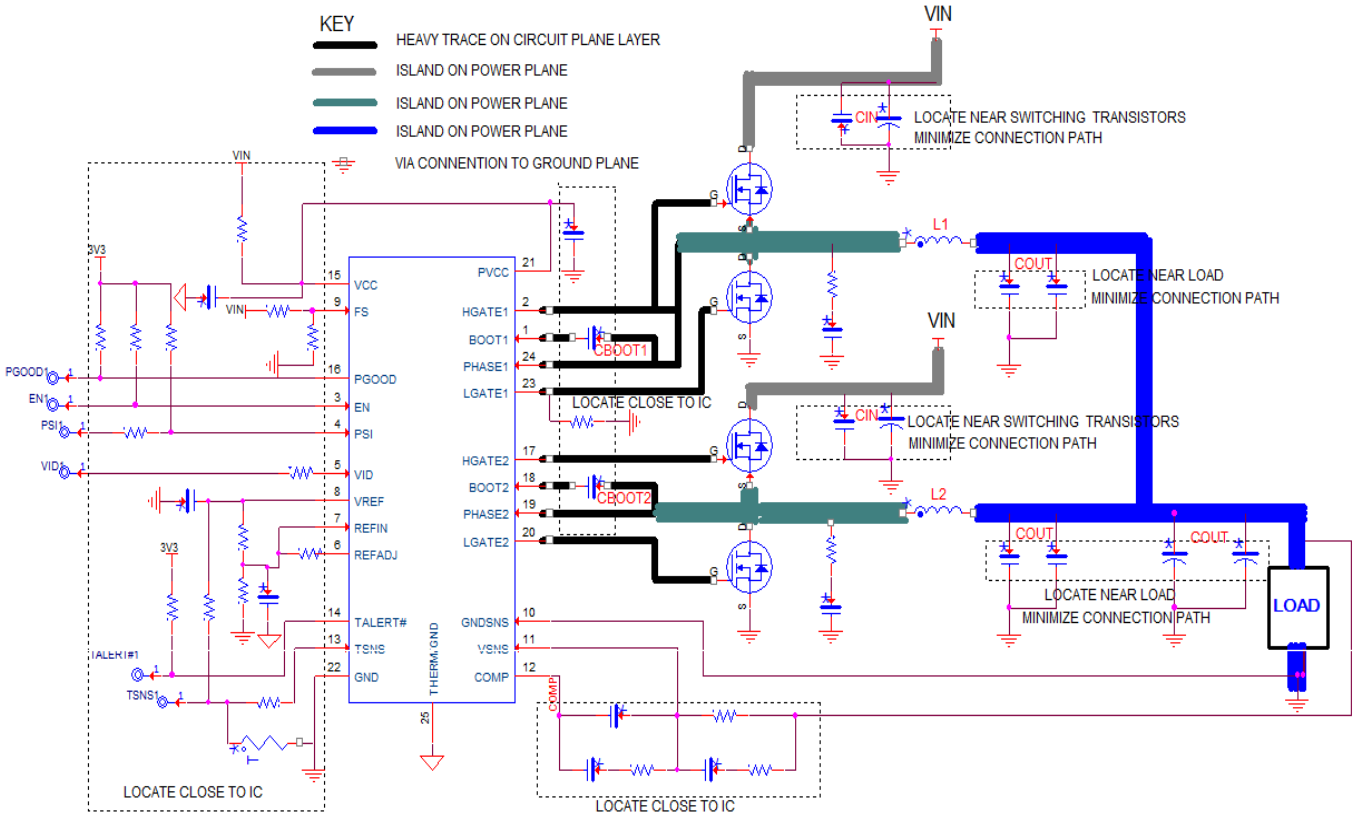
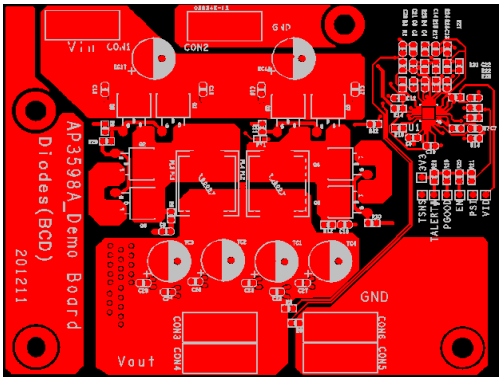
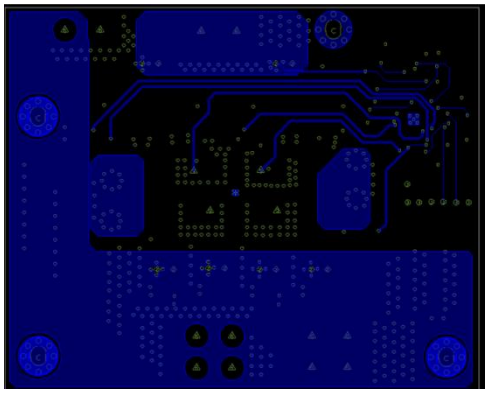



Figure 12. The Layout of AP3598A

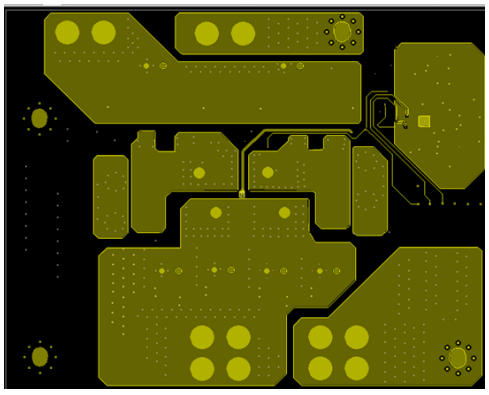
## PCB Layout Example



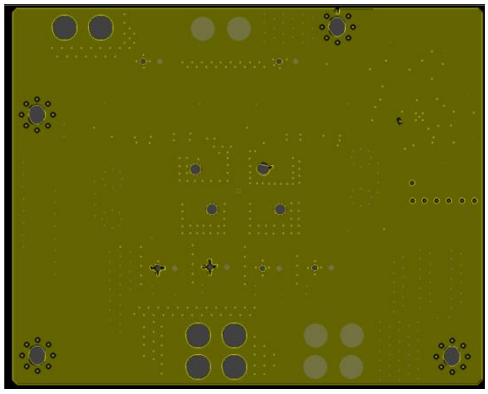

Top Layer



Bottom Layer



VCC Ldayer



Ground Layer

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