Design Guidelines for Off-line AC-DC Power Supply Using BCD PWM Controller AP3103

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1. Introduction

The AP3103 is a low start-up current, current-mode PWM controller with green-mode power-saving operation. The PWM switching frequency at normal operation is externally programmable and is trimmed to a tight range. The dithering of frequency will improve EMI feature. When the load decreases, the frequency will reduce and when at a very low load, the IC will enter the “burst mode” to minimize switching loss. About 20kHz frequency switching is to avoid the audible noise as well as reducing the standby loss.

The AP3103 integrates a lot of functions such as the Lead Edge Blanking (LEB) of the current sensing, internal slope compensation and several protection features that include cycle-by-cycle current limit, VCC Over Voltage Protection (VOVP), Over Temperature Protection (OTP), Over Load Protection (OLP). It is specially designed for off-line AC-DC power supply, such as, LCD monitor, netbook adapter and battery charger applications. It can offer designers a cost effective solution while keeping versatile protection features.

This paper presents a guideline for off-line AC-DC flyback converters using AP3103 and provides an effective way on how to design a SMPS. For a better understanding of AP3103 and its application, this paper also include the introduction to some internal functions, such as saw limiter, and some details need to notice when designing a SMPS using AP3103. The ways on how to improve the system efficiency, and eliminate the audio noise are also recommended in the paper.

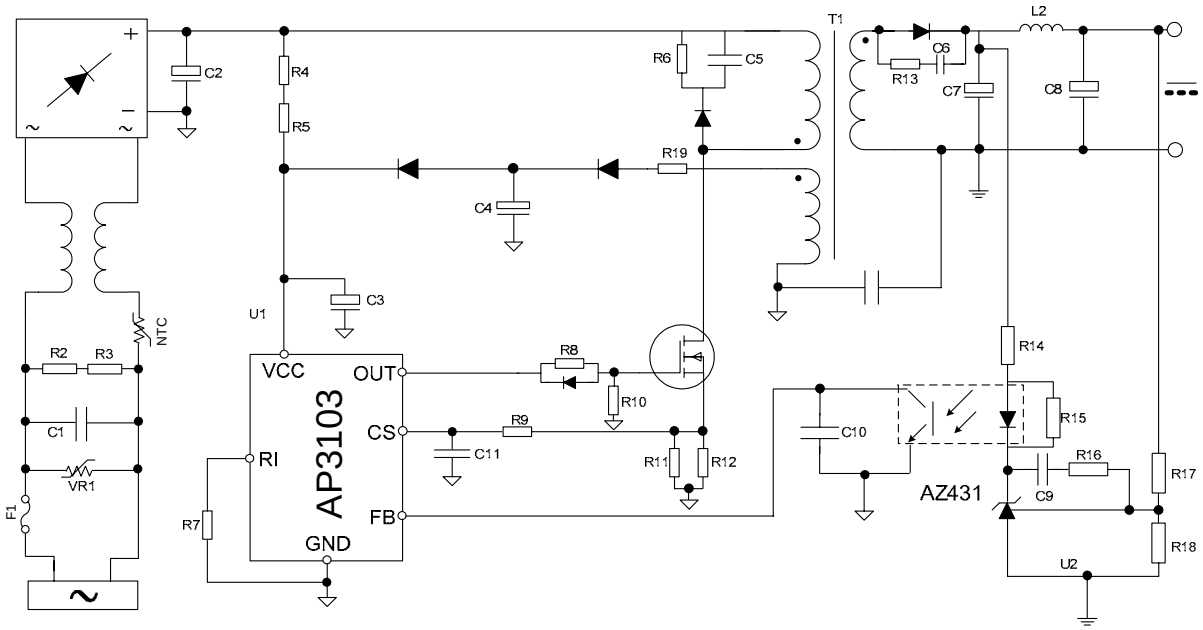

Figure 1. System Schematic Circuit with AP3103

2. Design Procedures

2.1 Defining System Specifications

Before deigning a SMPS, engineers must confirm the system specifications, which are usually proposed by customer or some sector criterions such as, energy star specification for External Power Supply (EPS). Some main specification for a SMPS are listed as below:

-Input Commercial Voltage, V_{AC}.
-Rated Output Power, P_O.
-Rated Output Voltage, V_O.
-System Efficiency, η.
-Output Voltage Ripple, ΔV.

2.2 Selecting DC Bulk Capacitor

The DC bulk capacitor C1 in Figure 1 is used to provide a smooth DC voltage by filtering low-frequency AC ripple voltage. The DC Bulk capacitor, together with the flyback transformer forms a LC filter to filter out the DM noise, and can be expressed as below:

$$C_{BULK} \geq \frac{P_O}{f_{AC} \times (V_{IN\_MAX}^2 - V_{IN\_MIN}^2) \times \eta} \quad \text{..... (1)}$$

Where P_O, f_{AC}, V_{IN_MAX}, V_{IN_MIN} is the rated output power, input commercial voltage, maximum voltage on bulk capacitor, and minimum voltage on bulk capacitor respectively. A simple way is to set C_{BULK} at 2 to 3μF per watt under full AC voltage input and at 1 to 2μF per watt under single AC voltage input.

2.3 Selecting Maximum Switching Duty Cycle (D_{MAX}) and Switching Frequency (f_S)

There are two basic operation modes in flyback converter: Continuous Current Mode (CCM) and Discontinuous Current Mode (DCM). Usually, the CCM and DCM operation modes alternate following the changing of input AC voltage. These two modes have their own advantages and disadvantages. DCM provides a better switching condition for rectifier diode on the secondary side, since the diode operates under zero-current switching. But DCM may cause high RMS current, which increases the conduction loss of the switching and the current stress on the output capacitor. So CCM is recommended under low input voltage or high output current, while DCM is recommended under high voltage or small output current.

Usually, it is recommended to design the system to work under DCM boundary at the highest input voltage for full load condition, and for better hold-up time after shutting off, the maximum duty cycle should be lower than the maximum duty cycle of AP3103.

Switching frequency setting may puzzle the system designers because, high switching frequency can minimize the system size, but, in return, it cause more loss, such as switching loss, core loss, EMI filter loss, etc. So compromise must be achieved among component size, power level, and acceptable loss.

2.4 Calculating Primary-side Inductance (L_M)

For CCM, there are maximum current and minimum current, the relation of which needs to be defined as below before designing, as the relation is uncertain at the beginning.

$$I_{P\_MAX} = k \times I_{P\_MIN} \quad \text{.....(2)}$$

Where I_{P_MIN} is zero for DCM.

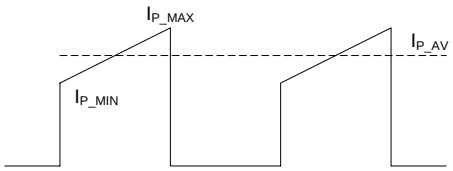

Figure. 2 Primary-side Current

So the primary-side inductance can be expressed as:

$$L_M = \frac{k^2 - 1}{8} \times \frac{V_{DC\_MIN}^2 \times D_{MAX}^2 \times \eta}{P_O \times f_S^{\ 2}} \quad \text{.....(3)}$$

Where V_{DC_MIN} is the minimum input DC voltage.

Once L_M is determined, the actual value of primary-side current can be expressed as below:

$$I_{P\_RMS\_MAX} = \sqrt{D_{MAX} \times (I_{P\_MAX}^2 - \Delta I \times I_{P\_MAX} + \Delta I^2 / 3)}$$

.....(4)

Where,

$$I_{P\_MAX} = \frac{k}{k-1} \times \frac{V_{DC\_MIN} \times D_{MAX}}{L_M \times f_S} \quad \text{.....(5)}$$

$$\Delta I = I_{P\_MAX} - I_{P\_MIN} \quad \text{.....(6)}$$

2.5 Selecting Proper Core and Calculating Winding

Transformer is one of the most important elements in flyback converter. A common method to select the core is to consider the window area (A_Q) and section area (A_E) of the transformer. There are also some practical experience for selecting the core. Some recommended core selection for single output under 65kHz switching frequency is shown in Table 1. For multiple outputs, the size should be properly larger.

Output Power (W)	Ferrite Cores	
	Triple Insulation Wire Construction	Margin Wound Construction
0 to 10	EE16/EI16 EF16 EE19/EI19	EEL16 EF20 EEL19
10 to 20	EE19/EI19 EF20 EFD20 EE22/EI22	EEL19 EF25
20 to 30	EI25 EF25 EI28	EF30 EI30 EER28
30 to 50	EI28 EF30 EI30 EER28	EI30 EER28 EERL28 EER35
50 to 70	EER28L EI35 EER35	EER28L EER35 ETD39
70 to 100	ETD34 EI35 EER35 E21	EER35 ETD39 EER40 E21

Table 1. Ferrite Core Selection Table

Once the core is selected, the primary winding can be expressed as:

$$N_P = \frac{L_M \times I_{P\_MAX}}{B_{MAX} \times A_E} \quad \text{.....(7)}$$

Where B_{MAX} is the maximum flux density. For ferrite core, B_{MAX} is better to be lower than 0.3T. So the secondary winding and auxiliary winding can be expressed as below respectively:

$$N_S = \frac{N_P \times (V_O + V_F) \times (1-D)}{V_{DC\_MIN} \times D} \quad \text{.....(8)}$$

$$N_A = \frac{N_S \times V_{CC}}{V_O} \quad \text{.....(9)}$$

Where V_F is forward voltage of diode in secondary side and V_{CC} is the operating voltage of AP3103.

2.6 Selecting the Power MOSFET

When the switch is off, input DC voltage, together with the output voltage reflected to the primary are imposed on the MOSFET. Ignoring the voltage spike caused by leakage inductance, the voltage on the MOSFET can be expressed as:

$$V_{MOS} = V_{DC\_IN} + N_T \times (V_O + V_F) \quad \text{.....(10)}$$

Where $N_T=N_P/N_S$. Usually, the maximum voltage imposed on the MOSFET is 90% of its rating voltage.

2.7 Selecting the Secondary-side Rectifier Diode

Schottky rectifiers have the merits of low forward-voltage drop and no reverse effect. These features can reduce the loss and improve the overall efficiency, so they are ideal for switching converter application. The main limitation of schottky include the working peak-reverse-voltage rating, the peak-repetitive forward current, and the average forward-current rating of the device. Normally, the forward-voltage drop of diode is proportional to the voltage rating and reverse proportional to average forward current rating. And the maximum junction temperature is also the limitation for system design.

In a flyback topology, the maximum working peak-reverse-voltage can be expressed as below:

$$V_{S\_PEAK} = V_O + \frac{V_{IN\_PEAK}}{N_T} \quad \text{.....(11)}$$

For the forward current rating, efficiency and temperature rising should be considered.

2.8 Selecting the Output Capacitor

The frequency of output ripple is the same to switching frequency. The output capacitor is used to provide enough energy to the load as well as filtering high frequency ripple voltage that have impacts on the ESR of capacitor, output current value, etc. Take the CCM flyback as an example, provided the primary-side inductance is big enough, the equation can be expressed as:

$$\Delta V_O = \Delta V_{O\_ESR} + \Delta V_C$$
$$= I_O \times ESR + \frac{1}{C_O} \times \int_{t_{OFF}} i_{CAP} dt \quad \text{.....(12)}$$

$$\Delta V_C = \frac{I_{O\_MAX} \times D_{MAX}}{C_F \times f_S} \quad \text{..... (13)}$$

From equations above, we can see low ESR type capacitor is required for output capacitor to sustain large RMS ripple current. Moreover, a low-pass LC filter can be added to the converter output to eliminate the requirement of high-performance capacitor as well as benefiting the EMC.

2.9 Selecting the Sampling Resistor and Start-up Resistor and VCC Capacitor

CCM needs a sampling resistor in primary side, for AP3103, the value of sampling resistor may have impacts on OLP, standby power, burst mode point, etc. If too large, it may cause high OLP resulting in system damage, and high burst-mode point resulting in low efficiency under light load, and also high standby power. So the selecting of the sampling resistor should be a trade-off among them.

Start-up resistor R_{ST} (R4, R5 in Figure 1) and VCC capacitor (C3, C4 in Figure 1) are key parameters for starting up, the maximum R_{ST} is determined by formula below:

$$R_{ST\_MAX} = \frac{V_{DC\_IN} - V_{UVLO}}{I_{ST}} \quad \text{.....(14)}$$

Where V_{DC_IN} is input DC voltage, V_{UVLO} is VCC UVLO threshold and I_{ST} is the start-up current.

C3 and C4 should be carefully selected. The turn-on time will be long if C3 is too large, and the system will fail to start if it is too small. The function of C4 is to provide energy for AP3103, if too small, the IC will not have enough energy to sustain the voltage level of VCC over UVLO (off), which may compel the IC to re-start repeatedly all the time.

3. Internal Functions of AP3103

3.1 Saw Limiter

Saw limiter is a compensation method to minimize the difference of OLP power between high input voltage and low input voltage. The power of OLP at high input voltage will be higher than at low input voltage if the OCP voltage is constant. Before the OLP functions, the system is protected by OCP cycle by cycle, and system damage may occur. There are two reasons for this, first, the rising slope of primary-side current is different with the changing of input voltage; Second, the comparator for current limit has delay time from input to output. The current rising rate at high input voltage is higher than that at low input voltage, so the maximum current (I_{P_MAX1}) at high input voltage is higher than the maximum current (I_{P_MAX2}) at low input voltage. If the system works at DCM under OLP, the power under OLP at low input voltage (P_L) and at high input voltage (P_H) can be expressed respectively as below:

$$P_L = \frac{1}{2} L_M I_{P\_MAX1}^2 f_S \quad \text{.....(15)}$$

$$P_H = \frac{1}{2} L_M I_{P\_MAX2}^2 f_S \quad \text{.....(16)}$$

P_H is higher than P_L under OLP because of the delay time of comparator. The reason why CCM need the compensation is the same to that of DCM.

So, saw limiter used in AP3103 can minimize the difference of OLP power to protect the system (Figure 4). The saw limiter begins to function when the switching turn-on time is lower than about 8μs, so the effect of OLP is relative to the winding ratio of the transformer. For example, the input AC voltage of a SMPS is from 90V to 265V, if the winding ratio is too big, the turn-on time will not reach 8 μs until the

AC voltage reaches 150V. That means there will be no compensation available below 150V, resulting in a wider-changing range of OLP power from 90V to 265V. So the winding ratio should be carefully considered when a better OLP performance is required.

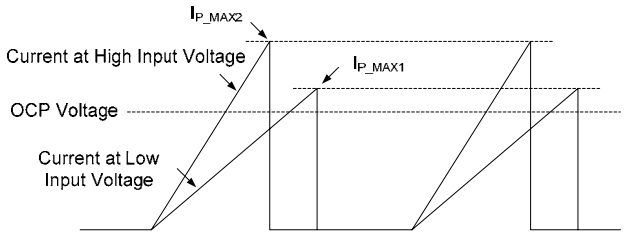

Figure 3. Primary-side Current of DCM under OLP

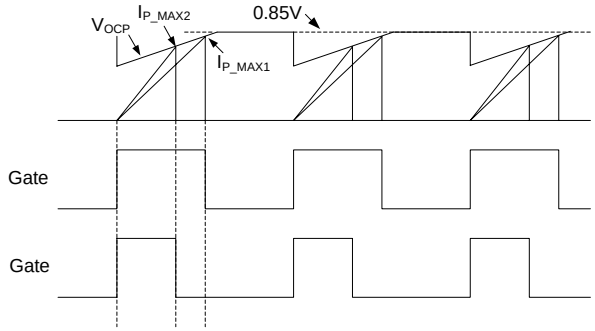

Figure 4. Saw Limiter

3.2 Frequency Fold-back

As we know, the switching loss is significant at light load, and is proportional to the switching frequency. The AP3103 has frequency fold-back function to reduce the switching frequency with the load decreasing to improve the efficiency at light load, and it is also helpful for improving the average efficiency. The minimum frequency should be more than 20kHz to avoid the interference from audio frequency.

Table 2 shows the efficiency test result on a 36W SMPS whose full load is 3A, input AC voltage ranges from 90V to 265V. And the test is done at the input voltage of 265V. The efficiency of AP3103 is higher than the chip without frequency fold-back at light load according to the test result.

Load (A)	AP3103		Chip without Frequency Fold-back	
	Frequency (kHz)	Efficiency (%)	Frequency (kHz)	Efficiency (%)
3	65.8	87.66	65.1	87.69
2.25	62.8	87.01	65.2	86.68
1.5	57.5	86.48	64.9	85.51
0.75	32.8	83.48	65.2	80.51

Table 2. Efficiency Comparison under 265V

4. Audible Noise Consideration

Audible noise is a common issue in SMPS application, usually, it mainly comes from the transformer and snubber capacitor. For the noise caused by transformer, the audible noise is due to unstable loop and burst mode frequency (Figure 5). For unstable loop, there must be audible sound frequency (normally from 2kHz to 20kHz) contained in the loop, the solution for this is to adjust the parameters of the loop to eliminate the sound. For burst mode frequency, which is unavoidable, one way is to use good adhesive to fix each part of the transformer, another way is to minimize the variety of flux density that could be done by reducing the maximum primary-side current under burst mode or minimize the primary-side inductance properly; The noise caused by snubber capacitor is due to the electrostrictive and piezoelectric effect in some ceramic capacitor under alternative electric field intensity. And the solution is to use film or other polypropylene capacitor.

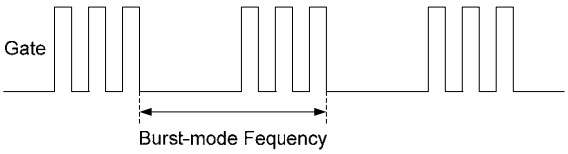

Figure 5. Burst Mode Frequency