AN71

Response time reduction of the ZXCT1009 Current Monitor

Geoffrey Stokes, Systems Engineer, Diodes Incorporated

Introduction and Summary

The transient response of the ZXCT1009 and ZXCt1008 Current Monitors includes a delay time which can vary from 2µs up to about 50µs. This could be a problem in systems which require the delay to be controlled within a narrow window for digital processing. The delay time variation in the basic application circuit relates to the very low bias level of the device, which is optimized for a number of low-power applications. This note describes a simple low-cost method to reduce the delay time to less than 2µs.

For speed improvement, the change to the application circuit amounts to the addition of only 2 low-power resistors. This simple application consists of the current monitor chip plus only 3 resistors including the current sense resistor. The effects of the new circuit on speed, sense voltage tolerance, CMRR and quiescent power consumption are discussed, and are seen to be acceptable in many applications.

Description

The basic application circuit is shown in **Figure 1**. The ZXCT1009 is designed to operate with a very low initial bias current, ranging from 1µA to 15µA, when the differential sense input voltage, V_{S+} - V_{S-}, is zero (or negative). Initially, the step response exhibits a delay time which can be from 2µs up to about 50µs. This depends upon the step sense voltage amplitude. The delay consistently decreases with increasing step amplitude. The bandwidth, and hence the step response time, of the internal amplifier is related to this bias current, which flows mainly between the terminals S+ and OUT.
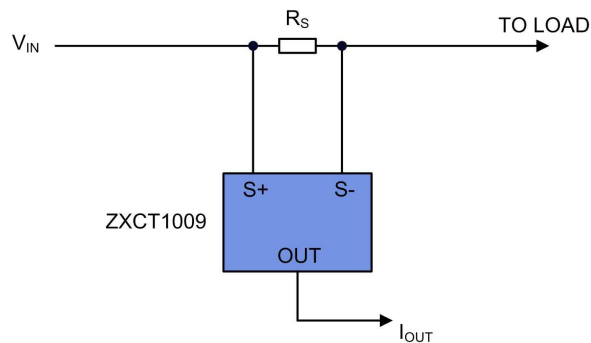

Figure 1: Basic Application Circuit

For speed improvement, a small positive offset is applied to the sense voltage, by adding only 2 low-power resistors R1 and R2, as shown in **Figure 2**. Consequently the bias current is increased, and therefore the bandwidth of the amplifier increases. The bandwidth does not increase indefinitely. When the input has reached a few milli-volts, the response time of the current monitor becomes fairly constant. By adding a small initial offset to the device, we can increase the initial bandwidth to achieve a significant reduction in delay. The performance results will show that a certain small offset will create the conditions to achieve a delay consistently less than 2µs, depending on the drive level required in the application.
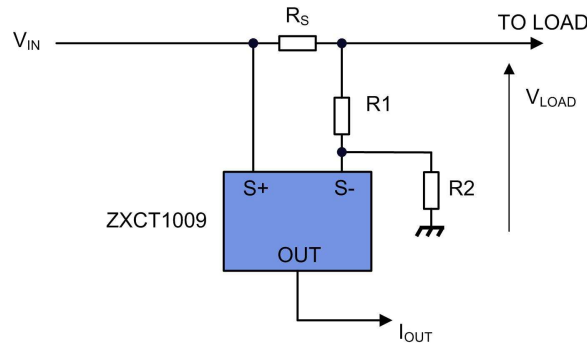
Figure 2: Application Circuit with Improved Speed

In **Figure 2**, R_S is the low-value current sense resistor placed in the high-side path of the power supply. In order to calculate the values of R1 and R2, we need to know the value of offset, V_{OFFSET} which will give the speed improvement required. Later we will show that this offset needs to be about 5mV. First we calculate the offset provided by the potential divider formed by R1 and R2:

$$V_{OFFSET} = V_{LOAD} . R_1 / (R_1 + R_2) + I_{S-} . R_1R_2/(R_1 + R_2) \qquad \textbf{Equation 1}$$

The first term is the wanted offset. The second term represents the unwanted effect of the current I_{S-} into the S- pin of the ZXCT1009. This will affect the result if it is significant compared to the current in the divider. We need a divider current which is at least 100 times larger than I_{S-}. This will ensure that the unwanted offset is 50uV or less. From the data sheet, I_{S-} is 100nA maximum. Therefore the divider current could reasonably be in the region of 10µA to 100µA. Then R1 and R2 form a sufficiently accurate potential divider consuming very little power.

Because V_{OFFSET} will be a few mV, and V_{LOAD} will be a few volts, the potential divider ratio will be of the order of 1000. Therefore R_1 is very much less than R_2. Also we ignore the second term and make the approximation:

$$V_{OFFSET} \approx V_{LOAD} . R_1 / R_2$$

or $\qquad R_2 \approx R_1 . V_{LOAD} / V_{OFFSET}$ $\qquad\qquad$ **Equation 2**

Next we consider a worked example. Following this, we discuss the tolerance, common mode rejection and quiescent current in the new circuit.

Example

For a 5V supply, the current monitor is required to produce an output of 1V to drive the on-board ADC of a microcontroller, when the load current reaches 2.5A. The sense resistor is chosen to be 0.02 ohms to give a voltage drop of 50mV in this condition. This results in a load voltage of 4.95V. For a fast-rising current step, the response time of the current monitor is required to be less than 2µs, measured between the 50% points of the rising current waveform and the current monitor output pin. We assume that the baseline of the current step is zero in this case. Note that we have discovered from measurements that large offsets reduce the response time. Therefore the response time after a current step from say, 2A to 2.5A will be significantly shorter, and the zero-baseline calculation gives us a safe design margin.

The transconductance (G_m) of the ZXCT1009 is 10mS, i.e.,10mA of output current per volt of input sense voltage. Therefore 50mV input gives 500µA of output current. Then the output of the current monitor will drive a 2k resistor connected to ground to give 1V output as desired.

We can see from measured results, described in the performance evaluation below and seen in **Figure 9**, that if the applied sense voltage offset is 5mV or greater, and the sense voltage step is between 25mV and 100mV, the delay between 50% points will be less than 1.5µs. Therefore the delay requirement is satisfied.

We now calculate the values of R1 and R2 to give an offset of approximately 5mV. We shall set the divider current at 50µA. Then R1 = 5mV/50µA = 100 Ω. Then from Equation 2,

$$R2 = 100 \cdot 4.95V/5mV = 9.9 \times 10^4 \text{ ohms}$$

A standard E24 value of 100k gives an offset of 4.95mV. If desired, this known offset can be multiplied by the device gain and subtracted or accounted at the output measuring point.

The final circuit is shown in **Figure 3**.
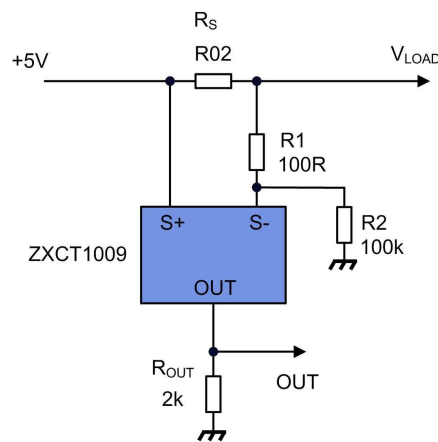
Figure 3: Example Circuit

Effect on Tolerance

The addition of a small input offset causes a similar proportionate offset at the current monitor output. This is predictable according to the tolerance of the resistors R1 and R2. For example, if the resistors have 1% tolerance, the offset tolerance will be up to 2%. Typically the additional input offset applied will be of the order of 5mV, and the ±2% error will be ±0.1mV. The circuit should be designed for a sense voltage which gives sufficient accuracy. From the data sheet we see that, over the useful range, accuracy improves with increasing sense voltage. For a very small sense voltage of 10mV, the output may be 90 to 120µA, i.e., an initial current monitor device error of ± 15%. This is the smallest sense voltage we would expect to see in an application. For a larger sense voltage of 100mV, the device error is ±2.5%. The input error introduced by the new application circuit in that situation is typically 0.1mV which represents 0.1% of the input sense voltage. This is much smaller than the data sheet error and is negligible in the typical application.

CMRR

It will be seen that, because the new offset is proportional to the supply voltage at the load, the common mode rejection ration (CMRR) is affected. The effect is in proportion to the potential divider ratio R1/R2, which is of the order of 1/1000 or -60dB. This effect must be taken into account in the design. However in most cases no special action is required. For example, if the supply voltage varies by 20%, a 5mV injected offset is subject to an error of 1mV. For a sense voltage of 100mV, the output changes by 1%, so the CMRR remains adequate to ensure that the change in the output is smaller than the system error.

Quiescent Current

The added offset naturally increases the quiescent current of the device. This can be calculated from the transconductance G_m = 10mS multiplied by the added offset. For example, an added offset of 5mV gives an increase in output current of 50µA. In addition a further current flows in R1 and R2, equal to V_{OFFSET} /R1 = 50µA for R1=100 ohms. The maximum initial quiescent current of the ZXCT1009 alone is 15µA, so the maximum total in the Example circuit is 50 + 50 + 15 = 115µA. This needs to be considered for battery-powered applications. Indeed the new speed-up circuit may not be suitable in very low average power applications. However the additional power dissipation is low. For example a 5V supply will dissipate 0.575mW or less for zero load current if the current in R2 is 50µA. Clearly there is a compromise between the acceptable error and the dissipation. The current in R2 could be reduced to 10µA with very little effect on the error. In this case, R1 and R2 are 5 times larger (e.g. 470 ohms and 470k respectively) and the total quiescent current is reduced by 40µA to 75µA, and the 5V dissipation is reduced to 0.375mW.

Test Circuit

The pulse test circuit schematic is shown in **Figure 4**. The device under test (DUT) is the ZXCT1009. The MOSFET is used to apply the load. R_T terminates the 50 ohm cable from the pulse generator close to Q1. Input decoupling capacitors are added to minimize the voltage droop at the supply input point, when the load is applied.
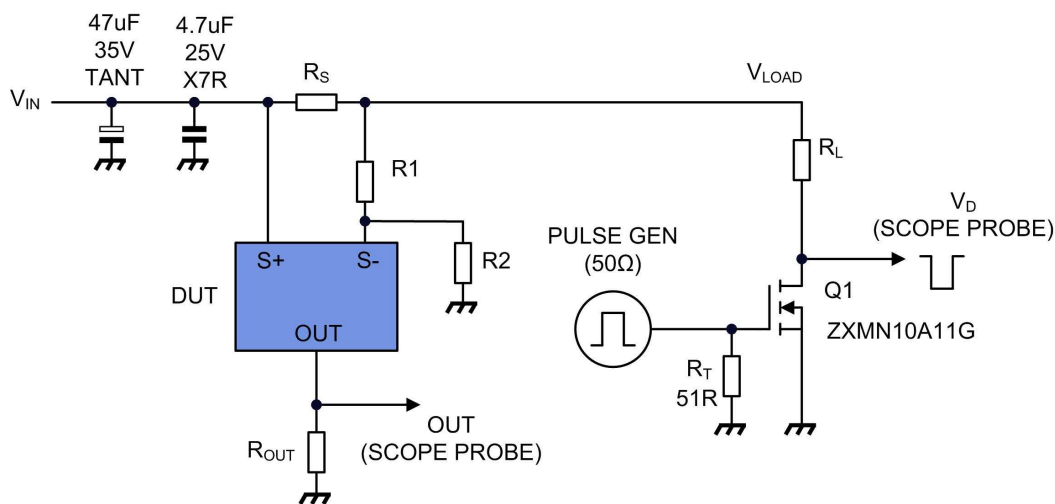
Figure 4: Test Schematic

The test arrangement is pictured in **Figure 5** and uses a modified evaluation circuit board, ZXCT1008EV1. There are solder links for selecting two different sense resistors, in this case, 0.2 ohm and 0.05 ohm.
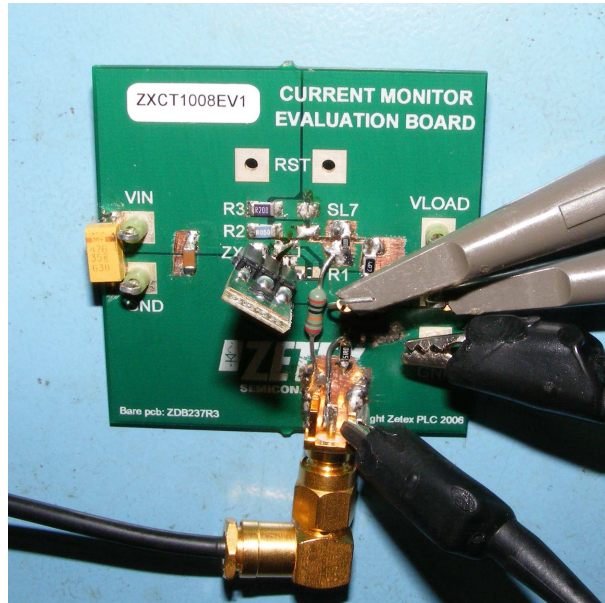
Figure 5: Photo of Test Circuit

Test Description and Results

The pulse generator is set to give a pulse of approximately +6V at the gate of Q1, with a base line of 0V. The pulse width is 50µs and the duty cycle is 1% or less. First the oscilloscope probes were compensated for a square corner response using the 1kHz calibrator provided at the oscilloscope front panel.

For each device measured, a number of calculations were made in an Excel spreadsheet. Note that for all measurements, the following values were fixed: Rout was 2.49k, R1 was 100 ohms and R_L was 9.3 ohms.

The independent parameters varied were:

Input Voltage, Vin, varied from 4V to 18V
Sense resistor, R_S, values 0.05 ohms and 0.2 ohms
Potential Divider resistor, R2, values 200k and 390k. (R1 was fixed as above.)

The measurements made were:

Pulse voltage amplitude at MOSFET drain, V_D
Pulse voltage amplitude at Output, V_{OUT}, in order to check the current monitor scale factor
Delay from falling edge of V_D to 50% point on rising edge of V_{OUT}, **t_D**
Delay from falling edge of V_D to ± 5% settling point of V_{OUT} (settling time), **t_S**

The calculations were:

Sense difference voltage, V_{S+} - V_{S-} (this is the drop across R_S plus the drop across R1)
Offset introduced by R1 and R2

Figure 6 shows a typical delay and settling time measurement.
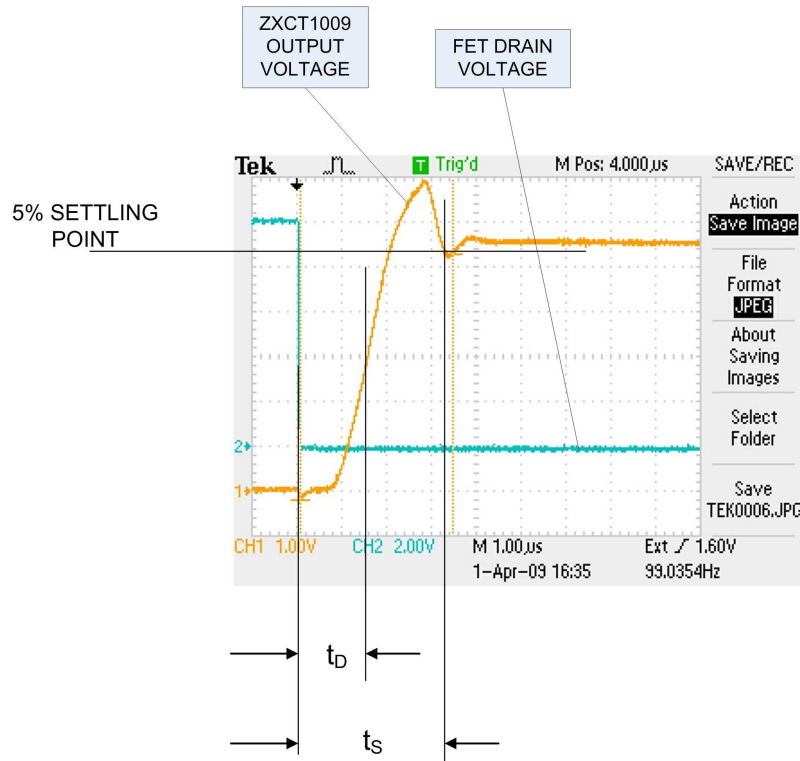
Figure 6: Oscilloscope waveforms

A total of 8 devices were measured, drawn from 5 different production batches.

The results are shown in the following graphs. As previously noted, the input voltage, the sense resistor and the value of R2 were varied and the sense voltage and offset calculated accordingly. **Figures 7** and **8** show the delay time and settling time respectively, with and without offset applied, showing that these times are consistently reduced by the new circuit with offset values at any value between 2.5mV and 9mV.
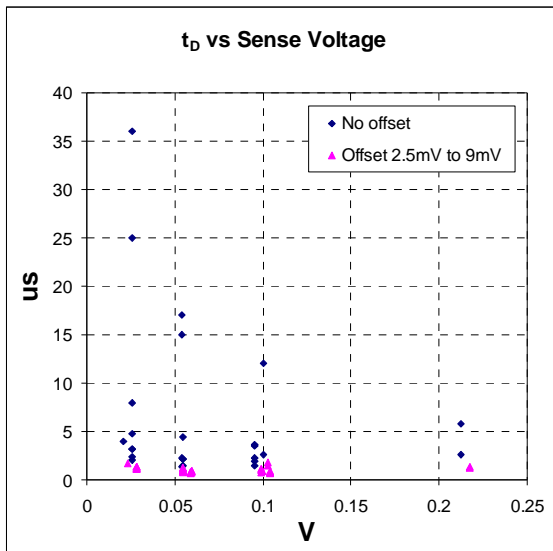
Figure 7: Delay Time
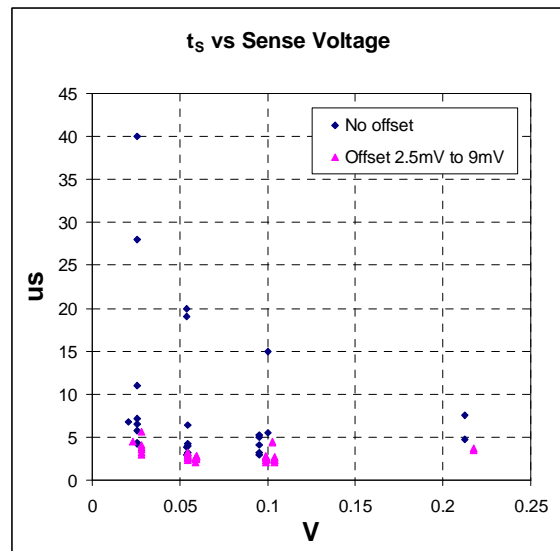
Figure 8: Settling Time

In **Figures 9** and **10** the results are shown on an expanded scale for the measurements, with fixed offset as a parameter. It can be seen that a small offset of 2.5mV to 5mV gives a large reduction in delay and settling times. For an offset of 5mV, the delay time is limited to approximately 1.5µs for sense voltages from 50mV to about 200mV. Similarly the settling time is limited to 4µs. The measurements at 9mV were limited in number, but show a relatively small speed improvement and therefore very little additional benefit compared to 5mV.

The ZXCT1008 was tested separately. The results are not detailed here but the ZXCT1008 gave a very similar improvement in speed versus applied offset to the ZXCT1009.
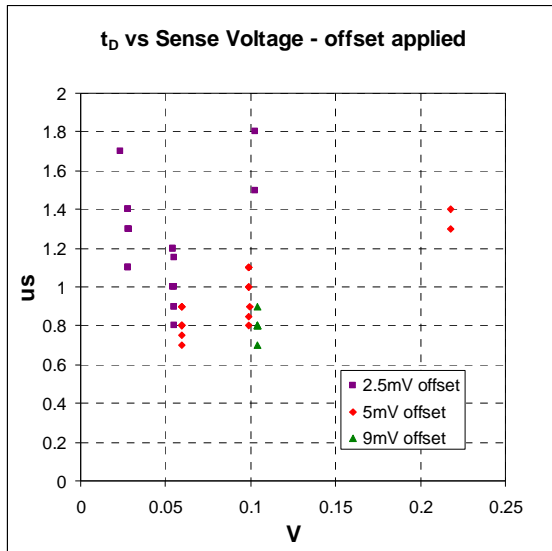
**Figure 9: Delay Time with offset
(expanded scale)**
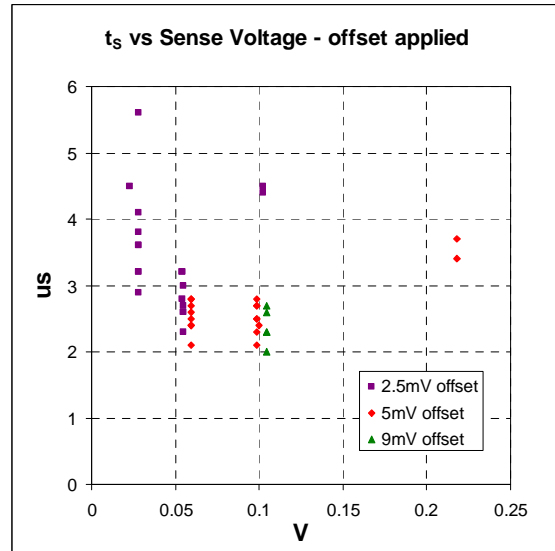
**Figure 10: Settling Time with offset
(expanded scale)**

Conclusion

The new application circuit provides much reduced delay time at very low cost. The circuit introduces an offset to the sense voltage. The offset can easily be set up by the simple addition of two resistors of moderate tolerance. By adding an input offset of 5mV, the delay time can be reliably limited to significantly less than 2µs. The effect of the offset at the output is relatively small, it can be calculated and can be easily compensated in the output detection circuit. The additional error introduced is much less than the initial device error in practical applications. Effects on quiescent power consumption and common mode rejection have been considered and are acceptable in many applications.

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