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High efficiency DC-DC PoL conversion using the DMS3015SSS

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Introduction

This application note describes the benefits of using the DIOFET™ DMS3015SSS in the low-side MOSFET position of synchronous buck point-of-load (PoL) converters. The DIOFET™ products monolithically integrates a power MOSFET and anti-parallel Schottky diode into a single die. This technology reduces both $R_{DS(ON)}$ and anti-parallel diode V_{SD} induced losses, ultimately improving the efficiency of PoL converters. The electrical and thermal performance benefits of the DMS3015SSS are illustrated through comparison with competing solutions in a popular synchronous buck converter.

Low-side MOSFET considerations for synchronous Buck converter

Microprocessor based computing, telecom and industrial systems have become increasingly sophisticated and ever more powerful. This places stringent demands on the power density and dissipation of the PoL converters. The synchronous buck converter is the most popular topology for PoL converters due to its low conduction loss and high switching frequency enabling miniaturization of magnetic component.

The primary building blocks of a synchronous buck converter are, as illustrated in Figure 1: the high-side control MOSFETs (Q1 and Q3); low-side synchronous MOSFETs (Q2 and Q4); output inductors (L1 and L2) and PWM controller. The PWM controller is selected basedon its ability to supply sufficient current to drive the MOSFETs at high frequency and to provide simple, single feedback loop, voltage mode control with fast transient response. In this example, the PWM IC is a dual-output step down controller that operates from a 3V to 28V input voltage.

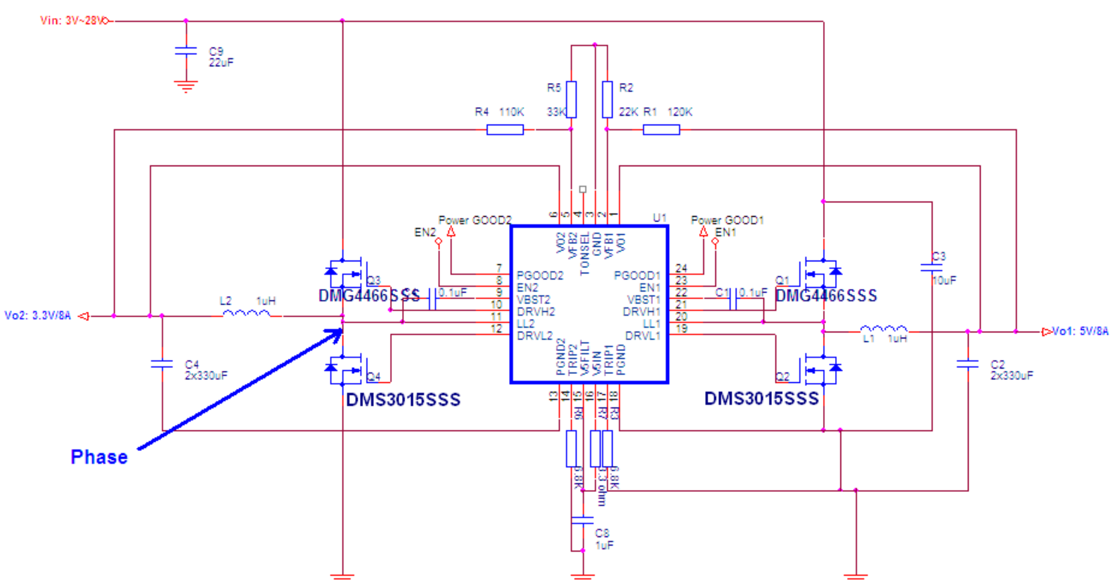


Figure 1. Dual-channel POL converter using DMS3015SSS and DMG4466SSS

The majority of the power losses in a PoL converter are due to losses in the external MOSFETs. These are:

- Conduction losses in low-side synchronous MOSFETs — Q2 and Q4
- Switching losses in high-side MOSFETs — Q1 and Q3
- Body diode conduction in Q2 and Q4
- Reverse-recovery charge losses due to Q2 and Q4 body diode

The efficiency of a PoL converter can be improved if these losses can be mitigated. As the duty cycle of the PWM IC is low then the conduction cycle of the synchronous MOSFET can be as high as 73%. Therefore the biggest improvement in PoL performance will be achieved by selecting a synchronous MOSFET with low $R_{DS(ON)}$, to minimize these conduction losses.

Furthermore, conduction losses can be further reduced by ensuring that the forward voltage drop of the synchronous MOSFET's anti-parallel diode is as low as possible. The anti-parallel diodes, which are normally the body diodes of Q2 and Q4, conduct during the PWM controller's dead time. It is for this reason that external Schottky diodes are often used in parallel with the low-side MOSFET since the V_{SD} of a Schottky is much lower than the intrinsic body diode of the MOSFET.

Schottky diodes also provides softer reverse recovery characteristic, lowering the turn ON losses of Q1 and Q3 at high frequency. However, the disadvantage of such implementation is that the external diode adds capacitance to the circuit, increasing the MOSFET turn OFF switching loss. . Extra care is also needed to minimize layout's parasitic inductance; otherwise the effectiveness of the Schottky will be reduced—if not negated.

DIOFET™ improves POL's efficiency and reliability

The DMS3015SSS has a low leakage Schottky structure interdigitated within the MOSFET cell to create an ideal solution for low voltage, fast switching conversion. It simplifies the design and provides:

- Low V_{SD} is achieved without compromising the $R_{DS(ON)}$ value
- Integrated Schottky diode has lower Q_{RR} and softer reverse recovery characteristic with respect to intrinsic body diode
- 20V gate breakdown voltage to ensure robustness against voltage spike

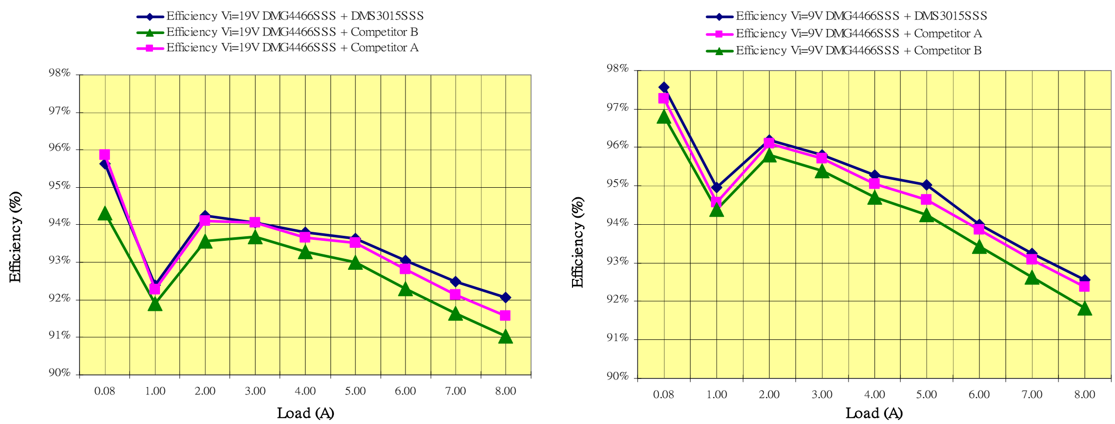
Table 1. comparison of DMS3015SSS electrical parameters against two competing Schottky-MOSFET solutions

Parameters	SYMBOL	Test Condition	DMS3015SSS			Competitor A			Competitor B			UNIT
Drain-Source Voltage	V_{DSS}		30			30			30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250uA$	1	1.5	2.5	1	1.6	3	1.3	1.65	2.5	V
On- Resistance	$R_{DS(ON)}$	$V_{GS}=10V$		8.5	11.9		10	12		11.5	14	mΩ
		$V_{GS}=4.5V$		9.5	14.9		12	15		17	21	
Gate-Source Charge	Qgs	$V_{GS}=10V$, $V_{DS}=15V$		3.40			2.10			2.00		nC
Gate-Drain Charge	Qgd			4.30			3.00			3.90		
Diode Forward Voltage	V_{SD}	$V_{GS}=0V$, $I_S=1A$		0.45	1.00		0.60	0.70		0.43	0.50	V

Performance evaluation

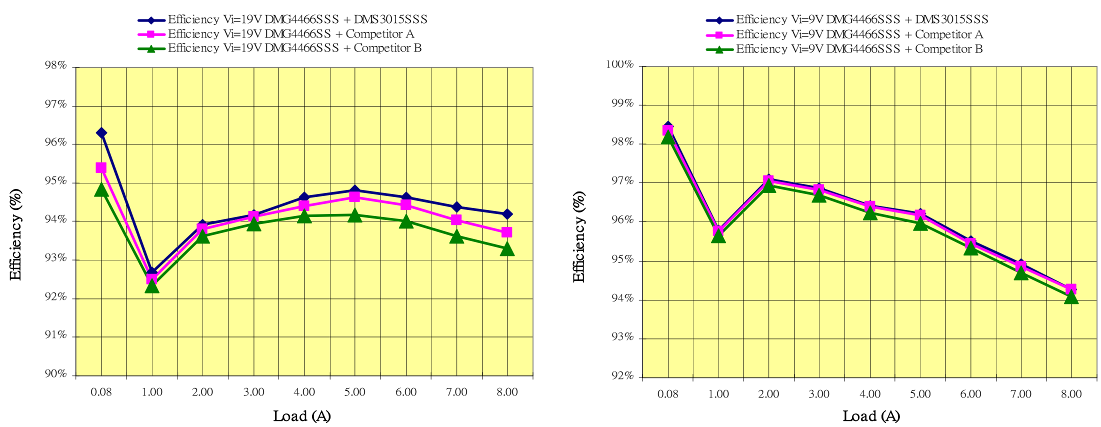
The performance of DMS3015SSS was evaluated against that of competitor 'A' and 'B' in a two output buck converter as shown in figure 1. The low gate charge, fast switching DMG4496SSS was selected as the high side switch (Q1 and Q3) and the DMS3015SSS, competitor A and competitor B were in turn evaluated in the synchronous position (Q2 and Q4). The efficiency of the 3.3V and 5V output voltages were measured whilst the converters output load was then varied from 0.8A to 8A in 1A steps. These measurements were taken under two input voltage conditions: at 19V's, to simulate the input voltage of a notebook PC from the AC Adaptor, and then at 9V to simulate the output voltage from a notebook PC battery pack. The results of these efficiency measurements are shown in Figures 2 and 3.

Figure 2a and 3a demonstrate that under 19V input conditions the DMS3015SSS increases the output of the PoL converter by upto 1% when compared with competitor B and by upto 0.5% when compared against competitor A. Furthermore, under 9V battery conditions the DMS3015SSS increases efficiency by upto 1% when compared against competitor B and is marginally better than competitor A.



(a) **(b)**

Figure 2. 5V output POL converter efficiency at (a) Vin = 19V and (b) Vin = 9V



(a) **(b)**

Figure 3. 3.3V output POL converter efficiency at (a) Vin = 19V and (b) Vin = 9V

Another important circuit consideration is the limitation of shoot-through or cross conduction current in the circuit. At high switching frequencies there is a risk that a temporary shoot-through or cross conduction could happen. This occurs during the switch-on interval of the high-side MOSFET as a very high dV/dt on the phase node (see Figure 1) that induces a gate voltage on the synchronous MOSFETs (Q2 and Q4). If the synchronous MOSFET sees an induced voltage greater than the gate threshold $V_{GS(th)}$, then it could be turned ON whilst the high-side switch is ON. This causes excessive power dissipation in both MOSFETs, and could ultimately lead to devices failure.

Shoot through can be minimized by selecting a synchronous MOSFET that has a low gate capacitance ratio (Q_{gd}/ Q_{gs}). The DMS3015SSS has a gate capacitance ratio of 1.1 which is much lower than that of either of the competing solutions summarized in table 1. Figure 4 illustrates that no shoot-through was observed when the DMS3015SSS was used as the synchronous MOSFET even when the phase node is subjected to rate of change of 600V/ns.

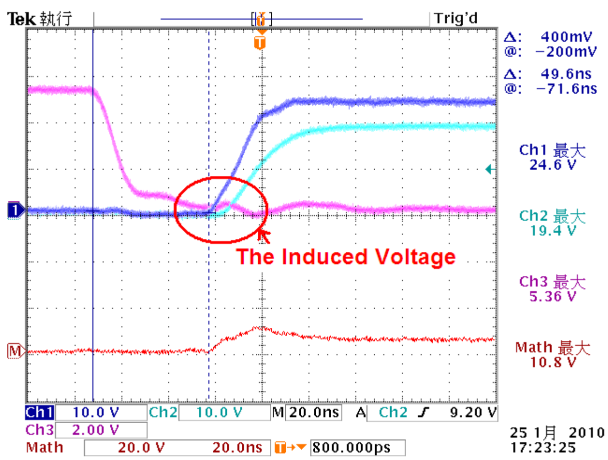
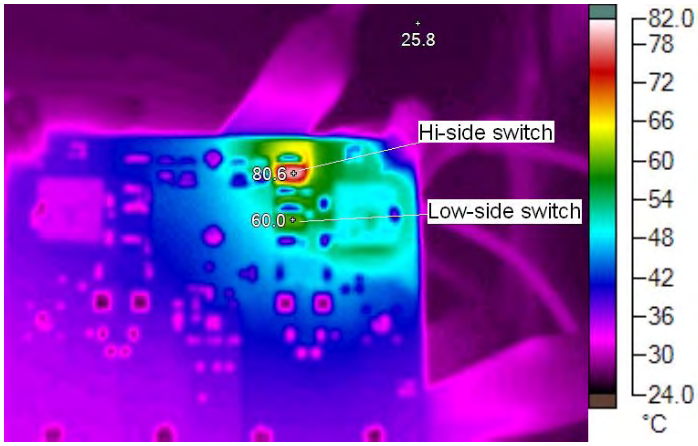


Figure 4 Operating waveforms at the turn-on transition of the high-side switch (Pink: Low-side MOSFET's V_{GS}; Blue: High-side MOSFET's V_{GS}; Cyan: Phase voltage)

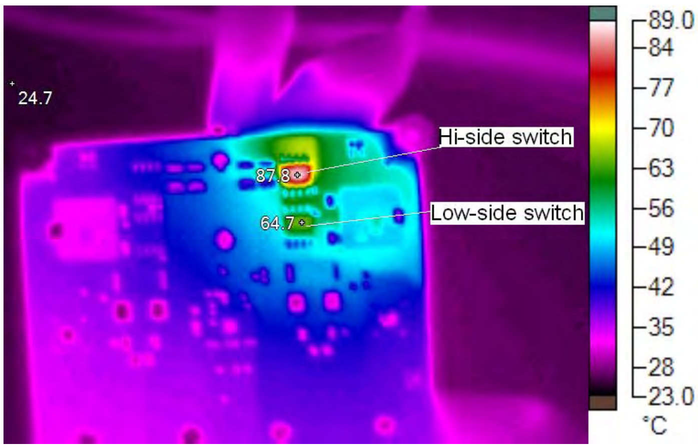
Furthermore, a thermal camera was used to measure the temperature of the high side and synchronous MOSFETs during these efficiency measurements. The PoL evaluation board was convection cooled in 25ºC ambient during the recording of the data. As can be seen in Figure 5 the DMS3015SSS operates at a temperature that is 5% lower than that of either of the competing Schottky-MOSFET solutions.

This lower operating temperature reduces conduction loss in the surrounding components and increases reliability, every 10ºC reduction in the junction temperature of the MOSFET will double the lifetime reliability of the PoL converter.

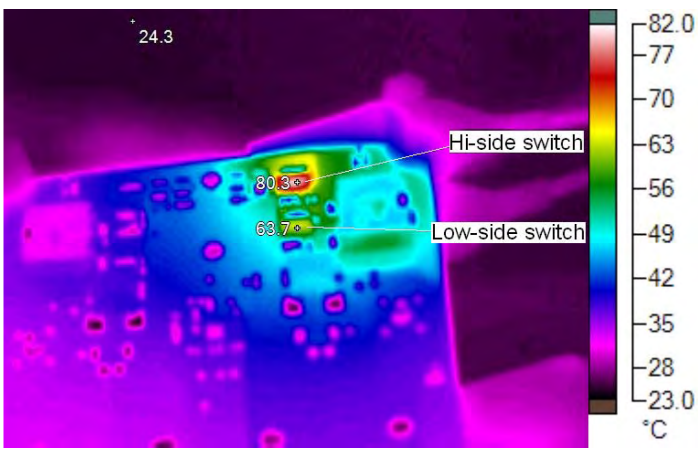
Figure 5. 5V output, 19V input POL converter thermal measurements for (a) DMS3015SSS, (b) Competitor 'A' and (c) Competitor 'B'



(a)



(b)



(c)

Conclusion

It has been demonstrated that the efficiency of the PoL converter can be up to 1 % higher when the DMS3015SSS is used than when competing solutions are used. Furthermore, the DMS3015SS provides this increase in performance whilst operating at a lower temperature, reducing conduction losses in the surrounding components and doubling the reliability of the PoL converter. Furthermore, the DMS3015SSS operates at a higher efficiency enabling the PoL converter to have a higher current handling capability or operate with a lower device junction temperature.