PI3EQXDP1201
PI3EQXDP1201 DP Application Information

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1 Introduction

PI3EQXDP1201 is a DisplayPort 1.2 re-driver for source application. The device is DisplayPort 1.1a and 1.2 compliant. In addition to the function of re-driving dual-mode DisplayPort signals, the device's built-in input equalizer is capable of reducing input signal jitters. PI3EQXDP1201 also provides AUX decoder, which supports link training and can automatically configure its equalization, swing and pre-emphasis levels.

1.1 Equalization, Swing and Pre-emphasis Settings

Equalization, swing and pre-emphasis of PI3EQXDP1201 can be controlled via pins or SMBus. Automatic configuration based on Aux configuration registers can be enabled via pin control. Please refer to PI3EQXDP1201 Demo Board Rev.A User Manual for detailed setting procedures.

1.2 Dual-mode DP Source

PI3EQXDP1201 supports dual-mode DisplayPort inputs and outputs. For PI3EQXDP1201 used in a dual-mode DP source application, AC coupling capacitors are placed between DP source chipset and input main link pins of PI3EQXDP1201, and between output main link pins of PI3EQXDP1201 and a DP output connector.

1.3 AUX Channels

Per DisplayPort Standard Version 1.2, AC coupling capacitor value in the range of 75 – 200nF is required between the DP source and the AUX channel. A 0.1uF AC decoupling capacitor is placed at each of AUX_SRCP and AUX_SRCN pins of PI3EQXDP1201. Source device is also required to pull down AUX+ to GND and pull up AUX- to DP_PWR between the DP connector and AUX channel. A resistor value in the range of 10kΩ to 105kΩ is recommended per DP Standard Version 1.2. A 100kΩ pull-down resistor is placed at AUX_SINKP pin of PI3EQXDP1201. And a 100kΩ pull-up resistor is placed at AUX_SINKN pin. When a DP sink device determines AUX+ and AUX- are being pulled to low and high, respectively, a DP source device is connected.

1.4 Cable Adaptor Detect

A 1MΩ pull-down resistor at CAD_SINK of PI3EQXDP1201 is recommended so as to prevent CAD_SINK from floating when no sink device is attached. If the sink device is HDMI/DVI, CAD_SINK and thus CAD_SRC will be pulled up. This is how source device distinguishes if the sink device is DP or not.

1.5 DDC Channels

If a DP-to-HDMI or DP-to-DVI cable adaptor is attached to the DP output connector in this source application, the dual-mode DP source will be signaled to transmit TMDS through high-speed channels of PI3EQXDP1201 to an HDMI or a DVI sink device. In this case, AUX_SRCP/N pins of PI3EQXDP1201 will be disabled. SCL_DDC and SDA_DDC pins will take action to transmit DDC transaction.

When designing a source application with nVidia or ATI source chipset, external DDC circuitry should be implemented at chipset side in order to pull DDC channels to sufficient high voltage level, which is larger than 0.7VDD per I2C specification. As some source chipsets generate AUX and DDC from the same signal pair, the external DDC circuitry is enabled only if HDMI or DVI sink device is attached. CAD_SRC is thus used to enable the two 2kΩ pull-up resistors for SCL and SDA.

1.6 Power Management

To enhance the flexibility of power management, individual lane of PI3EQXDP1201 can be powered down if input DisplayPort signal is not present or sink device is not attached. Besides, PI3EQXDP1201 offers two power supply modes – 3.3V single power supply or 1.5/3.3V dual power supply. To be convenience, 3.3V single power supply can be selected. For lower power consumption, 1.5V/3.3V dual power supply is more preferable.

ESD protection can also be independently powered down depending on the squelch per lane. ESD performance depends on a variety of test conditions. Please contact Pericom for a detailed ESD test report.

1.7 Layout Design Guideline

Layout especially for high-speed transmission is critical. Please refer to PIxxxx High Speed Layout Guideline for detailed recommendations.

2 Typical Application Circuit

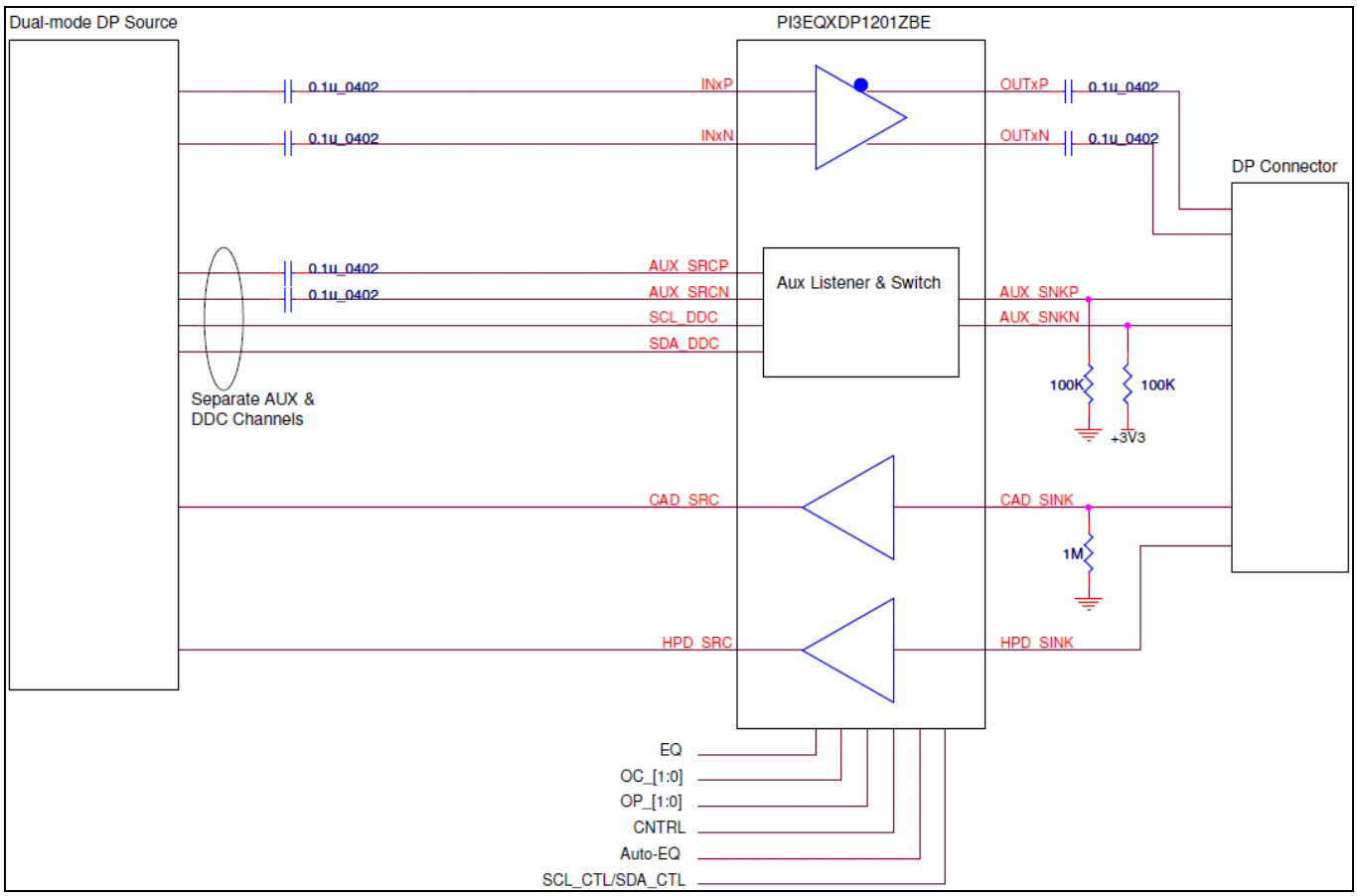

Figure 1: PI3EQXDP1201 Dual-mode DP Source Application Diagram with Separate AUX and DDC Channels from Source

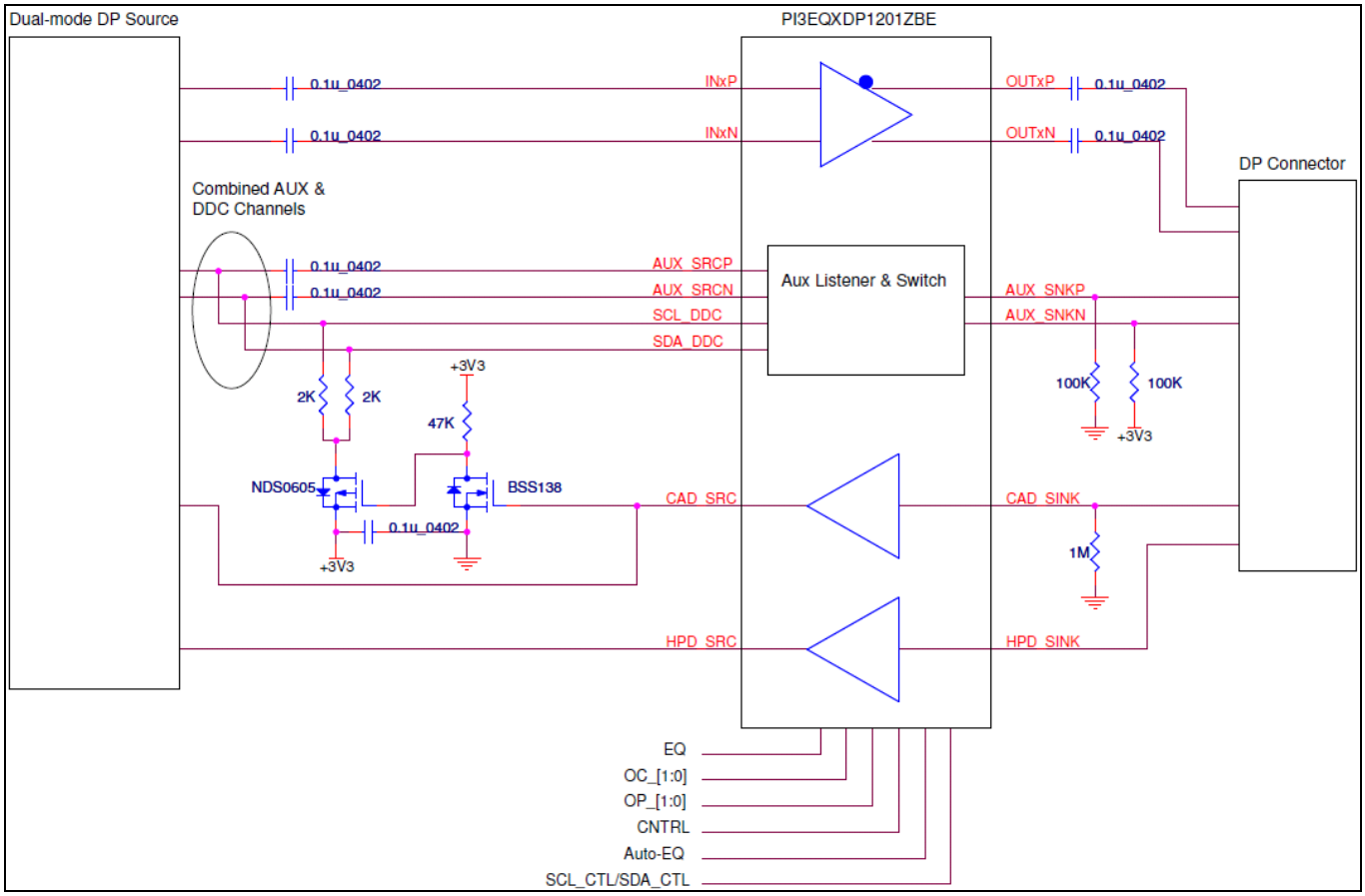

Figure 2: PI3EQXDP1201 Dual-mode DP Source Application Diagram with Combined AUX and DDC Channels from Source

3 Relative References

(1) VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010
(2) VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012
(3) VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009