PI3VDP612-A DP to DP and HDMI Source Application Note

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1. Introduction

Pericom's PI3VDP612-A mux/demux is targeted for next generation digital video signals. This device can be used to connect a DisplayPort™ (DP) source to two independent DP sinks or to connect two DP sources to a single DP display.

Application note explains how to use the PI3VDP612-A to connect to a Dual Mode DP source signal to drive one Dual Mode DP port and one HDMI port on PC source application. Figure 1 illustrates this application.

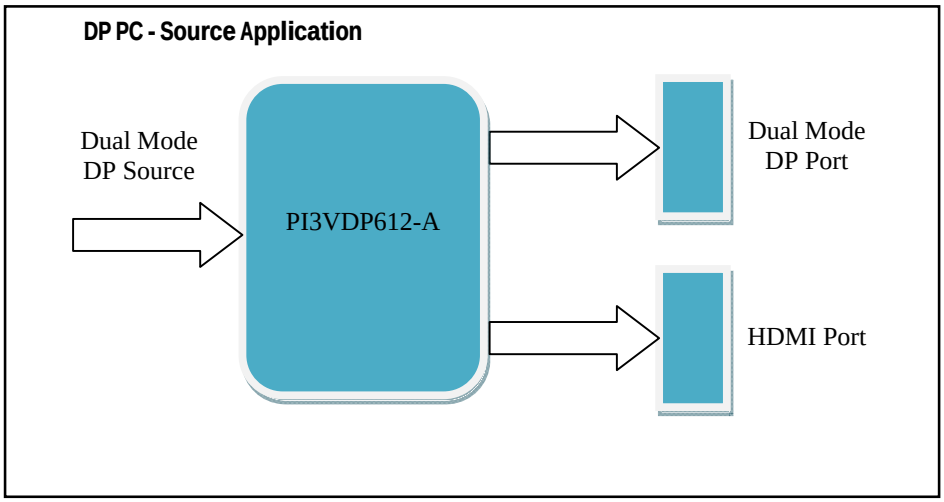

Figure 1: Application Diagram

2. DC Source Application

The system needs to implement the following circuits for the application to work correctly:

(1) **HDMI Signal Level Shifter**: This component is used to transform DP signal level to HDMI signal level. 499Ω pull-down resistor acts as a voltage divider in conjunction with the 50Ω +3.3V pull-up resistor on the HDMI sink device side to give a +3.0V DC offset voltage on the high speed HDMI lanes in order to meet HDMI signal level requirement. NMOS transistor connecting 499Ω resistor to GND is used to isolate the 499Ω connecting to GND when the system is powered down in order to meet HDMI compliance test specification's TMDS-VOFF requirement. Only one NMOS is needed to connect all 8 pieces of 499Ω resistors pull down to GND to save cost and circuit form factor.

(2) **DDC Signal Level Shifter on HDMI port**: This is used to level shift +3.3V interface DDC signal on the Dual Mode DP Source side to +5V interface on the HDMI port side using a single NMOS level shifter

(3) **HPD Signal Level Shifter on HDMI port:** This is used to level shift +3.3V interface HPD signal on the Dual Mode DP Source side to +5V interface on the HDMI port side using a single NMOS level shifter

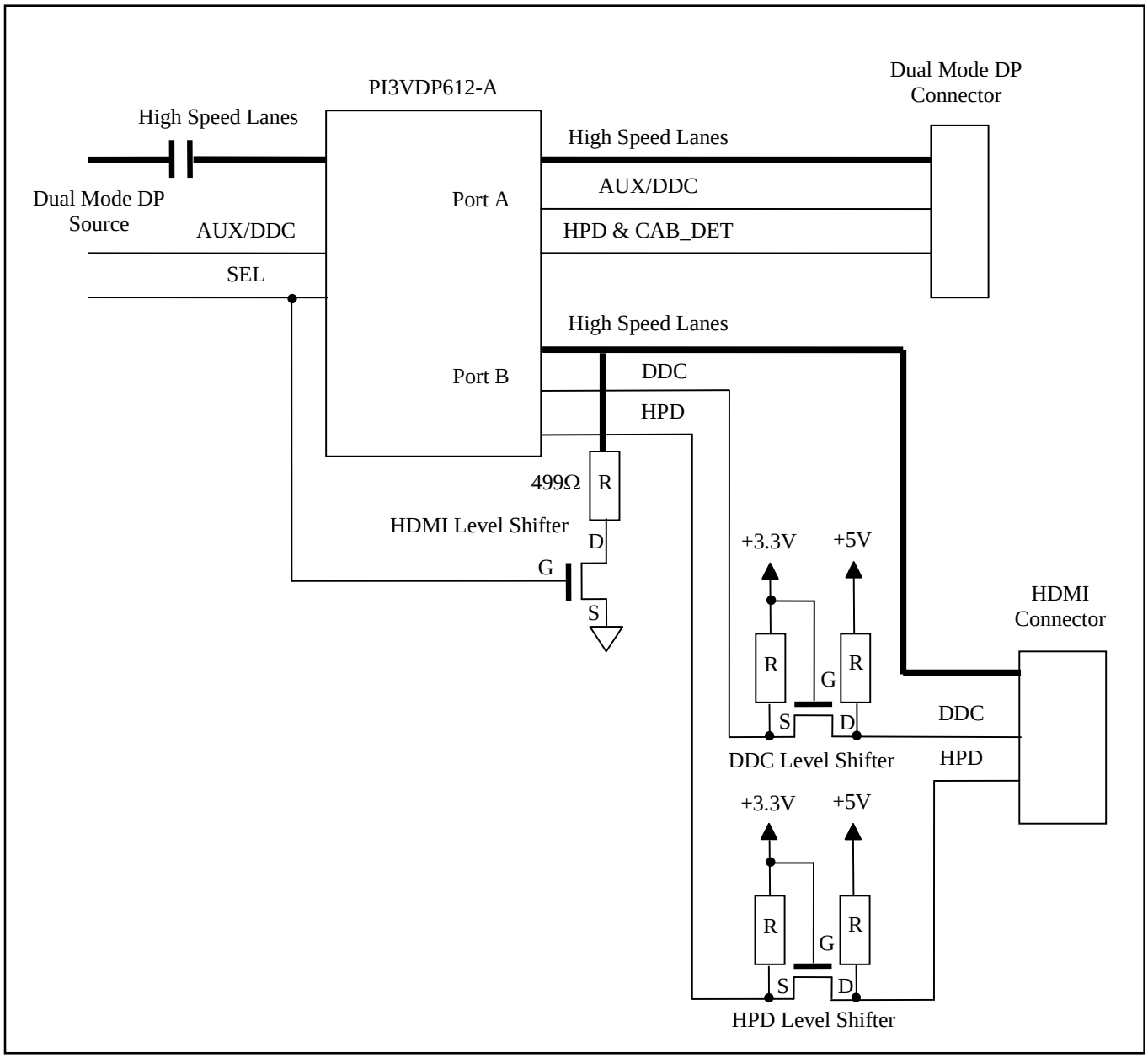

Figure 2: Application Circuit

3. Schematic Diagram

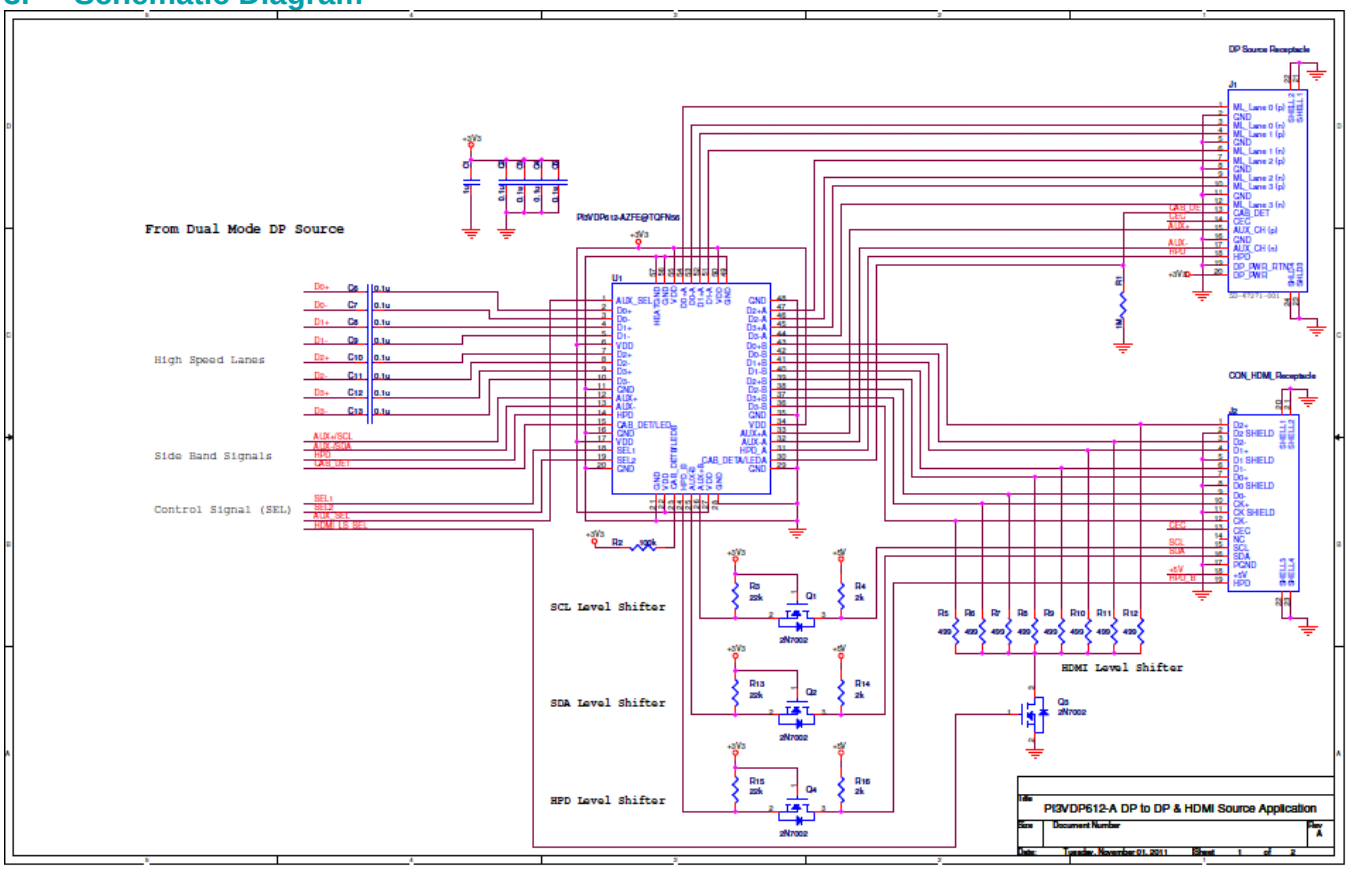

Figure 3: Application Schematics

(1) Signal from Dual Mode DP Source

- **High Speed Signal** – 0.1uF AC-coupling capacitor is needed on the signal from Dual Mode DP Source
- **AUX+/- or DDC Signal** – In this design, we assume that AUX and DDC are multiplexed on the Dual Mode DP Source; hence, it is DC-coupled on these signals to PI3VDP612-A. It is recommended to check the Dual Mode DP Source to see whether it is matched to this assumption or not. Otherwise, circuit is needed to change accordingly
- **HPD** – If Hot Plug Detect (HPD) signal from Sink device is in logic High, it indicates that the selected port sink device is plugged in; Otherwise, selected port sink device is unplugged
- **CAB_DET** – If CAB_DET signal is in logic High, it indicates that the selected port sink device is HDMI/DVI device; If it is logic Low, it indicates that the selected port sink device is DP device. A 100kohm pull-up resistor is placed on CAB_DETB pin as port B is configured as HDMI port in this design
- **SEL1/SEL2/AUX_SEL/HDMI_LS_SEL** – These signals are control signals to select port and enable the HDMI level shifter, when SEL1/SEL2/AUX_SEL is logic Low port A is selected; otherwise, port B is selected. For this design, these signals could be tied together to control

(2) Level Shifters

- **SDA/SCL/HPD Level Shifter** – It is used to level shift from +5V to +3.3V to interface with the Dual Mode DP signal level, 2N7002 NMOS could be used
- **HDMI Level Shifter** – It is used to transform from DP signal level to HDMI signal level. 499Ω pull-down resistor acts as a voltage divider in conjunction with the 50Ω +3.3V pull up resistor on the HDMI sink device side to give a +3.0V DC offset voltage on the high speed HDMI lanes in order to meet HDMI signal level requirement. NMOS (2N7002) connecting from 499Ω resistor to GND is to isolate the 499Ω connecting to GND when the system is powered down in order to meet HDMI compliance test specification's ID 7-3 TMDS-VOFF requirement. Only one NMOS is needed to connect all 8 pieces of 499Ω resistors pull down to GND to save cost and circuit form factor

(3) Power Supply Decoupling

Four 0.1uF and one 1uF capacitors are recommended for PI3VDP612-A. 0.1uF capacitors should be placed as closed to the VDD pins and should be distributed evenly to all VDD pins

(4) DP to HDMI pin mapping

According to the DP interoperability guideline, the following DP Source Device to HDMI pin mapping is needed to follow:

DP Pins	HDMI/DVI Pins
Main Link Lane 0	Channel 2
Main Link Lane 1	Channel 1
Main Link Lane 2	Channel 0
Main Link Lane 3	Channel CLK
AUX CH+	DDC Clock (SCL)
AUX CH-	DDC Data (SDA)
HPD	HPD
Pin 13	Cable Adaptor Detect (Optional)
Pin 14	CEC

Table 1: DP to HDMI Pin Mapping

4. Layout Consideration

(1) Power Supply Decoupling Capacitors

The Power Supply Decoupling Capacitors should be placed as close to the VDD pins of PI3VDP612-A as possible in order to reduce the trace inductance to enhance the decoupling performance. And it should be distributed evenly to all VDD pins

(2) Via on thermal pad

Via(s) is recommended to be placed on the thermal pad layout in order to have good electrical and thermal connection to GND

(3) 499ohm resistors

Traces connecting from the main link of HDMI port to 499ohm resistors should be minimized as these traces act like a stub, which affect the trace impedance at high frequency

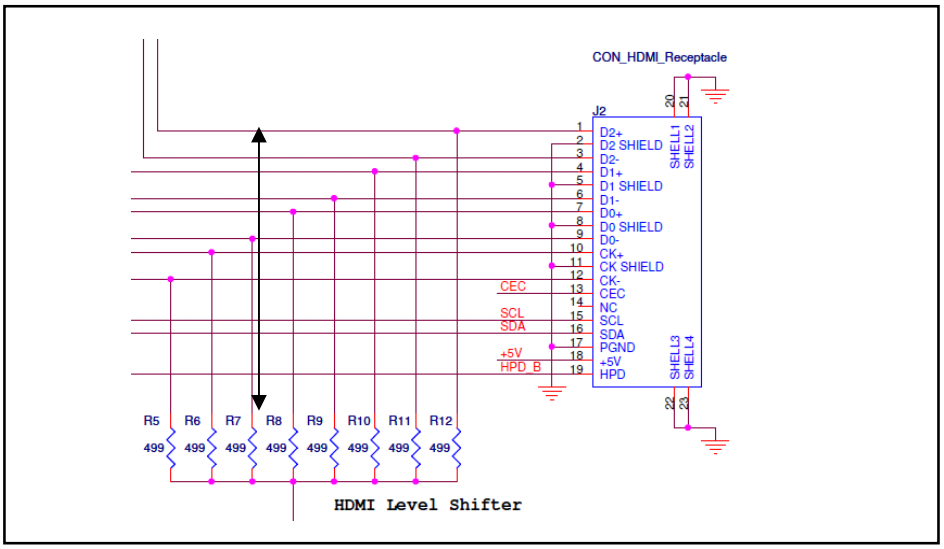

Figure 4: HDMI Level Shifter 499ohm Resistor Trace Consideration in Layout