PI7C9X20404SL / PI7C9X20303SL / PI7C9X20303UL
SlimLine™ PCI Express® Packet Switch Guidelines

1. Introduction

This application note provides a concise and practical guide for the board designers to easily incorporate the Pericom SlimLine PCI Express Packet Switches in their designs. This document includes design outlines, layout cautions and application reminders, which can help the designers to achieve optimal performance in their systems.

2. Power system

The PI7C9X20404SL, PI7C9X20303SL and PI7C9X20303UL packet switches define six types power block, as indicated in table 2-1.

Table 2-1: DC Electrical Characteristics

Power Pins	Min.	Typ.	Max.
VDDA	0.95V	1.0V	1.1V
VDDR	3.0V	3.3v	3.6V
VDDC	0.95V	1.0V	1.1V
VDDAUX	0.95V	1.0V	1.1V
VDDCAUX	0.95V	1.0V	1.1V
VTT	1.425V	1.500V	1.575V

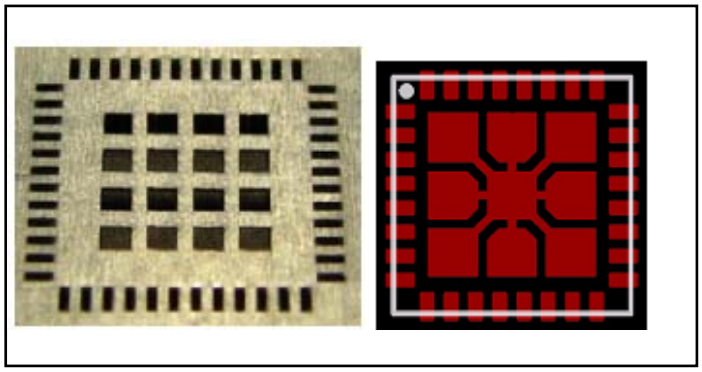
VDDA: analog power supply for PCI Express Interface
VDDR: digital power supply for 3.3v I/O Interface
VDDC: digital power supply for the core
VDDAUX: digital auxiliary power supply for PCI Express Interface
VDDCAUX: digital auxiliary power supply for the core
VTT: transmit termination power supply for PCI Express Interface

Every power pin needs one or more by-pass capacitors (0.1uF to 10uF).
By-pass capacitors must be close to the power pins. If it is possible, place the capacitors on other the side opposite of the ICs. The power noise must be lower than 5%.

3. QFN Center Metal Pad Layout Guidelines

The QFN packages (used by PI7C9X20303UL) have a center metal pad on the underside of the part, typically for grounding and heat conduction. It's this center metal pad that makes this form factor so difficult to use.

This is an example of recommended practice. The basic idea is to have a lower quantity of solder over a broader area. This reduces thickness in the center and other problems associated with large paste, such as outgassing and spattering. This will give good solder distribution and avoid high-centering or outgassing problems.



Note: These two illustrations refer to the TQFN package of PI7C9X20303UL.

4. Differential Signal (Tx/Rx) Layout Guidelines

PCI Express is a dual simplex point-to-point serial differential low-voltage interconnect. The bit rate is 2.5 G bit/sec/lane/direction at introduction. The signal is 8b/10b encoded with an embedded clock. Each lane consists of two pairs of differential signals. Differential trace impedance target of 100Ohm with a tolerance of 15% or better is desired. Tight coupling within the differential pair and increased spacing to other differential pairs helps to minimize crosstalk and EMI. If possible, Tx and Rx differential pairs should route alternately on the same layer (Tx pair next to a Rx pair rather than another Tx pair) to help minimize FEXT.

AC coupling capacitors of 100 nF should be placed at the same location (as close as possible) and should not be staggered from one trace to the other within the pair. While size 0603 capacitors are acceptable, size 0402 capacitors are strongly encouraged. C-packs are not allowed for AC coupling capacitors. The exact same package size of capacitor should be used for each signal in a differential pair. Pad sizes for each of the capacitors should be minimized. The "breakout" into and out of the capacitors should be symmetrical for both signal traces in a differential pair.

From our experience, the high-speed transmission line design is very important and a good transmission line design is a critical factor to achieve good signal quality. If the PCB design can be further improved, especially the traces of the TX and RX of the PCIe lanes, and the reference clock, the overall system stability should be improved.

Breakout Areas near a device package that resulted in "neck-downs" and decreased spacing should be limited to no more than 500 mils in lengths. The necking-down should be done symmetrically on both nets of the differential pair. Breakout sections require special attention to minimize crosstalk.

Test points and probing structures may impact the loss and jitter budgets. If possible, test points and probe structures should not introduce stubs on the differential pairs.

5. Reference Clock Input Pairs

The reference clock input pins connect to external 100MHz differential clock. The signal must match to LVPECL or HCSL spec.

A 100nF capacitor should be placed between the clock source and the packet switch. The purpose of this capacitor is to achieve AC coupling. This AC Coupling ensures the Packet Switch is compatible with the differential clock signals regardless the type of the clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered.

6. Physical Layer Setting (Modified by EEPROM)

The Pericom packet switches support physical signal fine-tuning. It can be achieved using EEPROM.
Table 4-1 / 4-2 / 4-3 show the common configurations used by all the parts in the packet switch family. Please consult the datasheet specific to the part for more details.

Table 6-1: Nominal Driver Current Values (Inom)

HIDRV	LODRV	NOMINAL DRIVER CURENT
0	0	20 mA
0	1	10 mA
1	0	28 mA
1	1	Reserved

Table 6-2: Ratio of Actual Current and Nominal Current

DTX [3:0]	ACTUAL CURRENT / NOMINAL CURRENT
0000	1.00
0001	1.05
0010	1.10
0011	1.15
0100	1.20
0101	1.25
0110	1.30
0111	1.35
1000	0.60
1001	0.65
1010	0.70
1011	0.75
1100	0.80
1101	0.85
1110	0.90
1111	0.95

Note: The default value of the registers DTX[3:0] is "0000".

Table 6-3: De-emphasis Level versus DEQ [3:0]

DEQ [3:0]	$(I_{TX} - I_{EO}) / I_{TX}$	De-emphasis (dB)
0000	1.00	0.00
0001	0.96	-0.35
0010	0.92	-0.72
0011	0.88	-1.11
0100	0.84	-1.51
0101	0.80	-1.94
0110	0.76	-2.38
0111	0.72	-2.85
1000	0.68	-3.35
1001	0.64	-3.88
1010	0.60	-4.44
1011	0.56	-5.04
1100	0.52	-5.68
1101	0.48	-6.38
1110	0.44	-7.13
1111	0.40	-7.96

Note: The default value of the registers DEQ[3:0] is "1000".

7. VGA Support

The PI7C9X20404SL, PI7C9X20303SL and PI7C9X20303UL packet switches support VGA function in all downstream ports. If the system needs to support a VGA chip, The VGA Enable bit in the Bridge Control register (offset 3Ch) is used to control the behaviors to both the VGA frame buffer addresses and to the VGA register addresses. When a VGA compatible device is located at downstream port of the 303UL, the VGA Enable bit must be set. When set, the packet switch will positively decode and forward memory accesses to VGA frame buffer addresses and I/O accesses to VGA registers from the upstream port to the downstream port and block forwarding of these same accesses from the downstream port to the upstream port.

The packet switches implements VGA Enable bit in the Bridge Control register as read-write bit for Port 1 and Port 2.

8. GPIO Control

The SlimLine packet switch provides GPIO pins, which can be programmed as either input or output pins through configuration registers. The user has the ability to monitor the input/output status or control the output signals by reading or writing the corresponding GPIO registers. After the packet switch is powered up, the GPIO pins are set to be input pins by default. Following is a block diagram for illustrating the GPIO pins and the associated control registers.

8.1. Output Operation

For GPIO to act as output pins, the user has to make sure the bus is in tri-state (no other master is driving it) before enabling the output buffer to avoid any possible bus contentions. First, the user puts the desired output status in the GPIO output register, and then sets low to the GPIO O/P enable register. So the output signal will be observed in the GPIO pins immediately.

8.2. Input Operation

To check the input/output status of GPIO pin, the output buffer has to be turned off by setting high to the GPIO Output Enable Register. This will prevent the signal driving by the chip from being read back. After disabling the output buffer, any signal status change in the GPIO pin will be reflected in the input bits of GPIO registers. The values can be captured through Configuration Read Command.

8.3. Example

1) To program GPIO as output pin and drive high off the chip
  Step 1: Write "1" into GPIO output bit of register, which is at D8H
  Step 2: Write "1" into GPIO output enable bit of register, which is at D8H
2) To program GPIO as input pin
  Step 1: Write "0" into GPIO output enable bit of register, which is at D8H
  Step 2: Read value from GPIO input bit of register, which is at D8H

9. SM-BUS

The SlimLine packet switches support the SMBus function. The SMBus address can be configured by GPIO[5:6:7]. The address is 1101XXX_b. Bit 0 is used to indicate R/W. Bit 1, 2, and 3 corresponds to GPIO[5], GPIO[6], and GPIO[7]. The Packet Switch supports only the Host Command (08H/03H). The 03H command is only used to terminate the command that is currently being executed.
Host command 08H used in Read or Write.

To complete a single SMBus read/write operation, two separate SMBus commands must be issued separately in two cycles. The low byte of the first command represents register offset. The high byte represents the port number. The second command represents the data used for the operation.

10. PRSNTx# Pin

When the SlimLine packet switches are connected to slots, the PRSNTx# pins must be connected to the slots' PRSNT# pins and pull-up resisters of 5.1K ohm, so that the presence of the cards can be detected. When slot is empty, the power saving function is enabled.
If the packet switch is used without the slot, the **PRSNTx# must be pulled low** with a 1K ohm resistor. In this case, power saving is never enabled.