Design of Power Factor Correction Circuit Using AP1661A

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1. Introduction

The AP1661A is a current-mode PFC controller operating in DCM boundary mode and pin-to-pin compatible with the predecessor AP1661 but with improved performance.

Designed with advanced Bi-CMOS process, the AP1661A features low start-up current and low operating current for extremely low power consumption to comply with the power saving requirements.

The AP1661A features a special highly linear multiplier to realize near unity power factor and extremely low THD, even with wide range mains.

The AP1661A also has rich protection features such as over voltage protection, brown-out protection and open loop protection.

The AP1661A meets IEC61000-3-2 standard even at one-quadrant load and THD lower than 10% at high-end line voltage and full load.

2. Product Features

- Zero Current Detection Control for DCM Boundary Conduction Mode
- Proprietary Design for Minimum THD
- Ultra-low Start-up Current (30μA)
- Low Quiescent Current (2.5mA)
- Adjustable Output Voltage with Precise OVP
- Internal Start-up Timer
- Disable Function for Reduced Current Consumption
- Totem Pole Output with 600mA Source Current and 800mA Sink Current
- Under-voltage Lockout with 2.5V Hysteresis
- 1% Precise Internal Reference Voltage
- Compact Size with DIP-8 and SOIC-8 Packages

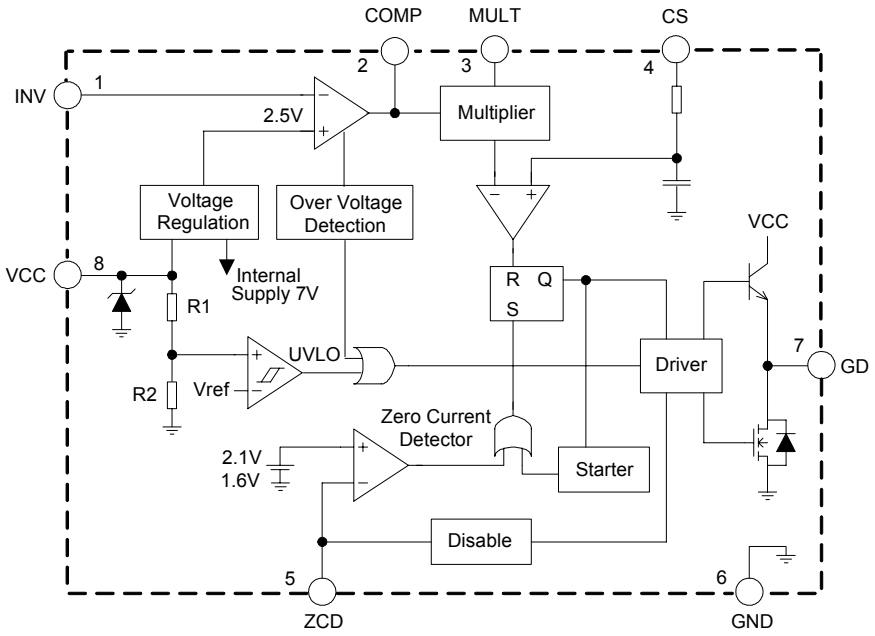

Figure 1. Functional Block Diagram of AP1661A

3. Pin Descriptions

INV (Pin 1): This pin is the inverting input of the error amplifier. It is connected to an external resistor divider which senses the output voltage.

COMP (Pin 2): This pin is the error amplifier output. It is made available for voltage loop compensation by resistor and capacitor combination between pin 1 and this pin.

MULT (Pin 3): Input of the multiplier. This pin senses the AC sinusoidal voltage and is multiplied with comp voltage.

CS (Pin 4): Input of the current control comparator. This pin senses the power switch current and compares with the output of the multiplier. When the CS pin voltage is higher than the output of the multiplier, the external MOSFET will be turned off.

ZCD (Pin 5): Zero current detection input. When the ZCD pin voltage decreases below 1.6V, the external MOSFET will be turned on. If it is connected to GND, the device is disabled.

GND (Pin 6): Ground. Current return for gate driver and control circuit of the IC.

GD (Pin 7): Gate driver output. A series resistor between this pin and the gate of power switch can reduce high frequency noise.

VCC (Pin 8): Supply voltage of gate driver and control circuits of the IC.

4. Functional Block Description

Supply Block

As shown in Figure 2, pin 8 is the VCC of AP1661A. There is a zener diode with typical 22V clamp voltage (30mA rated) to protect the device. A voltage regulator generates a 7.5V voltage to function as the IC's internal supply except for the output stage which is supplied directly from VCC. In addition, a precise internal reference (2.5V±1%@25°C) is used to get a good regulation.

An undervoltage lockout (UVLO) comparator is used to ensure a reliable operation

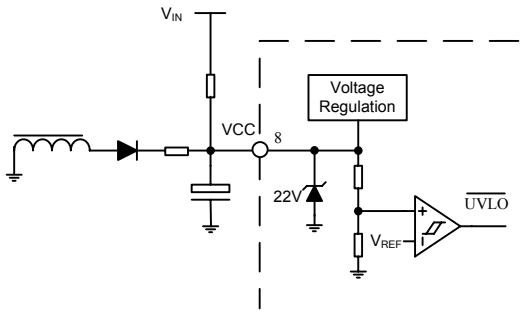

Figure 2. Supply Block

Error Amplifier and OVP Block

The error amplifier regulates the PFC output voltage. The internal reference on the non-inverting input of the error amplifier is 2.5V. The error amplifier's inverting input (INV) is connected to an external resistor divider which senses the output voltage. The output of error amplifier is one of the two inputs of multiplier. A compensation loop is connected outside between INV and the error amplifier output. Normally, the compensation loop bandwidth is set very low to realize good power factor for PFC converter.

To ensure fast over voltage protection, the internal OVP function is added. If the output over voltage occurs, excess current will flow into the output pin of the error amplifier through the feedback compensation capacitor. The AP1661A monitors the current flowing into the error amplifier output pin. When the detected current is higher than 40μA, the dynamic OVP is trigged. The IC will be disabled and the drive signal is stopped. If the output over voltage lasts so long that the output of error amplifier goes below 2.25V, static OVP will take place. Also the IC will be disabled until the output of error amplifier returns to its linear region.

R1 and R2 (see Figure 3) will be selected as below:

$$\frac{R1}{R2} = \frac{Vo}{2.5V} - 1 \qquad R1 = \frac{\Delta V_{OVP}}{40\mu A}$$

Pin 2 (COMP) is the output of the error amplifier. A slow bandwidth compensation network is placed between this pin and INV (pin 1) to avoid output voltage ripple influence to the system.

In the simplest case, this compensation is just a capacitor, which provides a low frequency pole as well as a high DC gain.

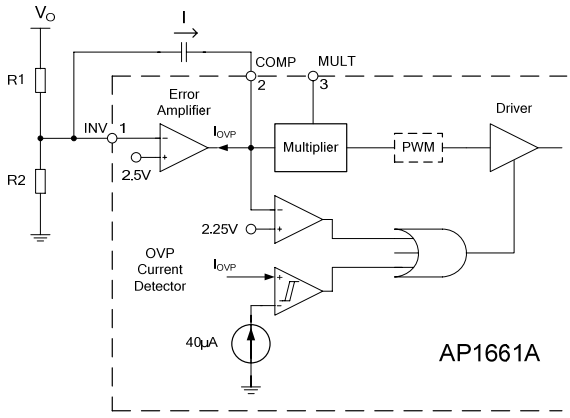

Figure 3. Error Amplifier and OVP Block

Zero Current Detection Block

The AP1661A is a DCM boundary conduction current mode PFC controller. Usually, the zero current detection (ZCD) voltage signal comes from the auxiliary winding of the boost inductor. When the voltage of this pin decreases below 1.6V, the driver signal becomes high to turn on the external MOSFET.

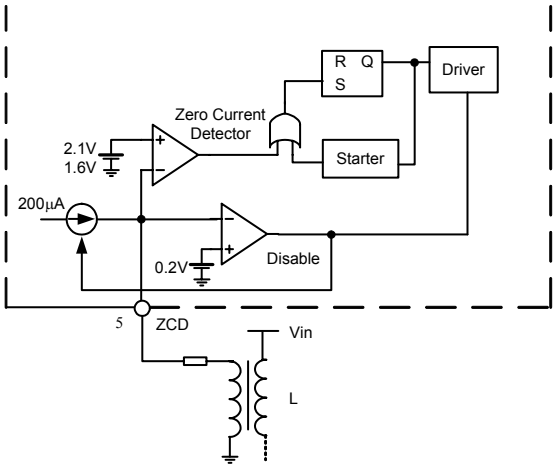

Figure 4. Zero Current Detection Block

The boost inductor winding turn ration, m, should be selected to ensure ZCD pin voltage higher than 2.1V during MOSFET turned-off. Then

$$m \le \frac{Vo - \sqrt{2} \cdot Vinrms(max)}{2.1}$$

A resistor is placed between the auxiliary winding and ZCD pin to limit the current sink into the IC. The limiting resistor's actual value can be fine-tuned to make the turn-on of the MOSFET occur exactly at the valley of the drain voltage oscillation. When the boost inductor current reaches zero, the inductor will oscillate with the MOSFET drain capacitance (see Figure 5). This will minimize the power loss when turned on.

An internal starter generates a pulse to turn on the external MOSFET at start-up since no signal is coming from ZCD. The repetition rate of the starter is greater than 70ms (@14kHz).

The ZCD pin can also be used to disable the IC. If the voltage of this pin falls below 0.25V, the IC will be shut down. Thus, the power consumption of the IC is reduced.

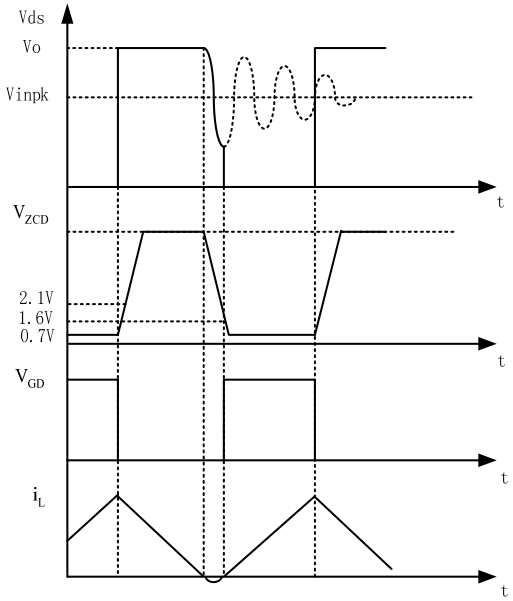

Figure 5. Optimum MOSFET Turn-on

Multiplier Block (Figure 6)

The multiplier has two inputs. One (Pin 3) is the divided AC sinusoidal voltage which makes the current sense comparator threshold voltage vary from zero to peak value. The other input is the output of error amplifier (Pin 2). In this way, the input average current wave will be sinusoidal as well as reflects the load status. Accordingly, a high power factor and good THD are achieved. The multiplier transfer character is designed to be linear over a wide dynamic range, namely, 0V to 3V for pin 3 and 2.0 V to 5.8V for pin 2. The relationship between the multiplier output and inputs is described as the following equation:

$$V_{CS} = k \times (V_{COMP} - 2.5) \times V_{MULT}$$

where V_{CS} (Multiplier output) is the reference for the current sense, k is the multiplier gain, V_{COMP} is the voltage on pin 2 (error amplifier output) and V_{MULT} is the voltage on pin 3.

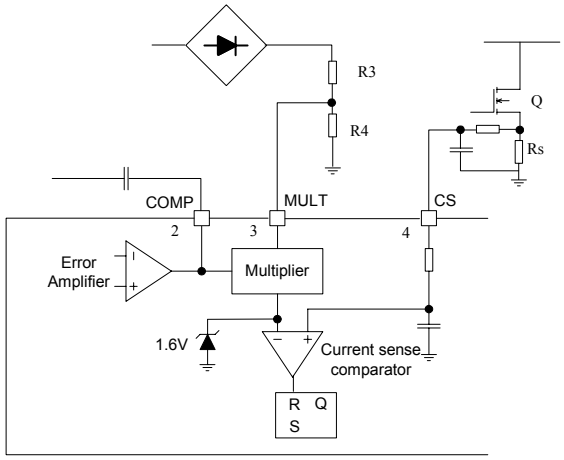

Figure 6. Multiplier Block

Figure 7 shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed in the range of 0 to 3V of V_{MULT} and 0 to 1.6V of V_{CS}.

V_{MULTpk}, the peak value for V_{MULT} occuring at maximum mains voltage, should be 3V or below. The MULT pin resister divider (see figure 6) will be as below:

$$\frac{R4}{R3+R4}=\frac{V_{MULTpk}}{\sqrt{2}\cdot Vinrms(max)}$$

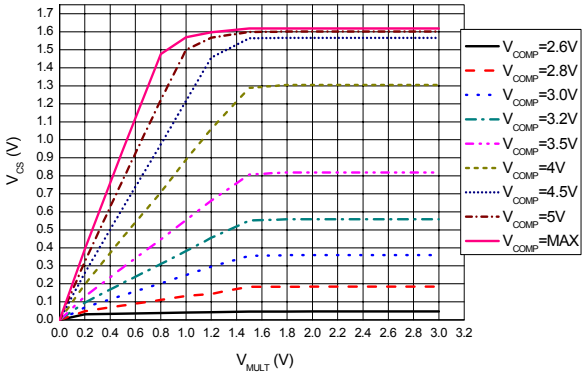

Figure 7. Multiplier Characteristics Family

In practical application, the typical resistor divider of MULT pin can be set 1/170 to achieve a good THD performance.

The AP1661A is equipped with a special circuit that reduces the AC input current conduction dead-angle near the zero-crossings of the line voltage (crossover distortion). In this way, the THD of the current is considerably reduced.

Current Comparator and PWM Latch

The PFC switch's turn-on current is sensed through an external resistor in series with the switch. When the sensed voltage exceeds the threshold voltage (the multiplier output voltage), the current sense comparator's output will become low and the external MOSFET will be turned off. This ensures a cycle-by-cycle current mode control operation.

The sense resistor value is calculated as:

$$R_S \le \frac{V_{CSpk}}{I_{Rspk}}$$

where V_{CSpk} is the maximum voltage of V_{CS}, which can be set 1.6V for linear operation in the entire working range.

When the power MOSFET is turned on, a narrow spike on the leading edge of the current waveform can usually be observed. There is an internal R/C filter in AP1661A to attenuate this noise and prevent the false triggering caused by the turn-on spike. In low power applications, the external R/C filter connected to the CS pin is not needed.

Driver

The AP1661A totem pole output stage is capable of driving a power MOSFET or IGBT with 600mA source current and 800mA sink current.

GND

Pin 6 is the Ground of the IC. This pin acts as the current return both for the internal circuitry signal and for the gate drive current. These two paths should be laid out separately in the printed circuit board.

5. Comparison Between AP1661A and AP1661

The AP1661A is pin-to-pin compatible with AP1661 and offers improved performance. Table 1 compares the two devices and lists the key parameters that have the most significant impact on the design.

Table 1. Comparison Between AP1661A and AP1661

Parameter	AP1661	AP1661A
Turn on & Turn off Threshold (typ.)	12/9.5V	12.5/10V
Start-up Current (typ.)	50μA	30μA
Quiescent Current (typ.)	2.6mA	2.5mA
Operating Supply Current (typ.) @C_L=1nF and f=70kHz	4mA	3.5mA
Enable Threshold on Pin 1 INV (max.)	720mV	600mV
Current Sense Reference Clamp (typ.)	1.7V	1.6V

The AP1661A has an increased 0.5V UVLO threshold to achieve more margin for the gate drive voltage. The low start-up current and operating current can reduce the power consumption to satisfy the power saving requirements. INV(pin 1) features brown-out and open-loop protection. To start the IC, the voltage on this pin must exceed 0.5V (typ.). When the input voltage is too low or the upper feedback resistor fails open, the device will be disabled. The INV can also be used as a remote control input for power management. A lower current sense clamp voltage allows lower peak current with the same sense resistor to get a reliable over current protection. The lower clamp voltage also allows a lower sense resistor for the same peak current, which can reduce the associated power dissipation to meet energy saving requirement.

6. Typical Application of AP1661A

Here a wide range of demonstration board is designed and the evaluation results are presented.

The target specification:
AC voltage RMS voltage: Vin_rms = 85V to 265V
DC output regulated voltage: V_O = 400V
Rated output power: P_O = 90W
Minimum switching frequency: f_{SW}(min)=35kHz
Expected efficiency: η>90%
Output voltage ripple at full load: $\Delta V_O \leq \pm 30V$
Maximum output overvoltage: ΔV_{OVP}=50V

Figure 8 shows the designed electrical schematic with the values of all parts.

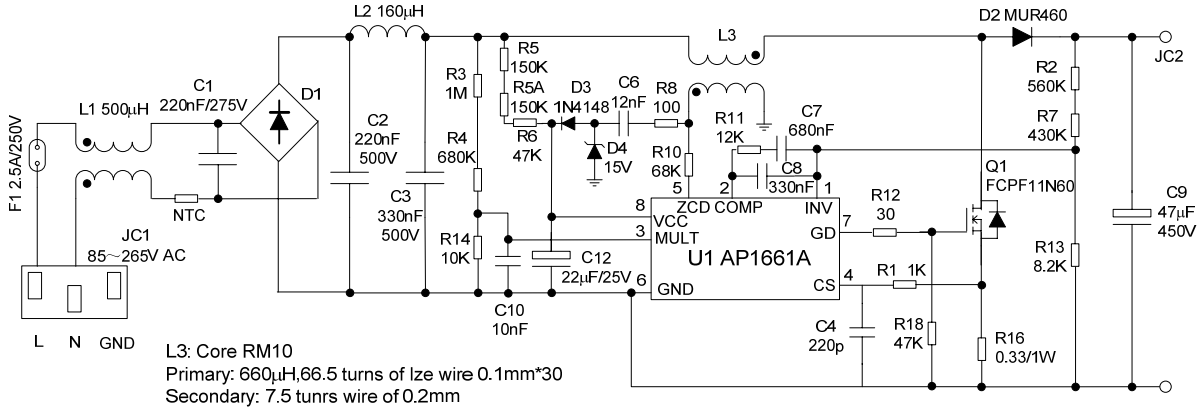

Figure 8. Design Electrical Schematic of AP1661A

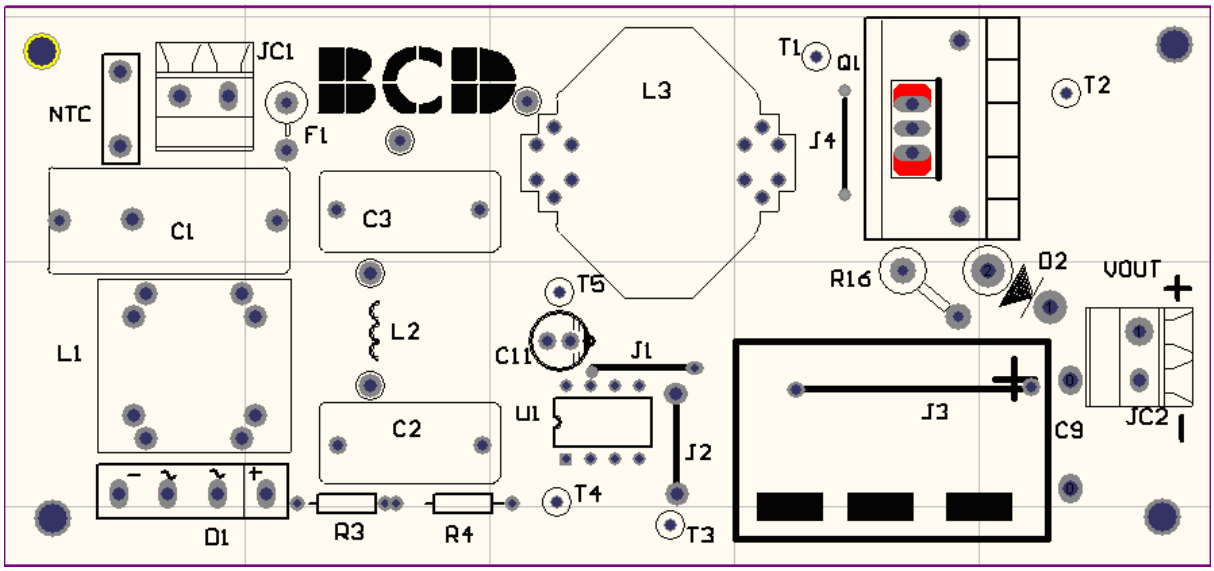

Figure 9. Demo Board PCB and Component Layout (Top View, 125mm×56mm)

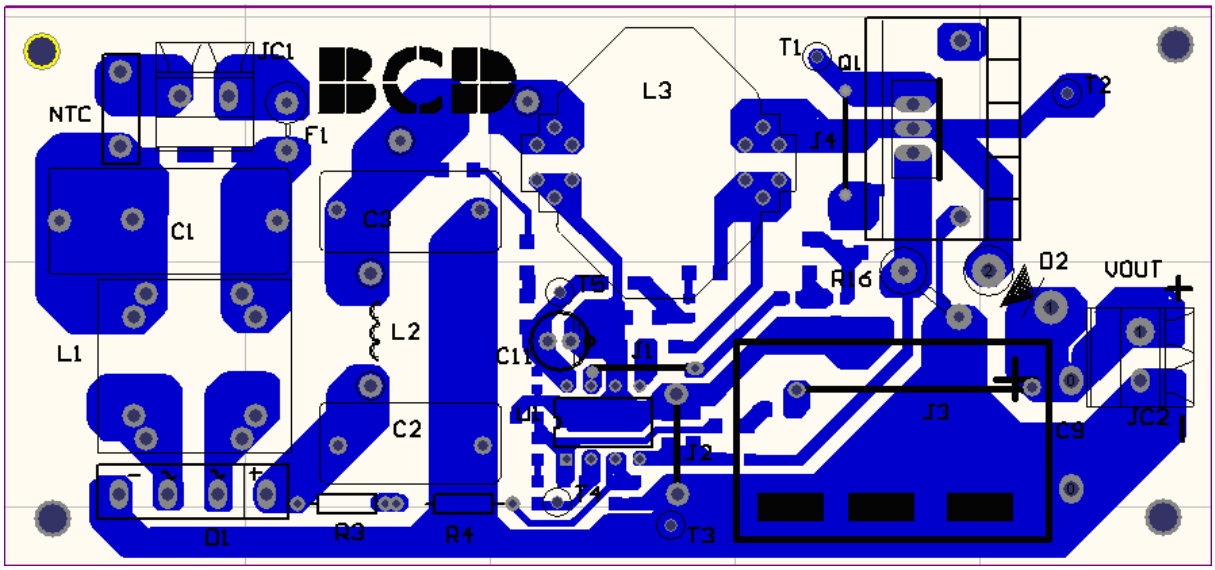

Figure 10. Demo Board PCB and Component Layout (Bottom View, 125mm×56mm)

To evaluate the performance of the PFC demonstration board, the following parameters have been measured: PF (Power Factor), THD (Total Harmonic Distortion), ΔV(Peak-to-Peak Output Voltage Ripple), Vo (Output Voltage) and η (Efficiency). Table 2 and Table 3 give the test results of AP1661 and AP1661A at full load condition respectively.

Compare AP1661A with AP1661, the converter can get a higher PF and better THD, especially at high end line voltage. The THD of AP1661A can even be reduced below 10% at full load.

Table 2. AP1661-90W Evaluation Results

Vin_rms (V)	P_{IN} (W)	P_O (W)	η (%)	V_O (V)	ΔV_O (V)	PF	THD (%)
85	99.21	89.85	90.57	398.8	17	0.9997	1.88
110	95.672	89.84	93.90	398.8	17	0.9992	3.55
150	93.996	89.84	95.58	398.9	17	0.9978	5.05
230	93.058	89.84	96.54	398.9	17	0.9874	8.66
250	92.977	89.82	96.60	398.9	17	0.9822	10.2
265	92.933	89.81	96.64	398.9	17	0.9773	11.71

Table 3. AP1661A-90W Evaluation Results

Vin_rms (V)	P_{IN} (W)	P_O (W)	η (%)	V_O (V)	ΔV_O (V)	PF	THD (%)
85	98.43	89.2	90.62	396.2	17	0.9997	1.78
110	94.908	89.18	93.96	396.2	17	0.9992	3.41
150	93.262	89.18	95.62	396.2	17	0.9978	4.87
230	92.344	89.20	96.6	396.3	17	0.9898	5.26
250	92.25	89.19	96.68	396.3	17	0.9856	5.47
265	92.205	89.18	96.72	396.3	17	0.9818	5.98