

# WLED Backlighting Solution for Medium LCD Panel Designed with AP3608E+AP3039

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## 1. Introduction

With the enhancement of environment-protecting consciousness, WLED backlighting is more popular than traditional CCFL backlighting. Nowadays, WLED becomes the mainstream of the small size LCD panel backlighting instead of CCFL. Because of so many advantages of WLED, such as fast response, safe, long lifetime, small size and so on, WLED will become more and more important in the medium size and large size LCD panel backlighting in the future. To compare with the small size LCD panel, medium and large size LCD panel need tens of WLEDs. It means many new requirements are needed to be met, for example, higher driver voltage and current match between WLED strings.

BCD semiconductor proposes a WLED backlight

solution for medium LCD panel under this condition.

## 1.1 Solution Description

The solution schematic is shown in Figure 1, The solution consists of two ICs, one is AP3039, the other is AP3608E. The solution can drive totally 80 WLEDs, and the current match accuracy between any two strings is within  $\pm 1.5\%$ . The operation frequency can be adjustable, which allows trade-offs between external component size and system efficiency. WLED brightness can be adjusted by PWM dimming function. The internal soft start circuit effectively reduces the inrush current when start-up. The solution has multiple features to protect the system from fault conditions. It features under voltage lockout protection, over voltage protection, over temperature protection and WLED open protection.

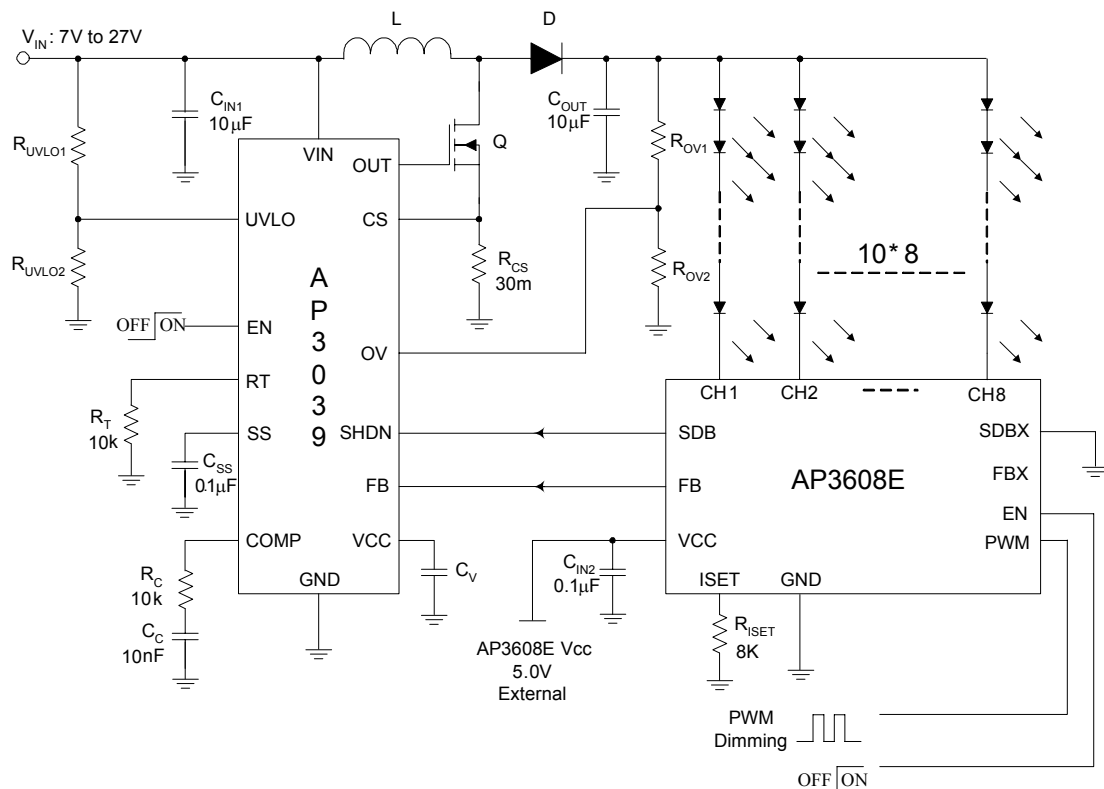


Figure 1. BCD Solution Schematic

## 1.2 AP3039 Description

The AP3039 is a high voltage low-side N-channel MOSFET controller ideal for boost converter. It adopts current mode and its operation frequency is adjustable from 400kHz to 1MHz. In the solution, the boost converter built up by AP3039 generates a high output voltage for WLEDs.

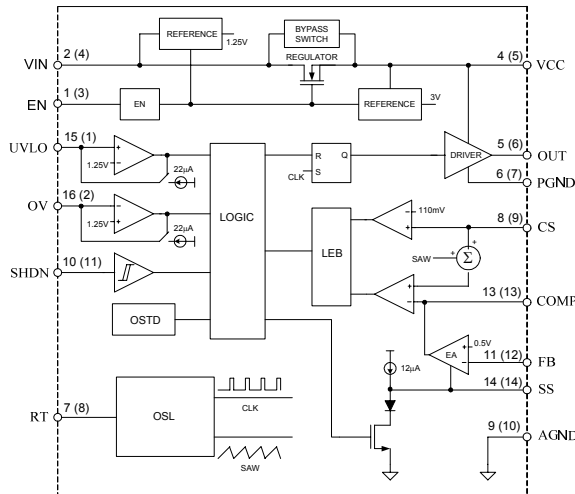


Figure 2. Functional Block Diagram of AP3039

Figure 2 is the functional block diagram of AP3039. Operation process: at the start of each oscillation cycle, the SR latch is set and external power switch Q (refer to Figure 1.) turns on. The switch current will increase linearly. The voltage on external sense resistor  $R_{CS}$  (refer to Figure 1.) is proportional to the switch current. This voltage is added to a stabilizing ramp and the result is fed into the non-inversion input of the PWM comparator. When this non-inversion input voltage exceeds inversion input voltage of PWM comparator which is the output voltage level of the error amplifier EA, the SR latch is reset and the external power switch turns off. This voltage level is the amplified signal of the voltage difference between feedback voltage and reference voltage of 0.5V. It is clear that the voltage level at inversion input of PWM comparator sets the peak current level to keep the output in regulation.

## 1.3 AP3608E Description

The AP3608E is designed for WLED display application, which contains eight well-matched current sinks to provide constant current through WLED. The full scale WLED current can be adjusted from 10mA to 100mA per channel with an external resistor. The maximum output current is 800mA when 8 channels are all enabled. The SDB pin and FB pin are the interface terminals for working with AP3039. FB pin samples voltage of each channel,

and exports the lowest voltage of the string to AP3039. If there is some channel unused, the channel pin should be connected to ground. The dimming can be achieved by feeding a PWM signal to PWM pin. Figure 3 is the functional block diagram of AP3608E. In the solution, AP3608E supplies current to 10\*8 (10 series, 8 strings) WLEDs with good current match accuracy.

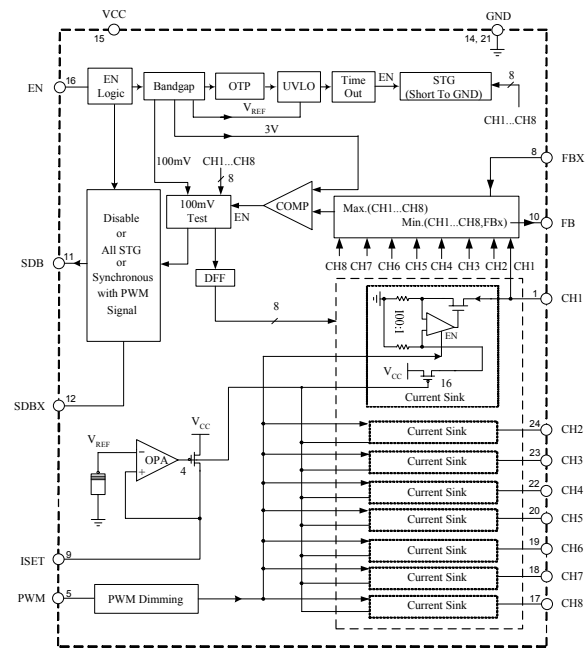


Figure 3. Functional Block Diagram of AP3608E

## 2. Component Selection

In the solution shown in Figure 1, several peripheral components are needed. This section will give some suggestion on how to select these components.

### 2.1 AP3039 Peripheral Component Selection

#### 2.1.1. $C_{IN1}$

The input capacitor ( $C_{IN1}$ ) of AP3039 filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 10 $\mu$ F ceramic capacitor is recommended in the typical application.

#### 2.1.2. L

When choosing an inductor, the first step is to determine the operating mode: continuous conduction mode (CCM) or discontinuous conduction mode (DCM). When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small size inductor is required, DCM mode can be chosen. In DCM mode,

the inductor ripple current and peak current are higher than those in CCM.

When the value of inductor is less than  $L_{CCM(MIN)}$ , the system operates in DCM mode.

$$L_{CCM(MIN)} = \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \left( \frac{V_{OUT} - V_{IN}}{I_{OUT} * f_{OSC}} \right) * \frac{\eta}{2}$$

Where  $\eta$  is the expected efficiency (the value can be taken from an appropriate curve in the datasheet).

### 2.1.3. D

The boost converter requires a diode D to carry the inductor current during the MOSFET off time. Schottky diodes are recommended due to their fast recovery time and low forward voltage. D should be rated to handle the maximum output voltage (plus switching node ringing) and the peak switch current. The conduction loss of diode is calculated by:

$$P_{DIODE} = I_{RMS\_OFF} * V_F$$

$$\left( I_{RMS\_OFF} \right)^2 = \left[ \frac{V_{IN}}{V_{OUT}} * \left( I_{IN}^2 + \frac{\Delta I_L^2}{12} \right) \right]$$

Where  $V_F$  is the forward voltage of the Schottky diode.

### 2.1.4. Q

When selecting the power MOSFET Q, some tradeoffs between cost, size, and efficiency should be made. Losses in the MOSFET can be calculated by:

$$P_{MOS} = P_{CONDUCTION} + P_G + P_{SW}$$

Where  $P_{CONDUCTION}$  is conduction loss,  $P_G$  is gate charging loss, and  $P_{SW}$  is switching loss.

$$P_{CONDUCTION} = K_{TH} * I_{RMS\_ON}^2 * R_{DS(ON)}$$

Where  $K_{TH}$  is the factor for the increase in on resistance of MOSFET due to heating. For an approximate analysis, the factor can be ignored and the maximum on resistance of the MOSFET can be used.

Gate charging loss,  $P_G$ , results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated as:

$$P_G = Q_g * V_{CC} * f_{OSC}$$

Where  $Q_g$  is the total gate charge of the MOSFET. Power of  $V_{CC}$  is applied by  $V_{IN}$  and the MOSFET driving current flows through  $V_{CC}$  regulator. This loss  $P_{V_{CC}}$  is estimated as:

$$P_{V_{CC}} = (V_{IN} - V_{CC}) * Q_g * f_{OSC}$$

So the total gate charging loss is  $P_{G\_TOTAL} = P_G + P_{V_{CC}}$ . The total gate charging loss occurs in IC and not in the MOSFET itself actually.

Switching loss,  $P_{SW}$ , occurs in transition period as the MOSFET turns on and off. This loss is consisted of turn on loss and turn off loss.

$$P_{TURNON} = \frac{1}{6} \left( I_{IN} - \frac{\Delta I_L}{2} \right) * V_{OUT} * t_r * f_{OSC}$$

$$P_{TURNOFF} = \frac{1}{6} \left( I_{IN} + \frac{\Delta I_L}{2} \right) * V_{OUT} * t_f * f_{OSC}$$

$$P_{SW} = P_{TURNON} + P_{TURNOFF}$$

Where  $t_r$  and  $t_f$  are the rise and fall times of the MOSFET.  $\Delta I_L$  is calculated by :

$$\Delta I_L = \frac{(V_{OUT} - V_{IN}) * V_{IN}}{L * f_{OSC} * V_{OUT}}$$

The maximum drain-to-source voltage applied across the MOSFET is  $V_{OUT}$  plus the ring due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the MOSFET is  $V_{CC}$  plus the ring from gate to source. So the voltage rating of the MOSFET selected must withstand the maximum drain-to-source voltage, and withstand the maximum gate-to-source voltage. The MOSFET with  $V_{DS}=60V$  and  $V_{GS}>10V$  is recommended in typical application.

### 2.1.5. C<sub>OUT</sub>

The output capacitor of the boost converter is used for output filtering and keeping the loop stable. The ESR value is the most important parameter of the  $C_{OUT}$ , because it directly affects the system stability and the output ripple voltage.

The total output ripple can be calculated by the following equations:

$$\Delta V_O = \Delta V_{O(CO)} + \Delta V_{O(ESR)}$$

$$\Delta V_{O(CO)} = \frac{I_{OUT}}{C_O} * \left( \frac{V_{OUT} - V_{IN}}{V_{OUT} * f_{OSC}} \right)$$

$$\Delta V_{O(ESR)} = I_{L\_PEAK} * R_{ESR(CO)}$$

$$(I_{L\_PEAK} = \frac{\Delta I_L}{2} + I_{IN})$$

Where  $\Delta V_{O(CO)}$  is caused by the charging and discharging on the output capacitor, and  $\Delta V_{O(ESR)}$  is caused by the capacitor's equivalent series resistance (ESR).

To get low output ripple, a low ESR ceramic capacitor is a good choice. The capacitance of  $10\mu F$  is recommended.

### 2.1.6. $R_{UVLO1}$ & $R_{UVLO2}$

The AP3039 contains an under voltage lockout (UVLO) circuit. Two resistors  $R_{UVLO1}$ ,  $R_{UVLO2}$  are connected from UVLO pin to ground and to the  $V_{IN}$  pin (refer to Figure 4.). The resistor divider must be designed such that the voltage on the UVLO pin is higher than 1.25V when  $V_{IN}$  is in the desired operating range. If this under voltage threshold is not met, all functions of AP3039 are disabled and system remains in a low power standby state. The UVLO threshold rising edge can be calculated by:

$$V_{in\_uvlo} = (\frac{R_{uvlo1}}{R_{uvlo2}} + 1) * 1.25V$$

The UVLO hysteresis is accomplished by an internal  $20\mu A$  current source which is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated. When the UVLO pin voltage falls below the threshold, the current source is turned off. The UVLO hysteresis can be calculated by:

$$V_{UVLO\_HYS} = R_{UVLO1} * 20\mu A$$

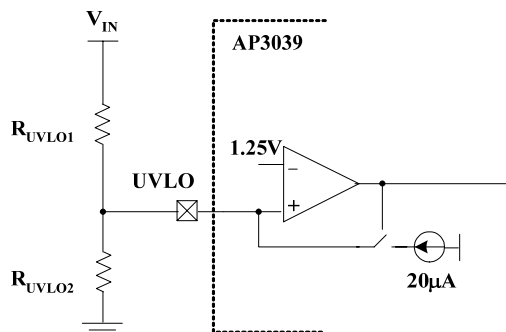


Figure 4. UVLO Protection Circuit

### 2.1.7. $R_{OV1}$ & $R_{OV2}$

The AP3039 has an over voltage protection (OVP) circuit. Two resistors  $R_{OV1}$ ,  $R_{OV2}$  are connected from OV pin to ground and to the output  $V_O$  (refer to Figure 5.)

When the loop is open or the output voltage becomes excessive in any case, the voltage on OV pin will exceed 1.25V, as a result, all functions of AP3039 are disabled and the output voltage will fall. The OVP threshold rising edge can be calculated by:

$$V_{o\_ovp} = (\frac{R_{ov1}}{R_{ov2}} + 1) * 1.25V$$

The OVP hysteresis is accomplished with an internal  $20\mu A$  current source and the operation process is the same as UVLO. The OVP hysteresis can be calculated by:

$$V_{OVP\_HYS} = R_{OV1} * 20\mu A$$

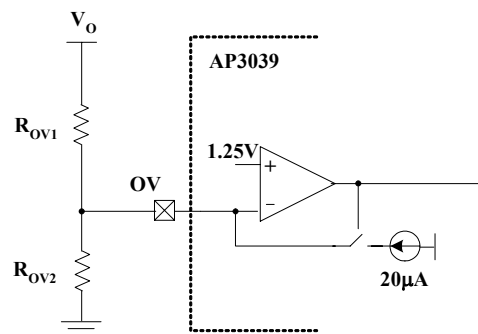


Figure 5. OVP Protection Circuit

### 2.1.8. $R_T$

An external resistor  $R_T$  is connected from RT pin to GND to set the operating frequency (refer to Figure 1). Operating frequency range is from 400kHz to 1MHz (as shown in Table 1). High frequency operation optimizes the regulator for the smallest component size, while low frequency operation can reduce the switch losses.

$R_T$ (k $\Omega$ )	Operation Frequency (kHz)
147	400
95	600
68	800
51	1000

Table 1. Frequency Selection

### 2.1.9. C<sub>SS</sub>

The AP3039 has a soft start circuit to limit the inrush current during startup. The soft start feature allows the boost converter output to gradually reach the initial steady state output voltage, thereby reducing startup stresses and current surges. The startup time is controlled by an internal 12μA current source and an external soft start capacitor C<sub>SS</sub> which connected from SS pin to GND (refer to Figure1). At power on, after the V<sub>IN</sub> UVLO threshold is satisfied, the internal 12μA current source charges the external capacitor C<sub>SS</sub>. The capacitor voltage will ramp up slowly and limit COMP pin voltage and the switch current.

### 2.1.10. C<sub>V</sub>

The VCC pin of AP3039 should be decoupled with a ceramic capacitor placed as close to the AP3039 as possible. This capacitor keeps VCC voltage steady when the system operates at a high frequency. The X5R or X7R ceramic capacitor should be adopted as decoupling capacitor because of their good thermal stability, and the capacitance of 0.47μF is recommended.

### 2.1.11. R<sub>CS</sub>

An external resistor R<sub>CS</sub> is connected from CS pin to PGND to detect switch current signal for current-mode boost converter. The current limit threshold voltage V<sub>CS</sub> of AP3039 is fixed at 110mV. The required resistance R<sub>CS</sub> is dependent to the peak inductor current at the end of the switch on-time, and can be calculated by the following equations:

$$R_{C\_MAX} < \frac{V_{CS}}{I_{L\_PEAK}}$$

$$P_{R_{CS}} = I_{RMS\_ON}^2 * R_{CS}$$

$$\left( I_{RMS\_ON}^2 = \frac{V_{OUT} - V_{IN}}{V_{OUT}} * \left( I_{IN}^2 + \frac{\Delta I_L^2}{12} \right) \right)$$

### 2.1.12. R<sub>C</sub>&C<sub>C</sub>

AP3039 adopts current mode PWM control to improve transient response and achieve simple loop compensation circuit. The designer should select R<sub>C</sub> and C<sub>C</sub> by trial and error to ensure the system have enough bandwidth and phase margin. R<sub>C</sub>=3.9k and C<sub>C</sub>=10n are sufficient for AP3039 work in 1MHz.

## 2.2 AP3608E Peripheral Component Selection

### 2.2.1 C<sub>IN2</sub>

The VCC pin of AP3608E should be decoupled with a ceramic capacitor placed as close to the AP3608E as possible. The X5R or X7R ceramic capacitor should be adopted as decoupling capacitor because of their good thermal stability, and the capacitance of 0.1μF is recommended.

### 2.2.2 R<sub>ISET</sub>

The maximum WLED current can be set up to 100mA per channel, by using the ISET pin. To set the reference current (I<sub>SET</sub>), connect a resistor (R<sub>ISET</sub>) between this pin and ground. The relationship of I<sub>SET</sub> and R<sub>ISET</sub> can be expressed by:

$$I_{SET} = 1.194V / R_{ISET}$$

This reference current is multiplied internally with a gain (K) of 400, and then mirrored on all enabled channels. This sets the maximum WLED current, referred to as 100% current (I<sub>CHX\_MAX</sub>). The value can be calculated by the following formula:

$$I_{CHX\_MAX} = K \cdot I_{SET}$$

The WLED current can be reduced from 100% by PWM dimming control.

## 3. Operation

### 3.1 Initialization

When peripheral components are ready, the solution should be initialized by following the below steps.

#### 3.1.1 STG (Short to Ground)

Before the solution begins to work, any unused channel should be connected to ground at first. For example, if CH8 is not needed in the application, CH8 should be connected to ground as shown in Figure 6. It is not allowed to float the unused channel or to connect unused channel to ground after solution powers on.

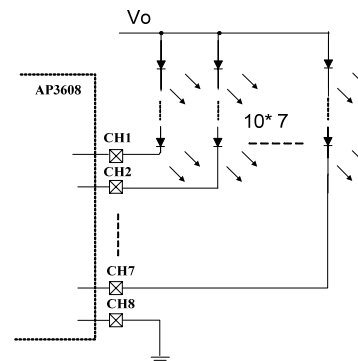


Figure 6. AP3608E Channel Set

### 3.1.2 Set $I_{CHX\_MAX}$

Set the maximum WLED current of all used channels according to the application, the detail information please refers to 2.2.2 section.

### 3.1.3 Power On

In the solution, AP3039 is suggested to power on first, and the AP3608E is the second.

## 3.2 PWM Dimming

After initialization is finished, the system goes into normal work mode. On the normal work mode, PWM dimming function of the solution provides less WLED color distortion and can be used to adjust the LCD brightness according to different application.

The PWM pin of AP3608E is used to achieve PWM dimming function. The WLED current can be adjusted by applying the PWM signal to PWM pin. On this mode, all enabled channels can be adjusted at the same time and the brightness can be adjusted from  $1\% \cdot I_{CHX\_MAX}$  to  $100\% \cdot I_{CHX\_MAX}$ . During the “high level” time of the PWM signal, the WLED turns on and the 100% current flows through WLED. During the “low level” time of the PWM signal, the WLED turns off and almost no current flows through WLED. So the average current through WLED is changed and the brightness is adjusted. The external PWM signal applied to PWM pin should be in the range of 100Hz to 2kHz for good dimming accuracy.

An example for PWM dimming is shown in Figure 8. All 8 channels are set to the maximum current  $I_{CHX\_MAX}$  at the beginning. When a 50% duty cycle PWM signal is applied to PWM pin, average current valued  $50\% \cdot I_{CHX\_MAX}$  flows through the 8 channels. When an 80% duty cycle PWM signal is applied to PWM pin, average current valued  $80\% \cdot I_{CHX\_MAX}$  flows through the 8 channels.

On PWM dimming mode, AP3608E gives a signal which is synchronous with PWM signal to AP3039 by SDB pin. During the “high level” time of the PWM signal, AP3039 supplies the proper output

voltage to WLEDs according to the signal of FB pin from AP3608E. During the “low level” time of the PWM signal, AP3039 keeps the output voltage regardless of the signal of FB pin, that is to say, signal of FB pin from AP3608E can not control the boost loop during PWM “low level” time.

## 3.3 Protection

### 3.3.1 UVLO Protection

The solution has the UVLO protection. Both AP3039 and AP3608E have the UVLO function. The system is disabled until  $V_{IN}$  of AP3039 exceeds the UVLO threshold and  $V_{CC}$  of AP3608E exceeds the UVLO threshold at the same time. The UVLO threshold and hysteresis of AP3039 can be set according to different application. The detailed information please refers to 2.1.6 section. The UVLO threshold and hysteresis of AP3608E is fixed, the typical UVLO threshold value is 3.8V and the typical hysteresis value is 200mV.

### 3.3.2 Over Voltage Protection

The solution has the OV protection. Set the proper OV threshold according to the number of WLEDs in the different applications. The detailed information please refer to 2.1.7 section. On normal work mode, if all used channels are open, the output of AP3039 will go high. Once the output voltage reaches the OV protection threshold, the AP3039 will turn off the external MOSFET and the system goes into disabled mode. The AP3039 will start to work after the output voltage drops below the OV protection threshold and the system goes into enabled mode again.

### 3.3.3 Open WLED Protection

The solution has the self-check and protection against open WLED. If any used WLED string opens, voltage on the corresponding CHX pin goes to zero and the FB pin of AP3608E exports the zero voltage to AP3039. So the boost converter controlled by AP3039 operates in open loop and the voltage on remainder CHX pin goes higher. Once the voltage on remainder CHX pin reaches the self-check voltage 3V, the AP3608E begins looking for the open string. After finding the open channel, AP3608E removes

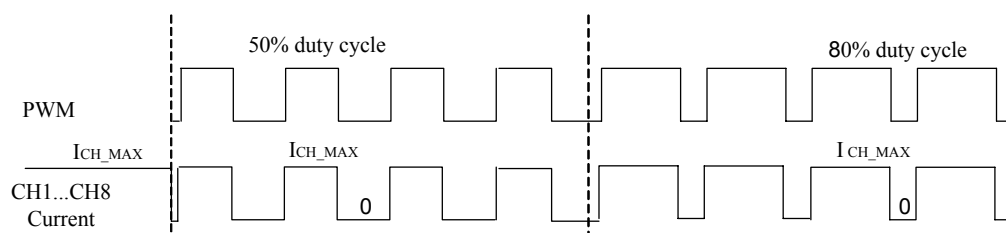


Figure 7. PWM Dimming Mode Example

the corresponding CHX pin from boost control loop, and then the boost circuit is controlled in the normal manner. Once the circuit returns normal operation, the voltage on the CHX pin is regulated to the normal level. It is necessary to pay attention that the open strings are removed from boost regulation, but not disabled. If the open WLED string is reconnected, it will sink current up to the programmed current level.

An example is shown in Figure 8. CH1, CH2 and CH3 are used channels while CH4 to CH8 are unused channels. If CH3 opens for any reason, the voltage on CH3 goes to zero. FB pin of AP3608E samples the lowest voltage of CH1, CH2 and CH3, so FB pin exports the zero voltage to AP3039 and AP3039 makes the output voltage go high. As a result, the voltage on CH1 and CH2 goes higher than normal value. Once either voltage of CH1 or voltage of CH2 pin reaches the self-check voltage 3V, the AP3608E begins looking for the open channel. After finding the open channel CH3, AP3608E removes the CH3 from boost control loop, and boost converter returns to normal operation. Once the system returns normal operation, the voltage on the CH1 and CH2 are regulated to the normal level.

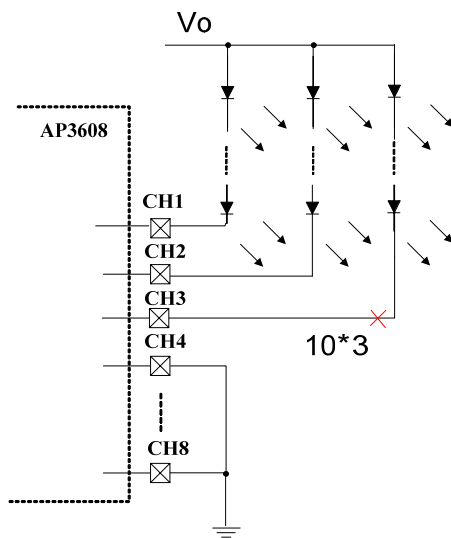


Figure 8

### 3.3.4 Short WLED Protection

The system can avoid destroy when some WLEDs are short. CH1 pin to CH8 pin of AP3608E can endure at least 30V high voltage. An example is shown in Figure 9, even though the WLEDs of CH3 are all short for any reason, AP3608E can still keep the safety.

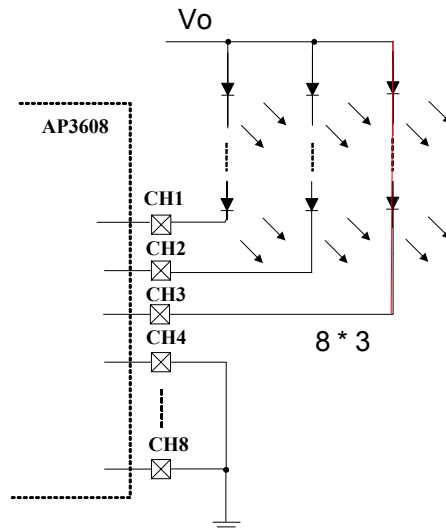


Figure 9

### 3.3.5 Over Temperature Protection

The solution has over temperature protection (OTP). Both AP3039 and AP3608E have the OTP circuit. The threshold of the OTP is typically 160°C, and the hysteresis of the OTP is typically 20°C.

### 3.3.6 Soft Start

The AP3039 in the solution has a soft start circuit to limit the inrush current during startup. The detailed information please refers to 2.1.9 section.

## 4. PCB Layout Guideline

Boost converter performance can be seriously affected by poor layout. To produce an optimal solution for medium LCD backlighting, good layout and design of the PCB are as important as the component selection. The following PCB layout guideline should be considered:

1. There are two high-current loops in the solution. One is the high-current input loop, and the other is the high-current output loop. The high-current input loop goes from the positive terminal of the  $C_{IN1}$  to the inductor, to the MOSFET, then to the current-sense resistor, and to the  $C_{IN1}$ 's negative terminal. The high-current output loop goes from the positive terminal of the  $C_{IN1}$  to the inductor, to the diode, to the positive terminal of the  $C_{OUT}$ , reconnecting between the  $C_{OUT}$  and the  $C_{IN1}$ 's ground terminals. Minimize the area of the two high-current loops to avoid excessive switching noise. The trace connected these two high-current loops must be short and thick.



2. Create two ground islands. One is called power ground island (PGND), the other is called analog ground island (AGND). PGND consists of  $C_{IN1}$  and  $C_{OUT}$  ground connections and negative terminal of the current-sense resistor  $R_{CS}$ . Maximizing the width of the PGND traces improves efficiency and reduces output voltage ripple and noise spike. AGND consists of the OV and UVLO detection-divider ground connection, the ISET and RT resistor ground connections,  $C_V$ ,  $C_{SS}$ ,  $C_C$  and  $C_{IN2}$  ground connections, and the device's exposed backside pad. Connect the AGND and the PGND directly to the exposed backside pad. Make no other connections between these separate ground planes.

3. Place the bypass capacitor  $C_V$  and  $C_{IN2}$  as close to the device as possible. The ground connection of these capacitors should be connected directly to AGND pins with a thick trace.

4. Keep the feedback trace away from the switching node, and make sure the feedback trace is short and thick. Place the OV and UVLO detection-divider resistors as close to the OV pin and UVLO pin as possible respectively. The divider's center trace should be kept short. Avoid running the sensing trace near switching node.