

PRODUCT/PROCESS CHANGE NOTICE (PCN)

<p>PCN Number: 05-21</p> <p>Date Issued: December 9, 2005</p> <p>Product(s) Affected: PI6C2509Q, PI6C2509-133</p> <p>Manufacturing Location Affected: Moving closed CSMS Fab 1 product to already approved CSMS Fab 2.</p> <p>Date Effective: March 9, 2006</p> <p><i>(Remaining Fab 1 inventory is now very limited. Immediate review by affected customers is requested).</i></p>	<p>Means of Distinguishing Changed Devices:</p> <p><input type="checkbox"/> Product Mark:</p> <p><input type="checkbox"/> Back Mark</p> <p><input checked="" type="checkbox"/> Date Code: Added letter code *</p> <p><input type="checkbox"/> Other</p> <p>* Product will have a letter "B" as the first character of the date code to signify CSMS Fab 2. All product samples should be identified this way.</p>
<p>Contact: Ed Mello</p> <p>Title: Director, Quality Systems</p> <p>Phone: (408) 435-0800, Ext. 207</p> <p>Fax: (408) 321-0324</p> <p>eMail: emello@pericom.com</p>	<p>Attachment: <input checked="" type="checkbox"/> Yes; <input type="checkbox"/> No</p> <p>No significant product features changed. Pericom Product and Design Engineering Characterization data confirmed Fab 2 devices should have no critical performance differences from Fab 1 products.</p> <p>Samples: Request from Sales.</p>
<p>Description and Purpose of Change:</p> <p>Product is transferring from approved wafer fab subcontractor Chartered Semiconductor Manufacturing Singapore's (CSMS) Fab 1, to the already approved Fab 2 facility. The devices use the same design and process type, and will be manufactured in Fab 2 with essentially the same qualified CMOS 0.5-µm SPDM process type as used in Fab 1. CSMS closed the older 150-mm wafer Fab 1 facility at the end of March 2004. Fab 2 will manufacture these Pericom products using 200-mm wafers. See CSMS website for more information:</p> <p>http://www.charteredsemi.com/media/corp/2003n/20030213.asp</p>	<p><input type="checkbox"/> Die Technology</p> <p><input checked="" type="checkbox"/> Wafer Fabrication</p> <p><input type="checkbox"/> Assembly Process</p> <p><input type="checkbox"/> Equipment</p> <p><input type="checkbox"/> Material</p> <p><input type="checkbox"/> Testing</p> <p><input type="checkbox"/> Manufacturing Site</p> <p><input type="checkbox"/> Data Sheet</p> <p><input checked="" type="checkbox"/> Other: CSMS Fab 1 closure, porting to Fab 2</p>
<p>Reliability/Qualification Summary: <i>Generic data using same process and design rules:</i> http://www.pericom.com/pdf/gen/rel_CSM2.pdf</p>	
<p>Customer Acknowledgement of Receipt:</p> <hr style="border-top: 1px dashed black;"/> <p>Customer: _____</p> <p>Name: _____</p> <p>Title: _____</p> <p>Date: _____</p> <p>E-Mail: _____</p> <p>Phone: _____</p> <p>Fax: _____</p> <p><input type="checkbox"/> Approval for shipments prior to effective date</p> <p>Customer Comments (Optional): _____</p>	

Table 1. PI6C2509Q DC Characteristics at 25C.

Parameter	Test Condition	Vcc V	CSM Fab2 Data	CSM Fab1 Data	Spec Limits
I _{in} (G, FB_IN, CLK_IN)	V _{in} =0V	3.6	0	-31 p	no spec limits
	V _{in} =3.6V	3.6	222 p	56 p	
	V _{in} =5.5V (5V tolerant)	3.6	145 p	--	
V _{il} max (G pin)	AV _{cc} = 0V, CLK_IN = V _{cc} , max V _{il} at G	3.0	1.410	1.355	max 0.8V
		3.3	1.570	1.505	
		3.6	1.735	1.660	
V _{ih} min (G pin)	AV _{cc} = 0V, CLK_IN = V _{cc} , min V _{ih} at G	3.0	1.415	1.360	min 2.0V
		3.3	1.575	1.510	
		3.6	1.740	1.665	
V _{il} max (CLK_IN pin)	AV _{cc} = 0V, G = V _{cc} , max V _{il} at CLK_IN	3.0	1.420	1.365	max 0.8V
		3.3	1.575	1.515	
		3.6	1.745	1.670	
V _{ih} min (CLK_IN pin)	AV _{cc} = 0V, G = V _{cc} , min V _{ih} at CLK_IN	3.0	1.425	1.370	min 2.0V
		3.3	1.580	1.520	
		3.6	1.750	1.675	
I _{oz} (Yx pins)	G=0, Pulldown resistance measured at V _{out} =0V	3.6	37.5 Ω	35.6 Ω	no spec limits
I _{ol}	AV _{cc} = 0V, V _{ol} = 0.55V AV _{cc} = 0V, V _{ol} = 0.80V	3.0	15.3 m	15.6 m	min 13mA
		3.0	21.8 m	22.4 m	min 19mA
I _{oh}	AV _{cc} = 0V, V _{oh} = 2.0V AV _{cc} = 0V, V _{oh} = 2.4V	3.0	-27.1 m	-25.8 m	max -22mA
		3.0	-16.9 m	-15.8 m	max -13.6mA
Static I _{cc} (Vcc pins only)	CLK_IN=0 or 1, G=0V, Yx outputs open, FB_OUT connected to FB_IN, V _{cc} =AV _{cc} =3.6V	3.6	2.2 n	3.0 u	max 10uA
Static I _{cca} (AVcc pin only)	CLK_IN=0 or 1, G=0V, Yx outputs open, FB_OUT connected to FB_IN, V _{cc} =AV _{cc} =3.6V	3.6	5.3 m	8.4 m	max 10uA

Equipment used: HP4145B, HP Power Supply & DMM

Table 2. PI6C2509Q output DC I_{ol} and I_{oh} at V_{cc}=3.0V, 25C, no spec limits.

Vol / Voh V	CSM Fab2		CSM Fab1	
	I _{ol}	I _{oh}	I _{ol}	I _{oh}
0	11.2 uA	-57.7 mA	-2 uA	-65.2 mA
0.25	7.11 mA	-55.9 mA	6.98 mA	-61.5 mA
0.50	14.0 mA	-53.6 mA	13.9 mA	-57.4 mA
0.75	20.6 mA	-50.7 mA	20.7 mA	-52.8 mA
1.00	26.7 mA	-47.2 mA	27.3 mA	-47.9 mA
1.25	32.2 mA	-43.0 mA	33.7 mA	-42.7 mA
1.50	37.1 mA	-38.2 mA	39.9 mA	-37.2 mA
1.75	41.2 mA	-32.9 mA	45.8 mA	-31.4 mA
2.00	44.4 mA	-27.1 mA	51.3 mA	-25.4 mA
2.25	46.7 mA	-20.8 mA	56.5 mA	-19.3 mA
2.50	48.2 mA	-14.2 mA	61.2 mA	-13.0 mA
2.75	49.0 mA	-7.3 mA	65.2 mA	-6.6 mA
3.00	49.4 mA	-50.2 uA	68.6 mA	-17.3 uA

Equipment used: HP4145B

Table 3. PI6C2509Q dynamic supply current at Vcc=3.6V, 25C, 30pF load at all 9 Yx outputs, FB_OUT connected to FB_IN with no external load, no spec limits.

CLK_IN Freq. MHz	CSM Fab2			CSM Fab1		
	Dynamic Supply Current Vcc pins only	Dynamic Supply Current AVcc pin only	Dynamic Supply Current Vcc & AVcc pins	Dynamic Supply Current Vcc pins only	Dynamic Supply Current AVcc pin only	Dynamic Supply Current Vcc & AVcc pins
25	37.8 mA	6.48 mA	44.7 mA	41.8 mA	7.95 mA	49.8 mA
33	49.3 mA	6.58 mA	56.2 mA	54.9 mA	8.13 mA	62.9 mA
66	101.1 mA	6.81 mA	107.8 mA	112.7 mA	8.83 mA	121.3 mA
100	159.9 mA	7.11 mA	166.3 mA	172.1 mA	9.70 mA	181.6 mA
133	193.5 mA	7.43 mA	200.4 mA	206.9 mA	10.75 mA	217.4 mA
150	199.2 mA	7.64 mA	206.2 mA	214.3 mA	11.32 mA	224.8 mA
170	195.2 mA	7.93 mA	202.6 mA	212.6 mA	12.09 mA	221.6 mA

Equipment used: HP Power Supply & DMM, HP81130A Pulse Generator, TEK TDS694C Scope with P6249 probes

Table 4. PI6C2509Q min and max input frequencies for PLL to lock, 25C, 30pF load at all 9 Yx outputs, FB_OUT connected to FB_IN with no external load.

Vcc V	CSM Fab2		CSM Fab1	
	Min CLK_IN Freq. for PLL to lock Spec = 25MHz	Max CLK_IN Freq. for PLL to lock Spec = 133MHz	Min CLK_IN Freq. for PLL to lock Spec = 25MHz	Max CLK_IN Freq. for PLL to lock Spec = 133MHz
3.0	7.5 Mhz	220 Mhz	1.1 Mhz	119 Mhz
3.3	8.5 Mhz	260 Mhz	1.2 Mhz	155 Mhz
3.6	9.2 Mhz	300 Mhz	1.2 Mhz	186 Mhz

Equipment used: HP Power Supply, HP81130A Pulse Generator, TEK TDS694C Scope with P6249 probes

Note: Jitter and phase error may be large and output swing may be small at these low & high freq. conditions.

Table 5. PI6C2509Q output rise and fall times, and duty cycle measured at 2Y2 on the PSC EV board, 25C, 30pF load at all 9 Yx outputs, FB_OUT connected to FB_IN with no external load.

CLK_IN Freq. MHz	Vcc V	CSM Fab2			CSM Fab1		
		Rise Time ns 0.4V to 2.0V no spec limits	Fall Time ns 2.0V to 0.4V no spec limits	Duty Cycle % at Vcc/2 spec=45 to 55%	Rise Time ns 0.4V to 2.0V no spec limits	Fall Time ns 2.0V to 0.4V no spec limits	Duty Cycle % at Vcc/2 spec=45 to 55%
25	3.0	1.448	1.846	48.9	1.502	1.610	49.3
	3.3	1.259	1.724	48.4	1.282	1.502	49.3
	3.6	1.149	1.614	48.4	1.122	1.413	49.4
50	3.0	1.419	1.866	48.8	1.513	1.598	48.4
	3.3	1.192	1.751	48.2	1.309	1.501	48.7
	3.6	1.162	1.640	47.7	1.152	1.417	48.8
100	3.0	1.417	2.051	48.3	1.506	1.603	48.7
	3.3	1.168	1.953	47.9	1.298	1.530	47.3
	3.6	0.965	1.829	47.6	1.142	1.456	47.7
133	3.0	1.521	2.036	48.4	**	**	**
	3.3	1.502	1.978	47.7	1.407	1.610	47.2
	3.6	1.296	1.893	46.9	1.229	1.513	47.6
150	3.0	1.825	2.007	47.9	**	**	**
	3.3	1.608	1.930	47.6	1.618	1.596	51.3
	3.6	1.368	1.886	47.0	1.461	1.509	49.6
170	3.0	2.049	1.906	46.4	**	**	**
	3.3	1.809	1.814	45.1	**	**	**
	3.6	1.625	1.703	44.4	1.468	1.526	45.8

Equipment used: HP Power Supply, HP81130A Pulse Generator, TEK TDS694C Scope with P6249 probes

** PLL does not lock

Table 6. PI6C2509Q max cycle-to-cycle jitters measured at Vcc/2 on 2Y2 rising edges, 25C, all Yx outputs 30pF load, FB_OUT connected to FB_IN with no external load. Spec limits = +/-100ps at 66MHz and 100MHz.

CLK_IN Freq. MHz	Vcc V	CSM Fab2		CSM Fab1	
		Cycle-to-cycle Jitter ps	Peak-Peak Jitter ps	Cycle-to-cycle Jitter ps	Peak-Peak Jitter ps
25	3.0	172	366	121	167
	3.3	174	483	116	162
	3.6	227	600	96	159
33.3	3.0	128	267	115	143
	3.3	122	362	105	142
	3.6	162	452	92	141
66.7	3.0	103	160	123	161
	3.3	93	144	110	153
	3.6	81	169	97	121
100	3.0	111	136	124	158
	3.3	91	126	114	143
	3.6	84	119	93	132
133.3	3.0	116	145	**	**
	3.3	99	127	134	165
	3.6	104	136	112	148
150	3.0	126	157	**	**
	3.3	103	135	136	201
	3.6	103	143	132	162
170	3.0	151	196	**	**
	3.3	116	159	**	**
	3.6	107	148	122	169

Equipment used: HP Power Supply, HP81130A Pulse Gen., TEK TDS694C Scope with P6249 probes and ASA M1

Table 7a. PI6C2509Q input to output mean delay measured from input CLK_IN rising edge at Vcc/2 to output rising edge at Vcc/2, and calculated output-to-output skew from the mean delay data, 25C, Part soldered on PSC EV board with 30pF load at all 9 Yx outputs, CLK_IN at 100MHz, **AVcc=Vcc for normal PLL mode**, FB_OUT connected to FB_IN with about 2-inch trace with no external load and not measured. Output-to-output skew max spec limit = 200ps.

Output Measured	CSM Fab2			CSM Fab1		
	Mean Delay ps PLL mode	Mean Delay ps PLL mode	Mean Delay ps PLL mode	Mean Delay ps PLL mode	Mean Delay ps PLL mode	Mean Delay ps PLL mode
	AVcc=Vcc=3.0V	AVcc=Vcc=3.3V	AVcc=Vcc=3.6V	AVcc=Vcc=3.0V	AVcc=Vcc=3.3V	AVcc=Vcc=3.6V
1Y0	288	290	284	255	250	246
1Y1	306	307	308	316	303	306
1Y2	289	291	299	269	266	272
1Y3	264	267	271	217	203	196
1Y4	262	267	268	252	241	234
2Y3	274	275	269	161	146	151
2Y2	252	255	252	157	148	146
2Y1	264	270	270	155	145	138
2Y0	272	271	277	119	105	103
Mean Delay	275	277	278	211	201	199
Min Delay	252	255	252	119	105	103
Max Delay	306	307	308	316	303	306
Output-to-output skew, ps	54	52	56	197	198	203

Equipment used: HP Power Supply, HP81130A Pulse Generator, TEK TDS694C Scope with P6249 probes and ASA M1

Table 7b. PI6C2509Q input to output mean delay measured from input CLK_IN rising edge at Vcc/2 to output rising edge at Vcc/2, and calculated output-to-output skew from the mean delay data, 25C. Part soldered on PSC EV board with 30pF load at all 9 Yx outputs, CLK_IN at 100MHz, AVcc=0V for buffer mode, FB_OUT connected to FB_IN with about 2-inch trace with no external load and not measured. Output-to-output skew max spec limit=200ps.

Output Measured	CSM Fab2			CSM Fab1		
	Mean Delay, ps	Mean Delay, ps	Mean Delay, ps	Mean Delay, ps	Mean Delay, ps	Mean Delay, ps
	Buffer mode AVcc=0V Vcc=3.0V	Buffer mode AVcc=0V Vcc=3.3V	Buffer mode AVcc=0V Vcc=3.6V	Buffer mode AVcc=0V Vcc=3.0V	Buffer mode AVcc=0V Vcc=3.3V	Buffer mode AVcc=0V Vcc=3.6V
1Y0	3821	3661	3543	6422	6018	5704
1Y1	3842	3678	3568	6481	6068	5760
1Y2	3826	3667	3556	6558	6212	5895
1Y3	3806	3645	3537	6384	5975	5663
1Y4	3810	3648	3536	6407	6008	5694
2Y3	3820	3660	3525	6315	5921	5615
2Y2	3807	3643	3512	6307	5915	5605
2Y1	3815	3651	3532	6311	5929	5607
2Y0	3812	3594	3534	6266	5887	5560
Mean Delay	3818	3650	3538	6383	5993	5678
Min Delay	3806	3594	3512	6266	5887	5560
Max Delay	3842	3678	3568	6558	6212	5895
Output-to-output skew, ps	36	84	56	292	325	335

Equipment used: HP Power Supply, HP81130A Pulse Gen, TEK TDS694C Scope with P6249 probes and ASA M1

Table 8. PI6C2509Q static & dynamic phase errors measured from CLK_IN input to FB_IN at the pins at Vcc/2 of rising edges, 25C, all 9 Yx outputs 30pF load, FB_OUT connected to FB_IN with a short jump wire and no external load. Static phase error spec limits = +/- 150ps at 66MHz and 100MHz.

CLK_IN Freq. MHz	Vcc V	CSM Fab2				CSM Fab1			
		BX0342OC Static Phase Error ps	BX0342OC Min Phase Error ps	BX0342OC Max Phase Error ps	BX0342OC Dynamic Phase Error ps	AY0322 Static Phase Error ps	AY0322 Min Phase Error ps	AY0322 Max Phase Error ps	AY0322 Dynamic Phase Error ps
		25	3.0	123	-91	346	574	178	63
	3.3	136	-126	401	615	187	71	301	281
	3.6	140	-238	499	824	187	77	295	263
33.3	3.0	128	-41	301	418	189	107	273	188
	3.3	143	-64	368	549	195	103	286	208
	3.6	147	-144	453	708	197	111	284	206
66.7	3.0	110	16	205	224	153	97	218	145
	3.3	128	6	248	308	164	110	215	127
	3.6	131	-48	313	426	166	113	219	119
100	3.0	128	66	180	138	179	120	237	143
	3.3	148	80	219	180	192	145	239	110
	3.6	150	71	225	195	179	138	216	97
133.3	3.0	89	44	139	107	**	**	**	**
	3.3	113	61	165	125	131	82	180	114
	3.6	117	63	171	130	145	108	184	94
150	3.0	117	69	165	115	**	**	**	**
	3.3	149	105	191	95	152	79	279	200
	3.6	143	91	200	120	182	145	220	94

Equipment used: HP Power Supply, HP81130A Pulse Gen., TEK TDS694C Scope with P6249 probes and ASA M1

** PLL does not lock