



3545 North First St. • San Jose, CA 95134 • USA

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN Number: **05-11**
 Date Issued: **May 6, 2005**
 Product(s) Affected: **PI6C2408-1H**
 Manufacturing Location Affected: **Moving this CSMS Fab 1 product to already approved CSMS Fab 2.**
 Date Effective: **August 5, 2005**
(Remaining Fab 1 inventory is very limited. Immediate review by affected customers is requested).

Means of Distinguishing Changed Devices:
 Product Mark:
 Back Mark
 Date Code: **Added letter code ***
 Other
 * Product will have a letter "B" as the first character of the date code to signify CSMS Fab 2. All product samples should be identified this way.

Contact: **Ed Mello**
 Title: **Director, Quality Systems**
 Phone: **(408) 435-0800, Ext. 207**
 Fax: **(408) 321-0324**
 eMail: emello@pericom.com

Attachment: Yes; No
No significant product features changed. Pericom Product and Design Engineering Characterization data confirmed Fab 2 devices should have no critical performance differences from Fab 1 products.
 Samples: **Request from Sales.**

Description and Purpose of Change:
Product is transferring from approved wafer fab subcontractor Chartered Semiconductor Manufacturing Singapore's (CSMS) Fab 1, to the already approved Fab 2 facility. The devices use the same design and process type, and will be manufactured in Fab 2 with essentially the same qualified CMOS 0.5-µm SPDM process type as used in Fab 1. CSMS closed the older 150-mm wafer Fab 1 facility at the end of March 2004. Fab 2 will manufacture these Pericom products using 200-mm wafers. See CSMS website for more information:
<http://www.charteredsemi.com/media/corp/2003n/20030213.asp>

Die Technology
 Wafer Fabrication
 Assembly Process
 Equipment
 Material
 Testing
 Manufacturing Site
 Data Sheet
 Other: **CSMS Fab 1 closure, porting to Fab 2**

Reliability/Qualification Summary: *Generic data using same process and design rules:* http://www.pericom.com/pdf/gen/rel_CSM2.pdf

Customer Acknowledgement of Receipt:

Customer: _____

Name: _____

Title: _____

Date: _____

E-Mail: _____

Phone: _____

Fax: _____

Approval for shipments prior to effective date

Customer Comments (Optional): _____



Confidential/For Customer Use Only

Date: March 9, 2005

Subject: PI6C2408-1H CSM Fab1 and Fab2 Characterization Comparison Report

Reference:

Process: CSM Fab 2, 0.5um 3.3V CMOS

Date Code: BX05080C

Lot #: MA31344.4A

Package: W16

Process: CSM Fab 1, 0.5um 3.3V CMOS

Date Code: U03330C

WO/Lot#: 230056

Package: W16

Equipment:

TEK TDS694C with P6249 probe & ASA M1

HP8082A Pulse Generator

HP8116A Function Generator

R & S Signal Generator SMY01

HP4145B

HP TIA

HP Power Supply

EV boards

Test Results:

Table 1. PI6C2408-1H DC Characteristics at 25C.

Parameter	Test Condition	Vdd V	CSM Fab1	CSM Fab2	Limit Min	Limit Max
V _{ol}	I _{ol} = 12mA	3.0	0.214V	0.212V		0.4V
V _{oh}	I _{oh} = -12mA	3.0	2.730V	2.780V	2.4V	
I _{oz} (OUTA _x & OUTB _x)	SEL1=SEL2=0, V _{out} = 3.6V SEL1=SEL2=0, V _{out} = 0V Pull-down resistance measured at 0V	3.6	112.3uA -773.4nA 11.8Kohms	109.2uA 96.41nA 12.6Kohms		
V _{il} max* (CLKIN)	SEL1=0, SEL2=1, max CLKIN input dc low level for outputs to switch from high to low	3.0 3.3 3.6	1.41V 1.56V 1.63V	1.30V 1.42V 1.53V		0.8V
V _{ih} min+ (CLKIN)	SEL1=0, SEL2=1, min CLKIN input dc high level for outputs to switch from low to high	3.0 3.3 3.6	1.44V 1.64V 1.78V	1.48V 1.66V 1.84V	2.0V	
V _{il} max* (SEL2)	SEL1=1, CLKIN at 67MHz, max SEL2 input dc low level for OUTB _x outputs to switch from PLL lock mode to Hi-Z	3.0 3.3 3.6	1.33V 1.46V 1.58V	1.34V 1.48V 1.64V		0.8V
V _{ih} min+ (SEL2)	SEL1=1, CLKIN at 67MHz, min SEL2 input dc high level for OUTB _x outputs to switch from Hi-Z to PLL lock mode	3.0 3.3 3.6	1.45V 1.62V 1.79V	1.44V 1.61V 1.80V	2.0V	
I _{off} (CLKIN)	V _{in} = 3.6V V _{in} = 5.5V (5V tolerant)	0	84pA 108pA	186pA 242pA		
I _{il} (CLKIN)	V _{in} = 0V Pull-down resistance measured at 0V	3.6	-50.30nA 11.7Kohms	63.08nA 19.0Kohms		
I _{ih} (CLKIN)	V _{in} = 3.6V V _{in} = 5.5V (5V tolerant)	3.6	114.5uA 114.6uA	72.23uA 72.42uA		
I _{il} (SEL _x)	V _{in} = 0V Pull-up resistance measured at 3.6V	3.6	-5.684uA 211Kohms	-3.405uA 124Kohms		
I _{ih} (SEL _x)	V _{in} = 3.6V	3.6	5.897nA	-14.80nA		
I _{in} (FB_IN)	V _{in} = 0V V _{in} = 3.6V	3.6	-4pA 29pA	-83pA 91pA		

Equipment used: HP4145B, HP8082A Pulse Gen., TEK TDS694C scope & P6249 probes, HP Power Supply.

Note: * measured V_{il} value must be greater than Max. limit. + measured V_{ih} value must be less than Min. limit.

Table 2. PI6C2408-1H DC Iol and Ioh at Vdd = 3.0V, 25C.

Vol / Voh V	CSM Fab1 Iol, mA	CSM Fab2 Iol, mA	CSM Fab1 Ioh, mA	CSM Fab2 Ioh, mA
0	0	0	-61.57	-74.66
0.5	26.52	26.78	-59.43	-71.56
1.0	45.72	46.54	-56.38	-67.30
1.5	55.79	57.49	-50.39	-59.68
2.0	58.94	61.50	-39.03	-46.15
2.5	59.54	62.44	-21.74	-25.95
3.0	59.62	62.61	0	0

Equipment used: HP4145B.

Table 3. PI6C2408-1H Peak-to-peak Supply Current at Vdd = 3.6V, 25C, closed loop operation.

CLKIN Freq. MHz	CSM Fab1 Idd, mA (15pF load)	CSM Fab2 Idd, mA (15pF load)
66.7	78	80
133	184	181
140	190	188

Equipment used: HP Power Supply, HP8082A Pulse Gen., TEK TDS694C scope & P6249 probes.

Table 4. PI6C2408-1H Min Vdd for PLL to lock at different frequencies, 25C. Closed loop operation

CLKIN Freq. MHz	CSM Fab1 Min Vdd, V for PLL to lock (15pF load)	CSM Fab2 Min Vdd, V for PLL to lock (15pF load)
66.7	2.49	2.06
133.3	2.54	2.20

Equipment used: HP8082A Pulse Gen., TEK TDS694C Scope & P6249 probes, HP Power Supply.

Note: Part may have large phase errors and jitters and small output swings at these low Vdd conditions, but the outputs still track input.

Table 5. PI6C2408-1H Min and Max Frequencies at 25C, all 8 outputs loaded with 15pF. Closed loop operation.

Vdd V	CSM Fab1 Min Freq., MHz, for PLL to lock (15pF load)	CSM Fab2 Min Freq., MHz, for PLL to lock (15pF load)	CSM Fab1 Max Freq., MHz, for PLL to lock (15pF load)	CSM Fab2 Max Freq., MHz, for PLL to lock (15pF load)
3.0	2.8	1.4	209	162
3.3	3.0	1.5	251	162
3.6	3.3	1.6	266	162

Equipment used: HP8082A Pulse Gen., TEK TDS694C Scope & P6249 probes, HP Power Supply.

Note: Part may have somewhat large phase errors and jitters at these min & max freq conditions, but the outputs still track input.

Table 6. PI6C2408-1H output rise and fall times, and duty cycle measured at OUTB3, 25C, all 8 outputs 15pF load, Closed loop operation.

CLKI N Freq. MHz	Vdd V	CSM Fab1 trise, ns 0.8V to 2.0V	CSM Fab2 trise, ns 0.8V to 2.0V	Limit Max ns	CSM Fab1 tfall, ns 2.0V to 0.8V	CSM Fab2 tfall, ns 2.0V to 0.8V	Limit Max ns	CSM Fab1 Duty Cycle, % at Vdd/2	CSM Fab2 Duty Cycle, % at Vdd/2	Limit Min – Max %
66.67	3.0	1.127	0.785	1.5	0.970	0.814	1.25	51.36	51.80	45-55
	3.3	0.879	0.644		0.860	0.700		51.19	51.66	
	3.6	0.696	0.559		0.763	0.615		50.92	51.80	
133.33	3.0	1.290	0.947	1.5	0.570	0.755	1.25	42.94	54.71	40-60
	3.3	1.106	0.760		0.528	0.675		43.95	54.53	
	3.6	0.932	0.632		0.485	0.599		44.39	54.23	
140	3.0	1.322	0.916	1.5	0.583	0.727	1.25	42.75	55.52	40-60
	3.3	1.122	0.695		0.534	0.653		44.45	55.83	
	3.6	0.930	0.582		0.493	0.581		45.17	55.83	

Equipment used: HP8082A Pulse gen., HP Power Supply, TEK TDS694C Scope & P6249 probes.

Table 7. PI6C2408-1H max Cycle-to-cycle Jitters measured at OUTB3 rising edge at Vdd/2, 25C, SSC off and on with 50KHz triangular modulation and +/-0.5% freq spread, closed loop operation, 15pF load at all 8 outputs.

CLKIN Freq. MHz	Vdd V	CSM Fab1 Max Cycle-to-cycle Jitter, ps SSC Off	CSM Fab2 Max Cycle-to-cycle Jitter, ps SSC Off	CSM Fab1 Max Cycle-to-cycle Jitter, ps SSC On	CSM Fab2 Max Cycle-to-cycle Jitter, ps SSC On	Limit Max Ps
66.67	3.0	128	84	114	83	150
	3.3	123	94	144	93	
	3.6	106	84	102	80	
140	3.0	149	81	146	84	150
	3.3	148	108	148	104	
	3.6	129	99	129	93	

Equipment used: HP8082A Pulse gen., HP8116A Fun. Gen., R & S Signal Gen. SMY01, HP Power Supply, TEK TDS694C Scope & P6249 probes & M1.

Table 8. PI6C2408-1H input to output mean delays measured from CLKIN rising edge at Vdd/2 to OUTx rising edge at Vdd/2, no SSC, 25C, closed loop operation, 15pF load at all 8 outputs.

Output Freq. MHz	Output Load pF	Output measured	CSM Fab1 tpd, ps Vdd=3.0V	CSM Fab1 tpd, ps Vdd=3.6V	CSM Fab2 tpd, ps Vdd=3.0V	CSM Fab2 tpd, ps Vdd=3.6V	Limit Max ps
66.67	33	OUTA1	-473	-402	-627	-563	900
		OUTA2	-354	-286	-614	-553	900
		OUTA3	-462	-412	-615	-552	900
		OUTA4	-418	-309	-534	-459	900
		OUTB1	-407	-328	-674	-583	900
		OUTB2	-401	-318	-654	-564	900
		OUTB3	-542	-447	-625	-548	900
		OUTB4	-533	-445	-635	-546	900
133.3	15	OUTA1	-396	-378	-713	-607	900
		OUTA2	-297	-276	-696	-597	900
		OUTA3	-524	-500	-705	-618	900
		OUTA4	-388	-343	-701	-563	900
		OUTB1	-314	-288	-754	-655	900
		OUTB2	-370	-344	-759	-660	900
		OUTB3	-444	-416	-717	-600	900
		OUTB4	-480	-447	-684	-595	900

Equipment used: HP8082A Pulse gen., HP Power Supply, TEK TDS694C Scope & P6249 probes & M1.

Table 9. PI6C2408-1H output to output skews tsk(o) measured at Vdd/2 of rising edge, 25C closed loop operation.

Output Freq. MHz	Output Load pF	Output measured	CSM Fab1 tsk(o), ps Vdd=3.0V	CSM Fab1 tsk(o), ps Vdd=3.6V	CSM Fab2 tsk(o), ps Vdd=3.0V	CSM Fab2 tsk(o), ps Vdd=3.6V	Limit Max ps
66.67	33	OUTAx	119	126	93	104	250
		OUTBx	141	129	49	37	250
		all 8	188	161	140	124	250
133.3	15	OUTAx	227	224	17	55	250
		OUTBx	166	159	75	65	250
		all 8	227	224	75	97	250

Equipment used: HP8082A Pulse gen., HP Power Supply, TEK TDS694C Scope & P6249 probes & M1.