3545 North First St. • San Jose, CA 95134 • USA

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN Number: **04-08**

Date Issued: **April 30, 2004**

Product(s) Affected: **PI74LPT16240; PI74LCX16240**
PI74LPT16373; PI74LCX16373
PI74LPT16374; PI74LCX16374

Manufacturing Location Affected: **Moving these CSMS Fab 1 products to already approved CSMS Fab 2.**

Date Effective: **July 30, 2004 (calendar week 31).**
(Any remaining Fab 1 inventory may ship until depleted).

Means of Distinguishing Changed Devices:

☐ Product Mark:

☐ Back Mark

☒ Date Code: **Added letter code** *

☐ Other

* **Product will have a letter "B" as the first character of the date code to signify CSMS Fab 2. All product samples should be identified this way.**

Contact: **Ed Mello**

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Attachment: ☒ Yes; ☐ No

No significant product features changed. Pericom Product and Design Engineering Characterization data confirmed devices from Fab 2 should have no critical performance differences than products produced in Fab 1.

Samples: **Available upon request to Sales**

Description and Purpose of Change:

Products are transferring from approved wafer fab subcontractor Chartered Semiconductor Manufacturing Singapore's (CSMS) Fab 1, to the already approved Fab 2 facility. These devices use the same base array die, design and process, and will be manufactured in Fab 2 with essentially the same qualified CMOS 0.5-µm SPDM process type as used in Fab 1. CSMS closed the older 150-mm wafer Fab 1 facility at the end of March 2004. Fab 2 will manufacture these Pericom products using 200-mm wafers. See CSMS website for more information:

http://www.charteredsemi.com/media/corp/2003n/20030213.asp

☐ Die Technology

☒ Wafer Fabrication

☐ Assembly Process

☐ Equipment

☐ Material

☐ Testing

☐ Manufacturing Site

☐ Data Sheet

☒ Other: **CSMS Fab 1 closure, porting to Fab 2**

Reliability/Qualification Summary: **See page 7**

Customer Acknowledgement of Receipt:

Customer: ______

Name: ______

Title: ______

Date: ______

E-Mail: ______

Phone: ______

Fax: ______

☐ Approval for shipments prior to effective date
Customer Comments (Optional): ______

PERICOM
Semiconductor Corporation

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Date: April 21, 2004

Subject: PI74LCX16374 Full Characterization Report

Introduction:

The PI74LCX16374 is a Fast CMOS, 3.3V, 16-Bit register. The new array from CSMS Fab 2 is compared side by side with the older array from CSMS Fab 1 facility. The PI74LCX16374 data is representative of other products in this family, the PI74LPT16374, the PI74LCXPI74LPT16373 and PI74LCX16240/PI74LPT16240 device types.

Reference:

Fab 2 Array: F832
Fab Process: CMOS 0.5 µm SPDM, 3.3v
Lot #: EA08056.2A
Date Code: BZBJ0413OC
Package: TSSOP (A48)

Fab 1 Array: ALVCH48
Fab Process: CMOS 0.5 µm, SPDM, 3.3V
Date Code: AZL30301AOC
Lot number: EY97475.4
Package: TSSOP (A48)

Data Sheet:

PS2090B (09/19/02)

Equipment:

TSSOP Re-Configurable Test Board
HP power supply & DMM,
HP4145B DC Analyzer
HP4285A LCR Meter
TDS8000 Oscilloscope
HP8110A Pulse Generator
HP8082A Pulse Generator
Thermostream Temperature Probe

Tables:

Table 1. DC characteristics
Table 2. AC Characteristics (Using regular PCB)
Table 3. Maximum Clock Frequency
Table 4. Timing Requirements, 25C
Table 5-6. Propagation delay of all path (Using 64-pin Re-configurable EV Board), 25C
Table 7. Input Capacitance and Cpd
Table 8. Dynamic Icc at 25C

Conclusion:

1. Both parts meet all data sheet specifications.
2. The new array has a stronger output drive.
3. The new array has faster low-to-high transition, and enable/disable time.
4. High-to-low transition is similar for both arrays.

Table 1. DC characteristics

			CSMS Fab 2			CSMS Fab 1					
Para-meter	**Test Conditions**	**Vcc**	**-10°C**	**25°C**	**90°C**	**-10°C**	**25°C**	**90°C**	**Min Spec**	**Max Spec**	**unit**
VIH*	Input High Voltage	2.7 V	1.205	1.215	1.240	1.180	1.190	1.210	2.0		V
VIH*	Input High Voltage	3.0 V	1.355	1.370	1.390	1.325	1.335	1.360	2.0		V
VIH*	Input High Voltage	3.3 V	1.510	1.525	1.550	1.470	1.480	1.510	2.0		V
VIH*	Input High Voltage	3.6 V	1.665	1.680	1.705	1.620	1.630	1.660	2.0		V
VIL*	Input Low Voltage	2.7 V	1.260	1.270	1.290	1.240	1.250	1.265		0.8	V
VIL*	Input Low Voltage	3.0 V	1.415	1.425	1.445	1.385	1.395	1.415		0.8	V
VIL*	Input Low Voltage	3.3 V	1.570	1.580	1.600	1.535	1.550	1.570		0.8	V
VIL*	Input Low Voltage	3.6 V	1.730	1.735	1.760	1.690	1.700	1.720		0.8	V
VOH	IOH=-12mA	2.7 V	2.50	2.48	2.46	2.46	2.44	2.40	2.2		V
VOH	IOH=-18mA	3.0 V	2.73	2.69	2.66	2.67	2.61	2.59	2.4		V
VOH	IOH=-24mA	3.0 V	2.63	2.58	2.53	2.55	2.47	2.44	2.2		V
VOL	IOL= 12mA	2.7 V	0.11	0.12	0.14	0.12	0.13	0.15		0.4	V
VOL	IOL= 16mA	3.0 V	0.15	0.16	0.18	0.15	0.18	0.19		0.4	V
VOL	IOL= 24mA	3.0 V	0.22	0.25	0.28	0.23	0.27	0.29		0.55	V
IIN	Vin= 0 V	3.6 V	11 p	23 p	21 p	-608 p	165 p	348 p		5	µ A
IIN	Vin= 3.6 V	3.6 V	46 p	98 p	2.2 n	-691 p	527 p	594 p		5	µ A
IIN	Vin= 5.5 V	3.6 V	43 p	129 p	3.1 n	-501 p	-231 p	1.7 n		5	µ A
Ioff	Vout= 0 V	0 V	-9.2 p	22 p	28 p	-155 p	696 p	707 p		5	µ A
Ioff	Vout= 3.6 V	0 V	42 p	140 p	2.7 n	-279 p	501 p	696 p		5	µ A
Ioff	Vout= 5.5 V	0 V	69 p	247 p	5.1 n	604 p	290 p	2.1 n		5	µ A
VIK	Iin=-18mA, /OE, D	2.7 V	-0.83	-0.79	-0.74	-0.86	-0.82	-0.76		-1.2	V
VIK	Iin=-18mA, x0x pin	2.7 V	-0.83	-0.79	-0.74	-0.84	-0.81	-0.73		-1.2	V
IOZ	Vout= 0 V	3.6 V	-45 p	-75 p	-863 p	-173 p	512 p	226 p		5	µ A
IOZ	Vout= 3.6 V	3.6 V	60 p	78 p	2.6 n	228 p	478 p	596 p		5	µ A
IOZ	Vout= 5.5 V	3.6 V	65 p	104 p	3.9 n	653 p	22 p	1.2 n		5	µ A
ICCL	Vin=0V	3.6 V	1.2 n	3.7 n	57 n	105 p	1.1 n	30.2 n		10	µ A
ICCH	Vin=3.6 V	3.6 V	321 p	1.8 n	56 n	-1.7 n	4.3 n	39.1 n		10	µ A
ΔICC	Vin=Vcc-0.6V	3.6 V	1.3 µ	3.6 µ	18.7 µ	55 n	369 n	3.6 µ		500	µ A

***Note: VIH/VIL Test Measurement Definition**

The Table 1 DC parametric data for VIH and VIL reflects the input switching threshold data for logic devices. When the measured value is compared to the VIH min or VIL max limits, the difference is the noise margin for that device's input; it does not mean the device is out of spec. This is a standard methodology for doing this type of design parameter test.

Table 2. AC Characteristics (Using regular double-sided board)

			CSMS Fab 2			CSMS Fab 1				
Symbol	**Vcc**	**Load**	**-10°C**	**25°C**	**90°C**	**-10°C**	**25°C**	**90°C**	**Max Spec**	**Units**
tpLH	2.7 V	50pF// 500Ω to Gnd	2.69	2.84	3.13	3.36	3.57	4.03	6.5	nS
tpHL	2.7 V	50pF// 500Ω to Gnd	2.70	2.89	3.19	2.72	2.88	3.28	6.5	nS
tpLH	3.0 V	50pF// 500Ω to Gnd	2.41	2.54	2.83	2.91	3.08	3.47	6.2	nS
tpHL	3.0 V	50pF// 500Ω to Gnd	2.78	2.97	3.32	2.72	2.88	3.27	6.2	nS
tpZH	2.7 V	50pF// 500Ω // 500Ω	2.73	2.87	3.16	3.49	3.66	4.03	6.3	nS
tpHZ	2.7 V	50pF// 500Ω // 500Ω	3.26	3.39	3.62	3.45	3.62	3.90	6.2	nS
tpZH	3.0 V	50pF// 500Ω // 500Ω	2.33	2.42	2.69	2.84	3.01	3.35	6.1	nS
tpHZ	3.0 V	50pF// 500Ω // 500Ω	2.96	3.10	3.39	3.12	3.27	3.52	6.0	nS
tpZL	2.7 V	50pF// 500Ω to Gnd	3.16	3.33	3.75	3.14	3.33	3.74	6.3	nS
tpLZ	2.7 V	500Ω to 6V	2.94	3.05	3.22	3.20	3.37	3.60	6.2	nS
tpZL	3.0 V	50pF// 500Ω to Gnd	2.67	2.84	3.15	2.56	2.78	3.22	6.1	nS
tpLZ	3.0 V	500Ω to 6V	2.90	3.00	3.24	3.09	3.26	3.46	6.0	nS

- tpd and enable timing are measured from 1.5V input to 1.5V output

-disable timing is measured from 1.5V input to VOH / VOL ± 0.3V

Table 3. Maximum Clock Frequency

Symbol	**Vcc**	**Load**	**CSMS Fab 2**	**CSMS Fab 1**	**Spec**
f_{MAX}	2.70 V	50pF// 500Ω to Gnd	189	229	170 Mhz
f_{MAX}	3.00 V	50pF// 500Ω to Gnd	194	271	170 Mhz

*Input signals from DG2040 Data Generator

-output must meet 45%/55% duty cycle

Table 4. Timing Requirements, 25C

Parameter	**Vcc**	**CSMS Fab 2**	**CSMS Fab 1**	**Min**	**Units**
SETUP, Data(High) before CLK↑	2.7V	0.43	0.56	2.5	ns
SETUP, Data(Low) before CLK↑	2.7V	1.11	1.29	2.5	ns
SETUP, Data(High) before CLK↑	3.0V	0.53	0.54	2.5	ns
SETUP, Data(Low) before CLK↑	3.0V	0.85	1.06	2.5	ns
HOLD, Data(High) after CLK↑	2.7V	-0.79	-1.00	1.5	ns
HOLD, Data(Low) after CLK↑	2.7V	-0.19	-0.26	1.5	ns
HOLD, Data(High) after CLK↑	3.0V	-0.51	-0.74	1.5	ns
HOLD, Data(Low) after CLK↑	3.0V	-0.15	-0.28	1.5	ns

Table 5. Propagation delay of all outputs, Vcc=3.0V, 25C

	CSMS Fab 2		CSMS Fab 1	
Path	**LH , nS**	**HL , nS**	**LH , nS**	**HL, nS**
Clk1 – 1O0	2.50	2.89	2.91	2.77
Clk1 – 1O1	2.52	2.93	2.93	2.79
Clk1 – 1O2	2.48	2.90	2.87	2.80
Clk1 – 1O3	2.45	2.91	2.84	2.82
Clk1 – 1O4	2.44	2.91	2.83	2.80
Clk1 – 1O5	2.45	2.89	2.83	2.79
Clk1 – 1O6	2.42	2.82	2.82	2.74
Clk1 – 1O7	2.42	2.84	2.83	2.74
Clk2 – 2O0	2.40	2.90	2.77	2.67
Clk2 – 2O1	2.39	2.86	2.76	2.66
Clk2 – 2O2	2.38	2.87	2.74	2.68
Clk2 – 2O3	2.36	2.93	2.71	2.69
Clk2 – 2O4	2.41	2.71	2.74	2.71
Clk2 – 2O5	2.39	2.70	2.75	2.70
Clk2 – 2O6	2.43	2.71	2.78	2.71
Clk2 – 2O7	2.49	2.73	2.82	2.73
Skew	**0.16**	**0.23**	**0.22**	**0.16**

- TSSOP Generic Board is used in this test
- Load=50pF//500 Ohm at the end of the trace line

Table 6. Propagation delay of all outputs, Vcc=2.7V, 25C

	CSMS Fab 2		CSMS Fab 1	
Path	**LH , nS**	**HL , nS**	**LH , nS**	**HL, nS**
Clk1 – 1O0	2.75	2.80	3.34	2.73
Clk1 – 1O1	2.77	2.85	3.37	2.77
Clk1 – 1O2	2.71	2.81	3.26	2.76
Clk1 – 1O3	2.68	2.83	3.22	2.80
Clk1 – 1O4	2.67	2.82	3.20	2.77
Clk1 – 1O5	2.69	2.80	3.24	2.76
Clk1 – 1O6	2.66	2.76	3.21	2.72
Clk1 – 1O7	2.67	2.76	3.22	2.72
Clk2 – 2O0	2.65	2.73	3.17	2.65
Clk2 – 2O1	2.63	2.71	3.14	2.64
Clk2 – 2O2	2.63	2.72	3.14	2.66
Clk2 – 2O3	2.60	2.73	3.11	2.64
Clk2 – 2O4	2.61	2.77	3.11	2.68
Clk2 – 2O5	2.64	2.75	3.13	2.66
Clk2 – 2O6	2.68	2.77	3.15	2.67
Clk2 – 2O7	2.73	2.84	3.24	2.70
Skew	**0.17**	**0.14**	**0.26**	**0.16**

- TSSOP Generic Board is used in this test
- Load=50pF//500 Ohm at the end of the trace line

Table 7. Input Capacitance and Cpd

Para-meter	Test Conditions	Vcc	CSMS Fab 2	CSMS Fab 1	Typ Spec	unit
Cin	Data Input, 1D1	3.3 V	3.1	3.3	7	pF
Cin	Control Input, /OE1	3.3 V	3.0	3.2	7	pF
Cin	Control Input, CLK	3.3 V	3.0	3.2	7	pF
Cout	Output, 1O1	3.3 V	4.5	4.9	8	pF
Cpd	Iccd=(Cpd)(Vcc)fin	2.7 V	15.6	14.8	20	pF
Cpd	Iccd=(Cpd)(Vcc)fin	3.3 V	19.3	16.4	20	pF

Table 8. Dynamic Icc at 25C

	CSMS Fab 2		CSMS Fab 1		
Frequency	**Vcc=2.7V**	**Vcc=3.3V**	**Vcc=2.7V**	**Vcc=3.3V**	**Units**
1MHZ	0.042	0.064	0.040	0.054	mA
5MHZ	0.207	0.314	0.200	0.267	mA
10MHZ	0.413	0.631	0.399	0.533	mA
20MHZ	0.825	1.258	0.797	1.064	mA

*one output switching without load

Date: October 17, 2003

Subject: Pericom Reliability Qualification – CSM-S Fab 2's 0.5 µm Process – SiliconClock

Chartered Semiconductor Manufacturing – Singapore Fab 2's CMOS, 3.3 volt, 0.50-µm process was recently qualified to Pericom's standard die level process qualification requirements for our SiliconClock family of Zero Delay (ZD) Clock Driver and Buffer products. CSM-S Fab 1 will be closing in March of 2004, so this is part of a continuing process to transfer products currently using similar CMOS, SPDM processes on 150 mm wafers to their Fab 2 facility. Fab 2 uses an equivalent 0.5-µm CMOS, SPDM process on 200-mm wafers. A sample of 130 units from a representative lot of our PI6C2510-133 device type has already successfully completed 2000 hours of Dynamic High Temperature Operating Life (DHTOL) test with no failures at 150°C and 3.6 volts applied bias. It will complete 3000 hours on October 31. This device type was used as the qualification vehicle since it's one of the more complex of our ZD Clock Driver and Buffer products. Therefore, all products using this process technology and design rule will meet Pericom's Wafer Fab Process Qualification requirements. This device also passed High Temp Storage Life (HTSL), Unbiased HAST (UHAST), and Temperature Cycle (TMCL) testing as shown in the table below.

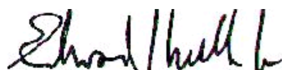
With no failures at the 168-hour timepoint, there is no concern over possible infant mortality issues that would require 100% burn-in for products using this process. This is the same result for all current Pericom designs and processes. The equivalent long-term life test FIT rate is 49.5 for Pericom devices using the same process and design rules, with a calculated MTBF of 260,000 hours. FIT rates are calculated using the Arrhenius equation, with an Activation Energy of 0.5 eV, an assumed customer system operating temperature of 55 °C, and a Confidence factor of 60%.

Pericom's Qualification Test results:

Rel Lot #	Device Type	Pkg. Type	Date Code	Stress Test	Stress Condition	Stress Duration	Sample Units	Results Pass/Fail
Q03007-1A	PI6C2510-133EL	L24	BY0323OC	DHTOL	150°C, 3.6 v	168 hrs	130	130/0
Q03007-1A	PI6C2510-133EL	L24	BY0323OC	DHTOL	150°C, 3.6 v	500 hrs	130	130/0
Q03007-1A	PI6C2510-133EL	L24	BY0323OC	DHTOL	150°C, 3.6 v	1000 hrs	130	130/0
Q03007-1A	PI6C2510-133EL	L24	BY0323OC	DHTOL	150°C, 3.6 v	2000 hrs	130	130/0
Q03007-1B	PI6C2510-133EL	L24	BY0323OC	HTSL	150°C	168 hrs	100	100/0
Q03007-1B	PI6C2510-133EL	L24	BY0323OC	HTSL	150°C	500 hrs	100	100/0
Q03007-1B	PI6C2510-133EL	L24	BY0323OC	HTSL	150°C	1000 hrs	100	100/0
Q03007-1C	PI6C2510-133EL	L24	BY0323OC	UHAST	130°C	96 hrs	80	80/0
Q03007-1D	PI6C2510-133EL	L24	BY0323OC	TMCL	-65, +150 °C	500 cycles	76	76/0

If there are any questions about this qualification, please contact me for further information.

Regards,



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