

**Process Reliability
Qualification Report**

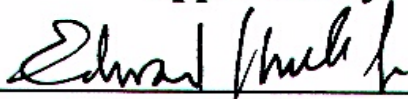
**SiliconClock
3.3V Zero-Delay &
Programmable Skew Clock
Drivers/Buffers
(2003 Update)**

Built In Reliability

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Reliability By Design

Approved by:



Edward J. Mello Jr., Director, Quality Systems



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COMMITMENT TO QUALITY:

Pericom supports the Quality Systems and Management concepts of the ISO-9000 series of international standards for Quality. A corporate Quality Policy (detailed below) has been established as the basis of our commitment to maintain a world class quality supplier status. Adhering to this policy is required for *all* employees, as Quality is not the responsibility of any one person or group; each and every employee shares it.

In recognition of our commitment, Pericom completed an ISO-9001 Registration Assessment Audit with Underwriter's Laboratories (UL), and Certificate Registration File Number A3151 was issued on March 27, 1995. We have successfully passed all Reassessment Audits since that time, and our Certificate was revised and reissued for two additional years on May 25, 1999. For customers requiring Pericom's Commercial and Government Entity (CAGE) identification, our assigned code is 06MQ5

Quality Policy:

Pericom will deliver products and services that conform to customer requirements. We shall perform each job correctly the first time, emphasizing constant improvement in the quality of our work.

"Pericom will deliver..." - delivery, not just intentions, is one of the key measures of Pericom's commitment to deliver a quality product to customers.


"...products and services..." - quality performance is not limited to physical products; sending a letter without spelling errors, or promptly and politely answering a telephone are services which demand our best quality.

"...that conform to customer requirements." - a clear understanding of all requirements are needed *before* one can deliver quality products or services. This also signifies mutual agreement, with clear, two-way communications, which applies to customers within as well as outside the company. The entire Pericom team understands that each customer has a set of requirements and expectations that must be met.

"We shall perform each job correctly the first time, ..." - doing jobs correctly the first time means meeting agreements, that quality improvement measures are driven to determine the source of defects and preventing those defects from reoccurring. The continual *process* of preventing defects will drive down the costs we and our customer's experience, because costs associated with rework, redesign, etc., are dollars taken from being price competitive.

"...emphasizing constant improvement in the quality of our work." - each employee shall strive to find better, faster, more economical ways to perform their job, to ensure that quality continues to improve along with cost effectiveness.


Alex Hui
President and CEO


Edward J. Mello, Jr.
Director, Quality Systems

PERICOM PRODUCT FAMILY AND WAFER FAB PROCESS

The Pericom product data presented in this report qualifies the following products from a marketing defined product family manufactured on the following wafer fab process:

Product Family: *SiliconClock*

Wafer Fab Process: *CSMS CS0E5E*

Wafer Supplier: *Chartered Semiconductor Manufacturing Corporation, Singapore*

Process Technology: *0.5µm Gate, 0.6µm M2, 3.3V Single-Poly Double-Metal CMOS*

Product Group: *3.3 Volt Zero-Delay & Programmable Skew Clock Buffers/Drivers*

Part Number	Product Description	Pins	Packages**
PI6C2301	One Output Phase-Locked Loop (PLL) Clock Driver	8	W
PI6C2302	2X Single Output PLL Clock Driver	8	W
PI6C2305-1	Five Output Zero-Delay Buffer	8	W
PI6C2308-1 (all)	Eight Output Zero-Delay Buffer, 10 to 134 MHz	8	L, W
PI6C2308A (all)	Eight Output Zero-Delay Buffer, 10 to 140 MHz	8	L, W
PI6C2309-1 (all)	Nine Output Zero-Delay Buffer	8	L, W
PI6C2310	PCI-X Clock Buffer, 133 MHz	24	L, Q
PI6C2401	1 Output Zero-Delay Clock Driver w/ Ext. Loopback	8	W
PI6C2402	1 Output Zero-Delay Clock Driver w/ Ext. Loopback, 2X Multiplier	8	W
PI6C2404A-1 (all)	2+2 Output Zero-Delay Clock Driver, 10 to 133 MHz	8	W
PI6C2405A-1 (all)	5 Output Zero-Delay Clock Driver (& High Drive)	8	L, W
PI6C2408 (all)	4+4 Output Zero Delay Clock Driver, 10 to 134 MHz (& High Drive)	16	L, W
PI6C2409-1 (all)	9 Output Zero-Delay Clock Driver (&High Drive)	16	L, W
PI6C2410	PCI-X Clock Buffer, 133 MHz, 4 outputs + Feedback	24	L, Q
PI6C2501	One Output PLL Clock Driver, 25 to 80 MHz	8	W
PI6C2501A	One Output PLL Clock Driver, 80 to 134 MHz	8	W
PI6C2502	Two Output PLL Clock Driver, 25 to 80 MHz	8	W
PI6C2502A	Two Output PLL Clock Driver, 25 to 80 MHz	8	W
PI6C2504	Four Output PLL Clock Driver, 25 to 80 MHz	16	Q
PI6C2504A	Four Output PLL Clock Driver, 80 to 134 MHz	16	Q
PI6C2509-133	Low Noise Nine Output PLL Clock Driver, 150 MHz	24	L
PI6C2510-133	Low Noise Ten Output PLL Clock Driver, 150 MHz	24	L
PI6C2516	Sixteen Output PLL Clock Driver, 135 MHz	48	A
PI6C2520	Low Noise Twenty Output PLL Clock Driver, 135 MHz	56	A
PI6C2952	180 MHz, Zero Delay Clock Driver w/Programmable Divider	32	FB
PI6C2972	125 MHz, Zero Delay Clock Driver w/Programmable Divider (LVTTL/LVCMOS inputs)	32	FC
PI6C2973 (all)	125 MHz, Zero Delay Clock Driver (LVTTL/LVCMOS/LVPECL)	32	FC
PI6C3991 (all)*	High Speed LVTTL Programmable Skew Clock Buffer	32	J
PI6C39911 (all)*	High Speed LVTTL Programmable Skew Clock Buffer	32	J
PI6C3Q991 (all)*	High Speed Balanced Programmable Skew Clock Buffer	32	J
PI6C3Q993 (all)*	High Speed Balanced Programmable Skew Clock Buffer	28	Q

* SuperClock™

** Refer to page 6 for package type codes and dimensions

AVAILABLE PACKAGE TYPE CODES AND DIMENSIONS

CODE	TYPE	LEAD STYLE, PITCH & STANDARD PACKAGE FAMILY DIMENSIONS
A	TSSOP	Gull wing bend leads, 0.5 mm lead pitch, 6.1 mm [240 mil] wide, 1.2 mm max height from seating plane
FB	LQFP	Gull wing bend leads, 0.80 mm lead pitch, 7.0 mm square [32 pin], 1.75 mm max height from seating plane
FC	LQFP	Gull wing bend leads, 0.65 mm lead pitch, 10.0 mm square [52 pin], 1.75 mm max height from seating plane
J	PLCC	J bend leads, 1.27 mm lead pitch, 14.0×11.4 mm [32 pin], 17.5×17.5 mm [44 pin] , 4 mm max height from seating plane
L	TSSOP	Gull wing bend leads, 0.65 mm lead pitch, 4.4 mm [173 mil] wide, 1.2 mm max height from seating plane
Q	QSOP	Gull wing bend leads, 0.64 mm lead pitch, 3.8 mm [150 mil] wide, 1.75 mm max height from seating plane
W	SOIC	Gull wing bend leads, 1.27 mm lead pitch, 3.8 mm [150 mil] wide, 1.75 mm max height from seating plane

PERICOM RELIABILITY TESTING METHODOLOGY

Pericom employs a commonly used industry method to generically qualify product. It is based on the premise that if one product of a specific wafer fab/package assembly process/materials is already qualified, then a second product that has similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second product without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.

The basis of this “qualification by similarity or extension” is the following rules:

A. For Wafer Fabrication Process and Materials:

- i) The wafer fabrication process technology and location are the same or similar*
- ii) The die array design rules and die size are the same or similar*
- iii) The standard and customized cell design and layout rules are the same or similar*
- iv) The density and complexity are the same or similar*
- v) The wafer fabrication materials are the same or similar*

B. For Package Assembly Process and Materials:

- i) The package assembly process technology and location are the same or similar*
- ii) The die paddle to package aspect ratio is the same or smaller*
- iii) The package dimensions width and thickness dimensions are the same or similar*
- iv) The leadframe/substrate design and lead/ball pitch are the same or similar*
- v) The package assembly materials are the same or similar*

Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs. All parts within the same family are designed to the same rules, and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/option, and only assembled on one package type process.

RELIABILITY PROCESS QUALIFICATION TESTS

PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)	PERICOM TEST CODE	EIA JEDEC STANDARD (NOTES BELOW)	EIAJ 4701 STANDARD JAPAN
Latch-Up Sensitivity	LU1	JESD17 (1)	ED-4701-1-C113
Latch-Up Sensitivity	LU2	JESD78 (2)	ED-4701-1-C113
Electrostatic Discharge Sensitivity	ESD1	MIL-STD-883 (3)	ED-4701-1-C111A
Electrostatic Discharge Sensitivity	ESD2	JESD22-A114B (4)	ED-4701-1-C111A
(Dynamic) High Temperature & Voltage Operating Life	DHTVOL	JESD22-A108B (5)	ED-4701-D101
High Temperature Storage Life (Bake)	HTSL	JESD22-A103A	ED-4701-3-B111A

PERICOM TEST CODE (SEE ABOVE)	TEST TEMPERATURE	MIN SAMPLE MAX/ACCEPT (MIN LOTS)	WHEN TESTS PERFORMED (NOTES BELOW)	AMPLITUDE MIN DURATION STRESS
LU1	25°C	1/0 (1 lot)	(1)	≥200mA/1.5×Vcc
LU2	25°C	1/0 (1 lot)	(2)	≥200mA/1.5×Vcc
ESD1	25°C	3/0 (1 lot)	(3)	≥1.3A/2000VHBM
ESD2	25°C	3/0 (1 lot)	(4)	≥1.3A/2000VHBM
DHTVOL	150°C (min. Bias: Vcc+10%)	129/1 (2 lots)	(6) (7) (8) (9)	3000 hrs (10)
HTSL	150°C (no bias)	32/0 (1 lot)	(6) (7) (8) (9)	168 hrs (10)

NOTES ON WHEN RELIABILITY TESTS ARE PERFORMED

1. LU performed for characterization data for new die design by Process Technology to JESD17 pre 1/1/00
2. LU performed for characterization data for new die/process by Process Technology to JESD78 after 1/1/00
3. ESD performed for characterization data for new die design by Process Technology to MIL-STD-883, Method 3015.7 prior to 1/1/00
4. ESD performed for characterization data for new die/process by Process Technology to MIL-STD-883, Method 3015.7 prior to 1/1/00 and to JESD22-A114 after 1/1/00. ESD performed for classification data for new die/process by Reliability to JESD22-A114 after 1/1/00
5. “Dynamic” implies AC signals are applied to the device inputs to simulate the worst case operating conditions of both inputs and outputs within the limitations of the burn-in sockets, board, power supplies and chamber.
6. Performed for new wafer fab subcontractor (on at least one device from the process family)
7. Performed for new array design family (on at least one device from the array design family)
8. Performed for new wafer fab process (on at least one device from at least one process family)
9. Performed for new die revision (on at least one lot of a device that has more than a one layer mask change)
10. Conditional release given when first lot completes 1000 hours with no rejects



Process Latch-Up & ESD Characterization Data

Latch-Up Test (LU)

CSMC 0.5 micron 3.3 volt SPDM CMOS (CS0E5E) Process

<i>Lot #</i>	<i>Device</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>V_{cc}_{max}</i>	<i>T_a</i>	<i>Remarks</i>
1	PI6C104-A1	A9814AOC	1	0	3.6V	25°C	JESD17
2	PI6C673	Z9936AOC	1	0	3.6V	25°C	JESD78
3	PI3C16212A	A9941AOC	1	0	3.6V	25°C	JESD78
4	PI6C2410	0230AOC	1	0	3.6V	25°C	JESD78

ESD Test (ESD)

Human Body Model (HBM)

CSMC 0.5 micron 3.3 volt SPDM CMOS (CS0E5E) Process

<i>Lot #</i>	<i>Device</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>V_{min}</i>	<i>T_a</i>	<i>Remarks</i>
1	PI6C671	Z9728AOC	3	0	2000V	25°C	MIL
2	PI3C16211	A9942BOC	3	0	2000V	25°C	MIL
3	PI3C3384	Z9910CSC	3	0	2000V	25°C	JESD22-A114A
4	PI6C2308C-1	ZD50145AOC	3	0	2000V	25°C	JESD22-A114A
5	PI6C2409	ZB10226AOC	3	0	2000V	25°C	JESD22-A114A
6	PI6C2405	0209AOC	3	0	2000V	25°C	JESD22-A114A
7	PI6C39911	Z0227AOC	3	0	2000V	25°C	JESD22-A114A
8	PI6C2410	0230AOC	3	0	2000V	25°C	JESD22-A114A



Process High Temperature Biased & Storage Die Life Test Data

Dynamic High Temperature & Voltage Operating Life Test (DHVTOL)

Reliability Failure Rate Summary

RELIABILITY STRESS TEST	REL LOT #	DEVICES TESTED	HOURS TESTED	DEVICE HOURS	NUMBER OF FAILS	ACTIVATION ENERGY (E _A)	FAILURE RATE
DHV/TOL <i>Early Life Failure Rate</i>	98095	120	168	20,160	0	N/A	0 PPM ²
	00062	118	168	19,824	0	N/A	0 PPM
	02061	130	168	21,840	0	N/A	0 PPM
PROCESS AVERAGE	→	368	168	61,824	0	N/A	0 PPM
DHV/TOL <i>Long Term Failure Rate</i>	98095	120	3000	360,000	0		
	00062	118	3000	354,000	0		
	02061	130	1000	130,000	0		
	<i>Total:</i>		368		844,000	0	0.5
MTBF / MTTF ¹	→	→	→	→	→	→	844,000 hrs

NOTES ON TABLE ABOVE AND ACCELERATION FACTORS:

1. $MTBF / MTTF = \text{Mean Time Between/To Failure} = 1/F_r$ ($F_r \geq 1$)
2. $PPM = \text{parts per million} = 10^{-6}$
3. $FIT = \text{Failures In Time} = F_r \times 10^9$
4. $F_r = \text{Failure rate (\% reject per 1000 hours)} = F_r \times 10^5 = \chi^2(x, v)/2 Ndt$
5. $\chi^2 = \text{Chi-squared value}$
6. $x = (1-CL)$ where $CL = \text{confidence level} = 60\%$
7. $v = (2N+2) = \text{degrees of freedom}$ where N is the number of rejects
8. $Ndt = \text{the equivalent device hours} = \text{device hours} \times AF$
9. $\text{Device hours} = \text{devices tested} \times \text{hours tested}$
10. $AF = \text{Acceleration Factor}$:
 - Arrhenius equation for accelerated temperature (A_t): $A_t = \exp\{-E_A/k(1/T_2 - 1/T_1)\}$
 - Arrhenius equation for accelerated voltage (A_v): $A_v = \exp\{C(V_S - V_o)\}$
11. $A_t = \text{thermal acceleration Factor}$
12. $A_v = \text{voltage acceleration Factor}$
13. $E_A = \text{average thermal activation energy for expected failure mechanisms} = 0.5 \text{ eV}$
14. $k = \text{Boltzmann's constant} = 8.62 \times 10^{-5} \text{ eV/}^\circ\text{K}$
15. $T_1 = \text{life test operating temperature}$
16. $T_2 = \text{system use operating temperature} = 55^\circ\text{C}$
17. $C = \text{constant that is a function of the dielectric thickness } (t_{ox}) = t_{ox}/100$
18. $V_S = \text{life test operating voltage}$
19. $V_o = \text{system use operating voltage}$

Dynamic High Temperature & Voltage Operating Life Test (DHVTOL)

CSMC 0.5 micron 3.3 volt SPDM CMOS (CS0E5E) Process

<i>Lot #</i>	<i>Device</i>	<i>Package</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>T_a</i>	<i>Remarks</i>
98095	PI6C2509	L24	Z9844ANC	120	0	3000	150°C	Vcc = 3.6 Volts
00062	PI6C2510	L24	Y0025AOC	118	0	3000	150°C	Vcc = 3.6 Volts
02061	PI6C2510-133	L24	AY0241AOC	130	0	1000	150°C	Vcc = 3.6 Volts

High Temperature Storage Life Test (HTSL)

CSMC 0.5 micron 3.3 volt SPDM CMOS (CS0E5E) Process

<i>Lot #</i>	<i>Device</i>	<i>Package</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>T_a</i>	<i>Remarks</i>
99033	PI74ALVCH32501	NB114	0035AOT	99	0	1000	150°C	MCM - 2 die
99033	PI74ALVCH32501	NB114	0036AOT	99	0	1000	150°C	MCM - 2 die
00061	PI3C34X484	NB96	0029AWC	97	0	1000	150°C	MCM - 4 die
00061	PI3C34X484	NB96	0036AWC	99	0	1000	150°C	MCM - 4 die
02061	PI6C2510-133	L24	AY0241AOC	130	0	1000	150°C	Vcc = 3.6 Volts