

Reliability Summary Report

PCI Bridge Products

March 20, 2003

(Updated Total Life Test Hours)

Reliability by Design

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COMMITMENT TO QUALITY:

Pericom supports the Quality Systems and Management concepts of the ISO-9000 series of international standards for Quality. A corporate Quality Policy (detailed below) has been established as the basis of our commitment to maintain a world class quality supplier status. Adhering to this policy is required for *all* employees, as Quality is not the responsibility of any one person or group; each and every employee shares it.

In recognition of our commitment, Pericom completed an ISO-9001 Registration Assessment Audit with Underwriter's Laboratories (UL), and Certificate Registration File Number A3151 was issued on March 27, 1995. We have successfully passed all Reassessment Audits since that time, and our most current Certificate was reissued for two additional years on May 24, 2001. Copies of our certificate and our Quality Systems Policy Manual are available at the Pericom website, <http://www.pericom.com/quality/index.php>. For customers requiring Pericom's Commercial and Government Entity (CAGE) identification, our assigned code is 06MQ5.

Quality Policy:

Pericom will deliver products and services that conform to customer requirements. We shall perform each job correctly the first time, emphasizing constant improvement in the quality of our work.

"Pericom will deliver..." - delivery, not just intentions, is one of the key measures of Pericom's commitment to deliver a quality product to customers.

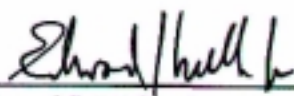
"...products and services..." - quality performance is not limited to physical products; sending a letter without spelling errors, or promptly and politely answering a telephone are services which demand our best quality.

"...that conform to customer requirements..." - a clear understanding of all requirements are needed *before* one can deliver quality products or services. This also signifies mutual agreement, with clear, two-way communications, which applies to customers within as well as outside the company. The entire Pericom team understands that each customer has a set of requirements and expectations that must be met.

"We shall perform each job correctly the first time, ..." - doing jobs correctly the first time means meeting agreements, that quality improvement measures are driven to determine the source of defects and preventing those defects from reoccurring. The continual *process* of preventing defects will drive down the costs we and our customer's experience, because costs associated with rework, redesign, etc., are dollars taken from being price competitive.

"...emphasizing constant improvement in the quality of our work..." - each employee shall strive to find better, faster, more economical ways to perform their job, to ensure that quality continues to improve along with cost effectiveness.


Alex Hui
President and CEO


Edward J. Mello, Jr.
Director, Quality Systems

PCI BRIDGE PRODUCT FAMILY

The information and data presented in this report is from the PI7C8154 device type, which also represents others from the same product family, using the same design rules and wafer fab process (TSMC-CS2L314). It's the most complex, with the largest die size in this family.

Part Number	Description	PCI Speed	PCI Bus Width	Ports	Pins	Package Type & Code
PI7C7300	3-Port PCI-to-PCI Bridge	66 MHz	32-bit	3	272	PBGA (NA272)
PI7C8150	2-Port PCI-to-PCI Bridge	66 MHz	32-bit	2	208, 256	FQFP (MA208), PBGA (ND256)
PI7C8150-33	2-Port PCI-to-PCI Bridge	33 MHz	32-bit	2	208, 256	FQFP (MA208), PBGA (ND256)
PI7C8152	2-Port PCI-to-PCI Bridge	66 MHz	32-bit	2	160	FQFP (MA160)
PI7C8154	2-Port PCI-to-PCI Bridge	66 MHz	64-bit	2	304	PBGA (NA304)
PI7C8154-33	2-Port PCI-to-PCI Bridge	33 MHz	64-bit	2	304	PBGA (NA304)

GENERIC WAFER FAB PROCESS TECHNOLOGIES

PROCESS	FAB	SUBCONTRACTOR CMOS PROCESS TECHNOLOGY DETAILS
TS2L314	TSMC	0.35 μ gate, 3.3V Single-Poly, Quad-Layer Metal (SPQM) CMOS
TS2L312	TSMC	0.35 μ gate, 3.3V Single-Poly, Dual-Layer Metal (SPDM) CMOS

WAFER FAB SUBCONTRACTOR AND CODES

CODE	FAB	FAB SUBCONTRACTOR & GEOGRAPHIC LOCATION	INTERNET ADDRESS
T	TSMC	Taiwan Semiconductor Manufacturing Corporation, Taiwan	http://www.tsmc.com/

STANDARD PACKAGE TYPE CODE AND DIMENSIONS

CODE	TYPE	LEAD STYLE, PITCH & STANDARD PACKAGE FAMILY DIMENSIONS
NA	PBGA	Plastic Ball Grid Array. 1.27 mm ball pitch, 31 x 31 mm (length/width), 2.53 mm thick – 304 ball 1.27 mm ball pitch, 27 x 27 mm (length/width), 3.50 mm thick – 256, 272 ball
ND	PBGA	Plastic Ball Grid Array. 1.0 mm ball pitch, 17 x 17 mm (length/width), 1.76 mm thick
MA	FQFP	Gull wing leads, 0.5 mm lead pitch, 6.1 mm [240 mil] wide, 1.2 mm thick

PACKAGE ASSEMBLY SUBCONTRACTORS AND CODES

MARK CODE	REPORT CODE	ASSEMBLY SUBCONTRACTOR/GEOGRAPHIC LOCATION	INTERNET ADDRESS
B	ASEM	ASE-Malaysia Semiconductor and Test	http://www.aseal.com.my
O	OSET	Orient Semiconductor and Test, Taiwan	http://www.ose.com.tw

MANUFACTURING INFORMATION

Die, Wafer Fabrication & Assembly – PI7C8154NA

<i>Component die size and thickness:</i>	6.99 x 6.99 x 0.36 mm³
<i>Current die revision:</i>	Z
<i>Silicon process & gate size</i>	TSMC – CMOS 0.35µm SPQM
<i>Wafer diameter (inches)</i>	8 (200 mm)

<i>Polysilicon layers (physical)</i>	<i>Poly 1</i>
Width (um)	0.35µm
Spacing (um)	0.65µm on “active”, 0.45 µm on “field oxide”
Thickness (Angstroms)	2.9K Å
Resistance	6.5 Ω/Sq
Current density @ breakdown	1.0 ma/µm (min, design spec)

<i>Metallization layers</i>	<i>Metal 1</i>	<i>Metal 2</i>	<i>Metal 3</i>	<i>Metal 4</i>
Width (um)	0.5 µm	0.6 µm	0.6 µm	0.6 µm
Spacing (um)	0.45 µm	0.5 µm	0.5 µm	0.6 µm
Thickness (Angstroms)	0.3K Å Ti / 1K Å TiN / 4K Å Al Cu / 1.4K Å TiN	1K Å TiN / 4K Å Al Cu / 1.4K Å TiN	1K Å TiN / 4K Å Al Cu / 1.4K Å TiN	1K Å TiN / 8K Å Al Cu / 0.25K Å TiN
Resistance	8.5 mΩ/Sq.	8.5 mΩ/Sq.	8.5 mΩ/Sq.	5.0 mΩ/Sq.
Current density @ breakdown	1.0 mA/µm	1.0 mA/µm	1.0 mA/µm	1.6 mA/µm

<i>Contacts/vias</i>	<i>Contact</i>	<i>Via</i>
Size (µm)	0.4 x 0.4 µm²	0.5 x 0.5 µm²
Overlap (µm)	M1/M2/M3/M4 overlap = 0.15 µm	
Oxide thickness (Angstroms)	10K Å	10K Å
Resistance	2.5 Ω/Ct	1.4 Ω /Via
Current density @ breakdown	1.06 mA	0.6 mA Via 1 & 2, 0.96 mA Via 3

Package Assembly

<i>Assembly Materials</i>	<i>OSE</i>	<i>ASEM</i>
Package Material/Ball Composition/Ball	BT Substrate/	BT Substrate/
Ball Composition/Ball Size	63% Sn/37%Pb/0.7 mm	63% Sn/37%Pb/0.7 mm
Die Attach Epoxy	Ablebond 8355F	Ablebond 8355F
Au Wire Size	1.0 mil	1.0 mil
Mold Compound	Plaskon SMT-B-1LV	Plaskon SMT-B-1LV

RELIABILITY TESTING METHODOLOGY

Pericom employs a commonly used industry method to generically qualify product. It's based on the following premise: if one product of a specific wafer fab/package assembly process/materials is already qualified, then a second product with similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.

The bases of “qualification by similarity or extension” are the following rules:

A. For Wafer Fabrication Process and Materials:

- i) The wafer fabrication process technology and location are the same or similar*
- ii) The die array design rules and die size are the same or similar*
- iii) The standard and customized cell design and layout rules are the same or similar*
- iv) The density and complexity are the same or similar*
- v) The wafer fabrication materials are the same or similar*

B. For Package Assembly Process and Materials:

- i) The package assembly process technology and location are the same or similar*
- ii) The die paddle to package aspect ratio is the same or smaller*
- iii) The package dimensions width and thickness dimensions are the same or similar*
- iv) The leadframe/substrate design and lead/ball pitch are the same or similar*
- v) The package assembly materials are the same or similar*

Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs, since all parts within the same family are designed to the same rules and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/option and only assembled on one package type process.

RELIABILITY QUALIFICATION - PLASTIC PACKAGE IC's

PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)	PERICOM TEST CODE	EIA JEDEC STANDARD (NOTES PAGE 9)	EIAJ 4701 STANDARD JAPAN
Latch-Up Sensitivity	LU1	JESD17 (1)	ED-4701-1-C113
Latch-Up Sensitivity	LU2	JESD78 (2)	ED-4701-1-C113
Electrostatic Discharge Sensitivity	ESD1	MIL-STD-883 (3)	ED-4701-1-C111A
Electrostatic Discharge Sensitivity	ESD2	JESD22-A114B (4)	ED-4701-1-C111A
(Dynamic) High Temperature & Voltage Operating Life	DHTVOL	JESD22-A108B (5)	ED-4701-D101
High Temperature Storage Life (Bake)	HTSL	JESD22-A103A	ED-4701-3-B111A
Temperature Humidity Bias (85/85/Biased)	THBT	JESD22-A101B	ED-4701-3-B122A
Temperature Humidity Storage (85/85/No Bias)	THST	JESD22-A101B	ED-4701-3-B122A
Accelerated Moisture Resistance (HAST/No Bias)	AMRT	JESD22-A118 (22)	-----
Autoclave (Pressure Cooker)	ACLV	JESD22-A102C	ED-4701-3-B123A
Temperature Cycling	TMCL	JESD22-A104B	ED-4701-3-B131A
Preconditioned Autoclave	PACLV	JESD22-A113B	A133B + B123A
Preconditioned Temperature Cycling	PTMCL	JESD22-A113B	A133B + B131A
External Package Integrity	EPI	Refer to QA-1803	-----
Internal Package Integrity	IPI	Refer to QA-1803	-----

PERICOM TEST CODE (SEE ABOVE)	TEMPERATURE HUMIDITY (PRESSURE)	SAMPLE SIZE MAX/ACCEPT (MIN LOTS)	WHEN TESTS PERFORMED (NOTES PAGE 9)	AMPLITUDE MIN DURATION STRESS
LU1	25°C	1/0 (1 lot)	(1)	≥200mA/1.5×Vcc
LU2	25°C	1/0 (1 lot)	(2)	≥200mA/1.5×Vcc
ESD1	25°C	3/0 (1 lot)	(3)	≥1.3A/2000VHBM
ESD2	25°C	3/0 (1 lot)	(4)	≥1.3A/2000VHBM
DHTVOL	125/150°C (min. Bias: Vcc+10%)	129/1 (3 lots)	(6) (10) (13) (16)	1000 hrs (18)
HTSL	150°C (no bias)	32/0 (1 lot)	(6) (10) (13) (16)	168 hrs (18)
THBT	85°C/85%RH (biased)	76/1 (1 lot)	(7)	1000 hrs
THST	85°C/85%RH (no bias)	76/1 (3 lots)	(20)	1000 hrs
AMRT	120°C/85%RH	76/1 (3 lots)	(23)	168 hrs
ACLV	121°C/100%RH(2atm)	76/1 (3 lots)	(8) (11) (14)	96 hrs (18)
TMCL	-65°C TO 150°C (no bias)	76/0 (3 lots)	(8) (11) (14) (21)	100 cycles (18)
PACLV	Level 1 Moisture Soak	100/1 (1 lot)	(9) (12) (15) (21)	168 hrs/168 hrs (19)
PTMCL	Level 1 Moisture Soak	76/0 (1 lot)	(9) (12) (15)	168 hrs/100 cycle (19)
EPI	25°C	5/0 (1 lot)	(17)	-----
IPI	25°C	5/0 (1 lot)	(17)	-----

NOTES ON WHEN RELIABILITY TESTS ARE PERFORMED

1. LU performed for characterization data for new die design by Process Technology to JESD17 pre 1/1/00
2. LU performed for characterization data for new die/process by Process Technology to JESD78 after 1/1/00
3. ESD performed for characterization data for new die design by Process Technology to MIL-STD-883, Method 3015.7 prior to 1/1/00
4. ESD performed for characterization data for new die/process by Process Technology to MIL-STD-883, Method 3015.7 prior to 1/1/00 and to JESD22-A114 after 1/1/00. ESD performed for classification data for new die/process by Reliability to JESD22-A114 after 1/1/00
5. “Dynamic” implies AC signals are applied to the device inputs to simulate the worst case operating conditions of both inputs and outputs within the limitations of the burn-in sockets, board, power supplies and chamber.
6. Performed for new wafer fab subcontractor (on at least one device from the process family)
7. Performed on at least one package per quarter as a monitor . This test is not performed as part of the qualification process due to the advances made in mold compound and assembly technologies. (Note D)
8. Performed for new package assembly subcontractor (on at least one package from at one package family)
9. Performed for new package assembly subcontractor (on the worst case package)
10. Performed for new array design family (on at least one device from the array design family)
11. Performed for new package design family (on at least one package lead count from the package family)
12. Performed for new package design family (on the worst case package)
13. Performed for new wafer fab process (on at least one device from at least one process family)
14. Performed for new package process/material (on at least one lot/package lead count from the package family)
15. Performed for new package process/material (on the worst case package)
16. Performed for new die revision (on at least one lot of a device that has more than a one layer mask change)
17. Performed for new package design family. Most tests can be done by the assembly supplier
18. Conditional release given when first lot completes 168 hours/100 cycles with no rejects
19. Establishes moisture sensitivity level (MSL) only. Not a condition of release. Stress can be done by supplier
20. Substituted for ACLV where conditions or package type dictate
21. Performed for redesigned package (on at least one lot from the package family) – “mini-qual”
22. Substituted for ACLV where conditions or package type dictate
23. Under development to replace saturated ACLV test

NOTES ON WHICH RELIABILITY TESTS ARE NOT PERFORMED

- A. Highly Accelerated Stress Test (HAST) is no longer performed since there is no known empirical correlation between HAST and THBT and it has been determined that HAST bias conditions are difficult to consistently maintain in a HAST environment. We recommend Unbiased HAST as a preferred test to verify resistance to moisture with better acceleration factors than THBT, HAST, or Autoclave.
- B. Thermal Shock Test (TMSK) is not performed since there is no known empirical correlation between TMSK and TMCL and it has been determined that the standard materials used to perform TMSK (fluorocarbons) present a potential health risk.
- C. Engineering evaluations have determined both the accelerated HAST and TMSK test environments have no real world equivalent and generate no value added data in lieu of advances made in mold compound and assembly technologies.
- D. Engineering evaluations have determined that the THBT test environment has a real world equivalent, however the time required to cause a failure precludes this as a qualification test as it would generate no value added data in lieu of advances made in mold compound and assembly technologies.

GUIDE TO READING THIS REPORT

Pericom Process Technology: See page 6

Pericom Package Type Code: See page 7

EXAMPLE:

CSM 0.6 micron 5.0 volt SPDM CMOS (CS0E6E) Process

<i>Lot #</i>	<i>Device</i>	<i>Package</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>T_a</i>	<i>Remarks</i>
00004	PI5C16215	A56	X0005FOC	157	0	3000	150 °C	Vcc = 7.0 V

Reliability Test Number

Sample Size

Rejects

Duration

Ambient Temp

<u>Date Code:</u>	<u>Definition (full traceability):</u>
<u>X</u> 0005FOC	Die revision letter code (<i>first issue no letter, then Z, X, Y, etc.</i>)
<u>0</u> 005FOC	Year of manufacture
<u>00</u> 5FOC	Work week of package assembly
<u>000</u> 5FOC	Package assembly subplot letter code
<u>0005</u> FOC	Package assembly facility code (see page 8)
<u>0005FO</u> C	Wafer fabrication facility code (see page 6)

<u>Typical Remarks:</u>
HTOL Bias Voltage
Failure Analysis Report (FAR) Number
Failure Point / Mechanism
Number of Die in Package
Moisture Sensitivity Level (MSL)
(<i>per JESD-22-A113B and J-STD-020B</i>)

Process/Design Test Summary

Dynamic High Temperature Operating Life Test (DHTOL)

Summary of TSMC 0.35 μm Process Life Test Data

<u>Process Name</u>	<u>FIT</u>	<u>MTBF</u>
<i>TS2L314</i>	<i>113</i>	<i>270,000 hours</i>
<i>TS2L312</i>	<i>29</i>	<i>480,000 hours</i>

NOTES:

FIT = Failures In Time = number of device failures per billion device hours and is calculated using the Arrhenius equation with an Activation Energy $E_A = 0.5 \text{ eV}$, System Temperature $T_S = 55^\circ\text{C}$, and $CL = 60\%$

MTBF = Mean Time Between Failure = the average time for device failure to occur and is calculated using:

Total Device Hours/Total Device Failures (a minimum of 1 even if there are no failures)

TSMC 0.35 μm , 3.3 volt SPQM CMOS (TS2L314) Process Results

Rel #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
R02060	PI7C8154	NA304	0238AOT	90	0	3000	125 °C	V _{cc} = 3.6V

Note: Updated 3/20/03 -life test for this lot has now completed 3000 hours with zero failures.

Failure Rate (Failures In Time @ 10⁹): = 113 FIT (0.5eV at 60% confidence level)

MTBF (Mean Time Between Failure): = 270,000 hours (Total Device hours/# failures (assumes 1 failure))

TSMC 0.35 μm , 3.3 volt SPDM CMOS (TS2L312) Process Results

Rel #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
00050A	PI90LV022	W16	0025AOT	160	0	3000	150 °C	V _{cc} = 3.6V

Failure Rate (Failures In Time @ 10⁹): = 29 FIT (0.5eV at 60% confidence level)

MTBF (Mean Time Between Failure): = 480,000 hours (Total Device hours/# failures, assumes 1 failure)

High Temperature Storage Life Test (HTSL)

TSMC 0.35 μm , 3.3 volt SPFM CMOS (TS2L314) Process

Lot #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
R02060	PI7C8154	NA304	0025AOT	100	0	1000	150 °C	

Package Environmental Test Summary

Temperature Humidity Biased Test (THBT)

PBGA-304

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>Remarks</i>
R02060	PI7C8154	NA304	0025AOT	90	0	1000	85 °C/85%RH

Moisture Autoclave (ACLV)

PBGA

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>Remarks</i>
R02060	PI7C8154	NA304	0025AOT	100	0	1000	

Temperature Cycle (TMCL)

PBGA

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Cycles</i>	<i>Remarks</i>
R02060	PI7C8154	NA304	0025AOT	76	0	500	

Preconditioned Moisture Autoclave (PACLV)

PBGA

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>Remarks</i>
R02060	PI7C8154	NA304	0025AOT	100	0	168	MSL 3

Preconditioned Temperature Cycle (PTMCL)

PBGA

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Cycles</i>	<i>Remarks</i>
R02060	PI7C8154	NA304	0025AOT	76	0	100	MSL 3

MOISTURE SENSITIVITY LEVEL OF PERICOM PACKAGES

Pericom's Integrated Circuit (IC) products are enclosed in plastic encapsulated or plastic covered substrate, Surface Mount Technology (SMT) packages. These have been evaluated by Moisture Sensitivity Testing (MST) and Moisture Resistance Testing (MRT) by Pericom and/or its assembly subcontractors and found to be in compliance with MSL requirements of the latest revisions to joint industry standards IPC/JEDEC J-STD-020A and JESD22-A113.

Pericom's SO (QSOP, SOIC (SOP), SSOP, TSSOP, SOT-23, and SC-70) and PLCC type packages have been determined to meet MSL 1 and therefore do not require any bake or dry pack prior to shipment. They are capable of withstanding 3 cycles of IR / Convection / Forced Air (N₂) reflow profiled to a recommended maximum peak temperature of 240°C. Customers do not need to store them in a specially controlled temperature and humidity environment prior to use. The floor life is unlimited at up to 30°C and 85% RH. No board mounting/reflow package damage should occur with product in these package types when utilizing industry standard SMT Reflow Solder profile methods and temperatures (including ramp rates and dwells).

Pericom's BGA (PBGA and LFBGA) and QFP (LQFP and TQFP) type packages have been determined to meet MSL 3 and therefore do require bake and dry pack prior to shipment. They are capable of withstanding three cycles of IR / Convection / Forced Air (N₂) reflow profiled to a recommended peak temperature of 225°C and a maximum peak temperature of 235°C. Customers do not need to store them in a specially controlled temperature and humidity environment prior to use provided they remain in tape and reel or trays (as applicable) in a dry environment. The floor life is limited to 168 hours at up to 30°C and 60% RH. No board mounting/reflow package damage should occur with product in these package types when utilizing industry standard SMT Reflow Solder profile methods and temperatures (including ramp rates and dwells), if used within the shelf life period.

Pericom ensures maximum protection against moisture penetration because our plastic encapsulated/covered substrate packages are designed using the most appropriate epoxy and leadframe/substrate materials applicable to the type of package being assembled. Pericom's IC chips also use a silicon nitride (SN₂) topside passivation to help reduce the possibility of moisture corrosion to the device metallization.

PERICOM PLASTIC PACKAGE IMPROVEMENTS

Pericom pioneered the use of 240°C Moisture/Reflow Sensitivity testing back in 1998. Pericom is currently preparing to evaluate higher reflow temperatures up to 260°C to accommodate customer requirements for lead-free soldering. Pericom works very closely with our package assembly subcontractors to constantly improve the mechanical design of all plastic packages they supply. The following areas are addressed:

A. For Plastic Encapsulated SO/PLCC Packages:

- i) Mold Compound material changes to improve mechanical and moisture sensitivity*
- ii) Leadframe material/design changes to improve mechanical and thermal sensitivity*
- iii) Die Attach Epoxy material/process changes to improve mechanical sensitivity*

B. For Plastic Overmolded PBGA/LFBGA:

- i) Mold Compound material changes to improve mechanical and moisture sensitivity*
- ii) Substrate material changes to improve mechanical and moisture sensitivity*
- iii) Die Attach Epoxy material/process changes to improve mechanical sensitivity*

PACKAGE SOLDER REFLOW CONDITIONS

SO/PLCC Convection/Infrared/N₂ Reflow Soldering

Stage	Maximum	Recommended	Minimum
Ramp up (°C /sec)	3°C /sec.	<2°C /sec. *	**
Dwell Time @ 183°C	150 sec.	<120 sec. *	60 sec. **
Solder Temperature	240°C **	<240°C *	**
Dwell Time @ Max.	40 sec.	<20 sec.	**
Ramp Down (°C /sec.)	5°C /sec.	<4°C /sec.	**

PBGA/LFBGA Convection/Infrared/N₂ Reflow Soldering

Stage	Maximum	Recommended	Minimum
Ramp up (°C /sec)	3°C /sec	<2°C /sec *	**
Dwell Time @ 183°C	150 sec.	<60 sec. *	60 sec. **
Solder Temperature	235°C **	<225°C *	**
Dwell Time @ Max.	20 sec.	<10 sec.	**
Ramp Down (°C /sec.)	5°C /sec.	<4°C /sec.	**

Notes:

Temperature measured at the component lead area in degrees Celsius.

* Will vary depending on board density, geometry and package type; good for up to three cycles (2-reflow+1 rework)

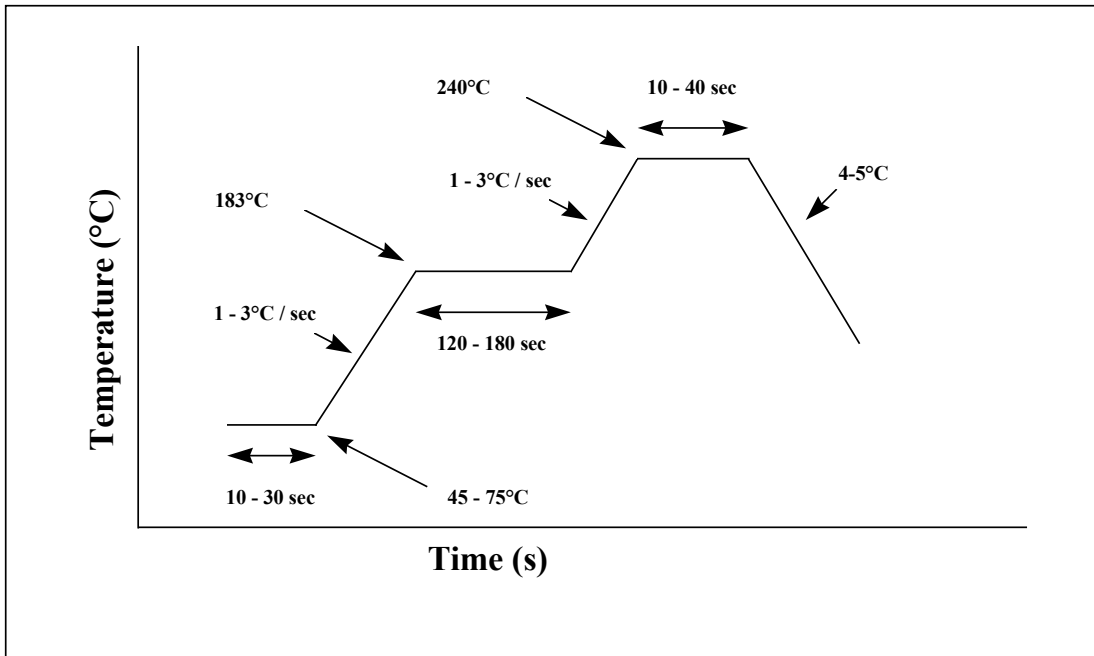
** Will vary depending on package types and board density.

PACKAGE SOLDER REFLOW PROFILES

Examples



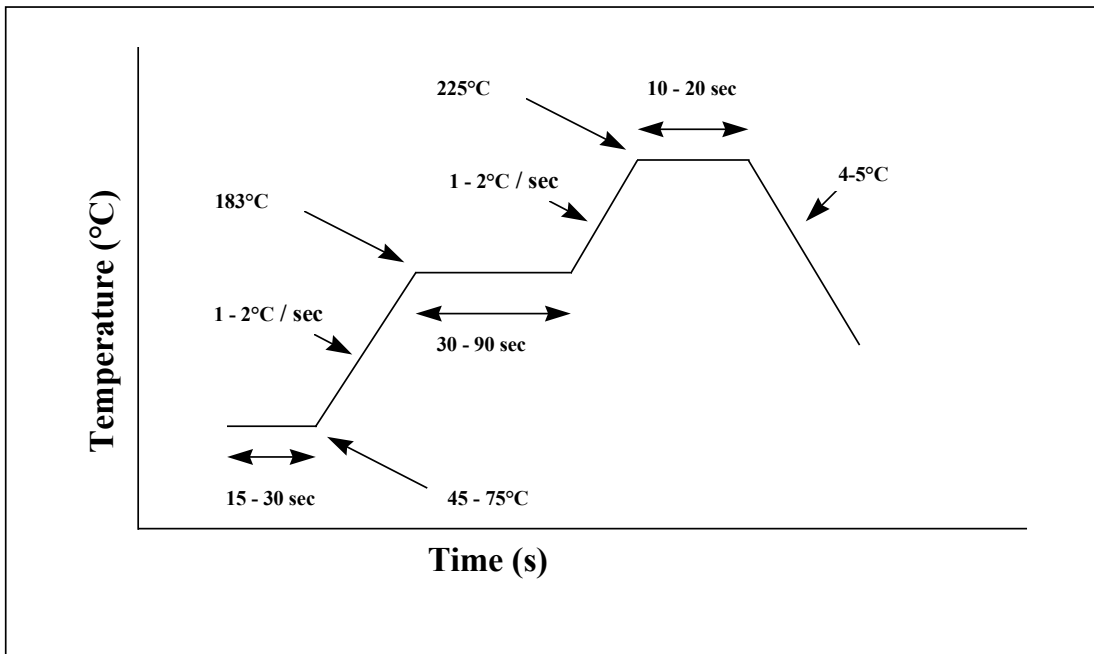
SO/PLCC Convection/IR +N₂
Solder Reflow Profile



01/01/01 issued by Pericom Semiconductor Corp.



PBGA/LFBGA Convection/IR
Solder Reflow Profile



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