

**Date:** May 10, 2004 - Update

**Subject:** CSMS Fab 2 CMOS 0.35µm Wafer Fab Reliability Report - PI74SSTV16857

This DDR Registered Buffer is manufactured for Pericom by CSM-S, Fab 2 facility in Singapore, using a 0.35µm, CMOS, 1P2M, 3.3-volt process that has been qualified for several years. It also generically covers CSMS's 1P3M process as well, differing only in the addition of a third metal layer. The TSSOP-56 package is assembled for Pericom by either OSE in Taiwan, Carsem in Malaysia, or SPEL in India. Other DDR products using the same design rules and process type are covered on a generic family basis, such as the PI74SSTV16859 and PI74SSTV32852.

The following Package Reliability Monitor Test information is a compilation of the process monitor results for this package type from all three facilities. The PI74SSTV16857 Electrical Test DPM is calculated from the sample test results for each lot, using an AQL of 0.065% after 100% electrical test screen to all required datasheet AC, DC and Functional tests. The FIT rates will be based on this device or an equivalent device using the same process and design rules, cumulatively from Q1, CY2003.

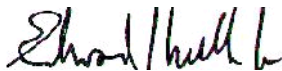
Monitor	CY2003 →	Q1	Q2	Q3	Q4	Totals
Package Reliability Monitor Tests	Solderability	182/0	204/0	194/0	204/0	784/0
	Temp Cycle	228/0	228/0	252/0	228/0	936/0
	ACLV	228/0	228/0	228/0	228/0	912/0
	HAST	228/0	228/0	228/0	228/0	912/0
	DHTOL	117/0	120/0	129/0	130/0	496/0
Electrical Test	DPM	0	0	0	0	0
FIT Rates *	Per 10 <sup>9</sup> hours	59.3	77.1	107.5	71.1	18.8

*accumulative*

*\*Note: The equivalent FIT rate is calculated using the Arrhenius equation, with an Activation energy of 0.5 eV, an assumed system operating temperature of 55 °C, and a Confidence Level of 60%. Test performed was Dynamic High Temperature Operating Life (DHTOL) Test with an accelerated Vcc bias of 3.6 volts, and a T<sub>A</sub> of 150 °C. The sample size was 117 for 2000 hours in the Q1 reporting period, 120 units for 1500 hours in Q2, 129 samples for 1000 hours in Q3, and 130 samples for 1500 hours in Q4. No rejects observed. Combined FIT rate for all lots tested is shown in the Totals column.*

If there are any questions about the above information, please let contact me at your convenience.

Regards,



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