

Reliability Summary Report PI6CV857A

August 28, 2002

Reliability by Design

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COMMITMENT TO QUALITY:

Pericom supports the Quality Systems and Management concepts of the ISO-9000 series of international standards for Quality. A corporate Quality Policy (detailed below) has been established as the basis of our commitment to maintain a world class quality supplier status. Adhering to this policy is required for *all* employees, as Quality is not the responsibility of any one person or group; each and every employee shares it.

In recognition of our commitment, Pericom completed an ISO-9001 Registration Assessment Audit with Underwriter's Laboratories (UL), and Certificate Registration File Number A3151 was issued on March 27, 1995. We have successfully passed all Reassessment Audits since that time, and our most current Certificate was reissued for two additional years on May 24, 2001. Copies of our certificate and our Quality Systems Policy Manual are available at the Pericom website, <http://www.pericom.com/quality/index.php>. For customers requiring Pericom's Commercial and Government Entity (CAGE) identification, our assigned code is 06MQ5.

Quality Policy:

Pericom will deliver products and services that conform to customer requirements. We shall perform each job correctly the first time, emphasizing constant improvement in the quality of our work.

"Pericom will deliver..." - delivery, not just intentions, is one of the key measures of Pericom's commitment to deliver a quality product to customers.

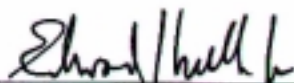
"...products and services..." - quality performance is not limited to physical products; sending a letter without spelling errors, or promptly and politely answering a telephone are services which demand our best quality.

"...that conform to customer requirements..." - a clear understanding of all requirements are needed *before* one can deliver quality products or services. This also signifies mutual agreement, with clear, two-way communications, which applies to customers within as well as outside the company. The entire Pericom team understands that each customer has a set of requirements and expectations that must be met.

"We shall perform each job correctly the first time, ..." - doing jobs correctly the first time means meeting agreements, that quality improvement measures are driven to determine the source of defects and preventing those defects from reoccurring. The continual *process* of preventing defects will drive down the costs we and our customer's experience, because costs associated with rework, redesign, etc., are dollars taken from being price competitive.

"...emphasizing constant improvement in the quality of our work..." - each employee shall strive to find better, faster, more economical ways to perform their job, to ensure that quality continues to improve along with cost effectiveness.


Alex Hui
President and CEO


Edward J. Mello, Jr.
Director, Quality Systems

PRODUCT FAMILY AND WAFER FAB PROCESS

The Pericom product data presented in this report represents data from those products using the same design rules and wafer fab process as the PI6CV857 and 857L, indicated below:

DDR Product

PI6CV857, 857L

2.5 Volt Bus SSTV Clock Driver

Primary Wafer Fab Process

CSMS -CS2L313

Back-up Wafer Fab

TSMC

GENERIC WAFER FAB PROCESS TECHNOLOGIES

PROCESS	FAB	SUBCONTRACTOR CMOS PROCESS TECHNOLOGY DETAILS
CS2L312	CSMS	0.35μ gate, 3.3V Single-Poly Double-Metal (SPDM) CMOS
TS2L312	TSMC	0.35μ gate, 3.3V Single-Poly Double-Metal (SPDM) CMOS
CS2L312A	CSMS	0.35μ gate, 3.3V Single-Poly Double-Metal (SPDM) CMOS (Enhanced)
CS2L313	CSMS	0.35μ gate, 3.3V Single-Poly Triple-Metal (SPTM) CMOS

WAFER FAB SUBCONTRACTOR AND CODES

CODE	FAB	FAB SUBCONTRACTOR & GEOGRAPHIC LOCATION	INTERNET ADDRESS
C	CSMS	Chartered Semiconductor Manufacturing Corporation, Singapore	http://www.charteredsemi.com
T	TSMC	Taiwan Semiconductor Manufacturing Corporation, Taiwan	http://www.tsmc.com.tw

STANDARD PACKAGE TYPE CODE AND DIMENSIONS

CODE	TYPE	LEAD STYLE, PITCH & STANDARD PACKAGE FAMILY DIMENSIONS
A	TSSOP	Gull wing leads, 0.5 mm lead pitch, 6.1 mm [240 mil] wide, 1.2 mm high

PACKAGE ASSEMBLY SUBCONTRACTORS AND CODES

MARK CODE	REPORT CODE	ASSEMBLY SUBCONTRACTOR/GEOGRAPHIC LOCATION	INTERNET ADDRESS
N	CSTS	Carsem (S Facility) Semiconductor and Test, Malaysia	http://www.carsem.com
O	OSET	Orient Semiconductor and Test, Taiwan	http://www.ose.com.tw
X	SPEL	SPEL Semiconductor Limited, India	http://www.spel.com

MANUFACTURING INFORMATION

Die and Wafer Fabrication

<i>Component die size and thickness:</i>	1.6 x 2.57 x 0.24 mm²
<i>Current die revision:</i>	V
<i>Silicon process & gate size</i>	Chartered Fab2 – CMOS 0.35µm SPTM Polycide
<i>Wafer diameter (inches)</i>	8

<i>Polysilicon layers (physical)</i>	<i>Poly 1</i>
Width (um)	0.35µm
Spacing (um)	0.50µm
Thickness (Angstroms)	1500Å Poly + 1000Å WSix
Resistance	10Ω/Sq
Current density @ breakdown	1.7 ma/µA/(min, design spec)

<i>Metallization layers</i>	<i>Metal 1</i>	<i>Metal 2</i>	<i>Metal 3</i>
Width (um)	0.5µm	0.6µm	0.6 µm
Spacing (um)	0.5µm	0.6µm	0.6 µm
Thickness (Angstroms)	600 Å TiN/5000 Å Al Cu/300 Å TiN	Same as Metal 1	600 Å TiN/8000 Å Al Cu/300 Å TiN
Resistance	60M Ω/Sq.	60MΩ/Sq	40 MΩ/Sq.
Current density @ breakdown	2.5mA/µm	2.5 mA/µm	3.1 mA/µm

<i>Contacts/vias</i>	<i>Contact</i>	<i>Via</i>
Size (µm)	0.4 x 0.4 µm²	0.5 x 0.5 µm²
Overlap (µm)	M1 overlap = 0.2µm, M2 overlap = 0.2µm, M3 overlap = 0.4µm	
Oxide thickness (Angstroms)	5250 Å	8000 Å
Resistance	14 Ω/Ct	1.5Ω/Via
Current density @ breakdown	2.0mA /µm	2.0mA /µm

Package Assembly

<i>Assembly Materials</i>	<i>OSE</i>	<i>Carsem</i>	<i>SPEL</i>
Leadframe Material/Finish	Cu/Solder Plate 85% Sn/15%Pb		
Die Pad Size	100 x 180 mils	118 x 196	90 x 190
Die Attach Epoxy	Ablebond 8355F	Ablebond 84-1LMISR4	Ablebond 84-1LMISR4
Au Wire Size	1.2 mil	1.0 mil	1.0 mil
Mold Compound	KMC 184-2	Aratronic 2184	EME7351-LP

RELIABILITY TESTING METHODOLOGY

Pericom employs a commonly used industry method to generically qualify product. It's based on the following premise: if one product of a specific wafer fab/package assembly process/materials is already qualified, then a second product with similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.

The bases of “qualification by similarity or extension” are the following rules:

A. For Wafer Fabrication Process and Materials:

- i) The wafer fabrication process technology and location are the same or similar*
- ii) The die array design rules and die size are the same or similar*
- iii) The standard and customized cell design and layout rules are the same or similar*
- iv) The density and complexity are the same or similar*
- v) The wafer fabrication materials are the same or similar*

B. For Package Assembly Process and Materials:

- i) The package assembly process technology and location are the same or similar*
- ii) The die paddle to package aspect ratio is the same or smaller*
- iii) The package dimensions width and thickness dimensions are the same or similar*
- iv) The leadframe/substrate design and lead/ball pitch are the same or similar*
- v) The package assembly materials are the same or similar*

Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs, since all parts within the same family are designed to the same rules and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/option and only assembled on one package type process.

RELIABILITY QUALIFICATION - PLASTIC PACKAGE IC's

PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)	PERICOM TEST CODE	EIA JEDEC STANDARD (NOTES PAGE 9)	EIAJ 4701 STANDARD JAPAN
Latch-Up Sensitivity	LU1	JESD17 (1)	ED-4701-1-C113
Latch-Up Sensitivity	LU2	JESD78 (2)	ED-4701-1-C113
Electrostatic Discharge Sensitivity	ESD1	MIL-STD-883 (3)	ED-4701-1-C111A
Electrostatic Discharge Sensitivity	ESD2	JESD22-A114B (4)	ED-4701-1-C111A
(Dynamic) High Temperature & Voltage Operating Life	DHTVOL	JESD22-A108B (5)	ED-4701-D101
High Temperature Storage Life (Bake)	HTSL	JESD22-A103A	ED-4701-3-B111A
Temperature Humidity Bias (85/85/Biased)	THBT	JESD22-A101B	ED-4701-3-B122A
Temperature Humidity Storage (85/85/No Bias)	THST	JESD22-A101B	ED-4701-3-B122A
Accelerated Moisture Resistance (HAST/No Bias)	AMRT	JESD22-A118 (22)	-----
Autoclave (Pressure Cooker)	ACLV	JESD22-A102C	ED-4701-3-B123A
Temperature Cycling	TMCL	JESD22-A104B	ED-4701-3-B131A
Preconditioned Autoclave	PACLV	JESD22-A113B	A133B + B123A
Preconditioned Temperature Cycling	PTMCL	JESD22-A113B	A133B + B131A
External Package Integrity	EPI	Refer to QA-1803	-----
Internal Package Integrity	IPI	Refer to QA-1803	-----

PERICOM TEST CODE (SEE ABOVE)	TEMPERATURE HUMIDITY (PRESSURE)	SAMPLE SIZE MAX/ACCEPT (MIN LOTS)	WHEN TESTS PERFORMED (NOTES PAGE 9)	AMPLITUDE MIN DURATION STRESS
LU1	25°C	1/0 (1 lot)	(1)	≥200mA/1.5×Vcc
LU2	25°C	1/0 (1 lot)	(2)	≥200mA/1.5×Vcc
ESD1	25°C	3/0 (1 lot)	(3)	≥1.3A/2000VHBM
ESD2	25°C	3/0 (1 lot)	(4)	≥1.3A/2000VHBM
DHTVOL	125/150°C (min. Bias: Vcc+10%)	129/1 (3 lots)	(6) (10) (13) (16)	1000 hrs (18)
HTSL	150°C (no bias)	32/0 (1 lot)	(6) (10) (13) (16)	168 hrs (18)
THBT	85°C/85%RH (biased)	76/1 (1 lot)	(7)	1000 hrs
THST	85°C/85%RH (no bias)	76/1 (3 lots)	(20)	1000 hrs
AMRT	120°C/85%RH	76/1 (3 lots)	(23)	168 hrs
ACLV	121°C/100%RH(2atm)	76/1 (3 lots)	(8) (11) (14)	96 hrs (18)
TMCL	-65°C TO 150°C (no bias)	76/0 (3 lots)	(8) (11) (14) (21)	100 cycles (18)
PACLV	Level 1 Moisture Soak	100/1 (1 lot)	(9) (12) (15) (21)	168 hrs/168 hrs (19)
PTMCL	Level 1 Moisture Soak	76/0 (1 lot)	(9) (12) (15)	168 hrs/100 cycle (19)
EPI	25°C	5/0 (1 lot)	(17)	-----
IPI	25°C	5/0 (1 lot)	(17)	-----

NOTES ON WHEN RELIABILITY TESTS ARE PERFORMED

1. LU performed for characterization data for new die design by Process Technology to JESD17 pre 1/1/00
2. LU performed for characterization data for new die/process by Process Technology to JESD78 after 1/1/00
3. ESD performed for characterization data for new die design by Process Technology to MIL-STD-883, Method 3015.7 prior to 1/1/00
4. ESD performed for characterization data for new die/process by Process Technology to MIL-STD-883, Method 3015.7 prior to 1/1/00 and to JESD22-A114 after 1/1/00. ESD performed for classification data for new die/process by Reliability to JESD22-A114 after 1/1/00
5. “Dynamic” implies AC signals are applied to the device inputs to simulate the worst case operating conditions of both inputs and outputs within the limitations of the burn-in sockets, board, power supplies and chamber.
6. Performed for new wafer fab subcontractor (on at least one device from the process family)
7. Performed on at least one package per quarter as a monitor . This test is not performed as part of the qualification process due to the advances made in mold compound and assembly technologies. (Note D)
8. Performed for new package assembly subcontractor (on at least one package from at one package family)
9. Performed for new package assembly subcontractor (on the worst case package)
10. Performed for new array design family (on at least one device from the array design family)
11. Performed for new package design family (on at least one package lead count from the package family)
12. Performed for new package design family (on the worst case package)
13. Performed for new wafer fab process (on at least one device from at least one process family)
14. Performed for new package process/material (on at least one lot/package lead count from the package family)
15. Performed for new package process/material (on the worst case package)
16. Performed for new die revision (on at least one lot of a device that has more than a one layer mask change)
17. Performed for new package design family. Most tests can be done by the assembly supplier
18. Conditional release given when first lot completes 168 hours/100 cycles with no rejects
19. Establishes moisture sensitivity level (MSL) only. Not a condition of release. Stress can be done by supplier
20. Substituted for ACLV where conditions or package type dictate
21. Performed for redesigned package (on at least one lot from the package family) – “mini-qual”
22. Substituted for ACLV where conditions or package type dictate
23. Under development to replace saturated ACLV test

NOTES ON WHICH RELIABILITY TESTS ARE NOT PERFORMED

- A. Highly Accelerated Stress Test (HAST) is no longer performed since there is no known empirical correlation between HAST and THBT and it has been determined that HAST bias conditions cannot be maintained in a HAST environment. We recommend Unbiased HAST as a preferred test to verify resistance to moisture with better acceleration factors than THBT, HAST, or Autoclave.
- B. Thermal Shock Test (TMSK) is not performed since there is no known empirical correlation between TMSK and TMCL and it has been determined that the standard materials used to perform TMSK (fluorocarbons) present a potential health risk.
- C. Engineering evaluations have determined both the accelerated HAST and TMSK test environments have no real world equivalent and generate no value added data in lieu of advances made in mold compound and assembly technologies.
- D. Engineering evaluations have determined that the THBT test environment has a real world equivalent, however the time required to failure precludes this as a qualification test as it would generate no value added data in lieu of advances made in mold compound and assembly technologies.

GUIDE TO READING THIS REPORT

Pericom Process Technology: See page 6

Pericom Package Type Code: See page 7

EXAMPLE:

CSM 0.6 micron 5.0 volt SPDM CMOS (CS0E6E) Process

<i>Lot #</i>	<i>Device</i>	<i>Package</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>T_a</i>	<i>Remarks</i>
00004	PI5C16215	A56	X0005FOC	157	0	3000	150 °C	Vcc = 7.0 V

Reliability Test Number

Sample Size

Rejects

Duration

Ambient Temp

<u>Date Code:</u>	<u>Definition (full traceability):</u>
<u>X</u> 0005FOC	Die revision letter code (<i>first issue no letter, then Z, X, Y, etc.</i>)
<u>0</u> 005FOC	Year of manufacture
<u>00</u> 5FOC	Work week of package assembly
<u>000</u> 5FOC	Package assembly subplot letter code
<u>0005</u> FOC	Package assembly facility code (see page 8)
<u>0005FO</u> C	Wafer fabrication facility code (see page 6)

<u>Typical Remarks:</u>
HTOL Bias Voltage
Failure Analysis Report (FAR) Number
Failure Point / Mechanism
Number of Die in Package
Moisture Sensitivity Level (MSL)
(<i>per JESD-22-A113B and J-STD-020B</i>)

Process/Design **Test Summary**

Dynamic High Temperature Operating Life Test (DHTOL)

Summary of Process Life Test Data

<u>Process</u>	<u>FIT</u>	<u>MTBF</u>
CS2L313	9	175 years

NOTES:

FIT = Failures In Time = number of device failures per billion device hours and is calculated using the Arrhenius equation with an Activation Energy $E_A = 0.5 \text{ eV}$ and System Temperature $T_S = 55^\circ\text{C}$

MTBF = Mean Time Between Failure = the average time for device failure to occur and is calculated using:

Total Device Hours/Total Device Failures (a minimum of 1 even if there are no failures)

CSMS 0.35 μm , 3.3 volt SPDM/SPTM CMOS (CS2L312, CS2L312A & CS2L313) Process

Lot #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
98068A	PI3B3384	S24	9824AOC	130	0	3000	150 °C	Vcc = 3.6V
98082A	PI74ALPT16245	V48	Z9829ASC	130	0	1000	150 °C	Vcc = 3.6V
98096A	PI74ALPT16245	V48	Z9845AOC	116	0	3000	150 °C	Vcc = 3.6V
00042A	PI3B3384	S24	Z0022AOC	240	0	1000	150 °C	Vcc = 3.6V
00044A	PI74ALVCT16245	V48	Y0020AOC	130	0	1000	150 °C	Vcc = 3.6V
00063A	PI74SSTV16857	V48	0030AOC	120	0	500	150 °C	Vcc = 3.6V
00063AR	PI74SSTV16857	V48	0030AOC	117	0	2000	150 °C	Vcc = 3.6V

Maximum Failure Rate: 9 FIT 0.5eV at 60% confidence level

MTBF: 1,532,000 hours (~175 years)

TSMC 0.35 μm , 3.3 volt SPDM CMOS (TS2L312) Process

Lot #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
00050A	PI90LV022	W16	0025AOT	160	0	3000	150 °C	Vcc = 3.6V

Maximum Failure Rate: 29 FIT 0.5eV at 60% confidence level

MTBF: 480,000 hours (~55 years)

High Temperature Storage Life Test (HTSL)

CSMS 0.35 μm 3.3 volt SPDM/SPTM CMOS (CS2L312, CS2L312A & CS2L313) Process

Lot #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
98048B	PI3B3384	S24	9816AOC	100	0	1000	150 °C	
00043A	PI3B3384S	S24	Y0020BOC	160	0	1000	150 °C	
00044B	PI74ALVCT16245	A48	Y0020COC	80	0	1000	150 °C	
00051B	P74SSTV16857	A48	Y0016DOC	79	0	1000	150 °C	
00063B	P74SSTV16857	V48	0030AOC	80	0	1000	150 °C	

TSMC 0.5 μm , 3.3 volt SPDM CMOS (TS2L312) Process

Lot #	Device Type	Package	Date Code	SS	Rej.	Hours	T _a	Remarks
00050B	PI90LV022	W16	A10025AOT	80	0	1000	150 °C	

Package
Environmental Test
Summary

Temperature Humidity Biased Test (THBT)

TSSOP

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>Remarks</i>
98093D	PI5C16215	TSSOP / A48	9912ASC	78	0	1000	
99053	PI5C16215	TSSOP / A48	9923ASC	78	0	1000	
00004C	PI5C16215	TSSOP / A48	9923ASC	80	0	1000	

Moisture Resistance Autoclave (ACLV)

TSSOP

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>Remarks</i>
98051-1A	PI74FCT162543T	TSSOP / A56	9821ANC	100	0	168	
98051-2A	PI74FCT162543T	TSSOP / A56	9822ANC	99	0	168	
98051-3A	PI74FCT162543T	TSSOP / A56	9823ANC	99	0	168	
99016-1A	PI5C16211	TSSOP / A56	Z9924AJC	77	0	168	
99016-2A	PI5C16211	TSSOP / A56	Z9925AJC	99	0	168	
99016-3A	PI5C16211	TSSOP / A56	Z9926AJC	94	0	168	
99048-1A	PI5C16211	TSSOP / A56	Z006AEC	100	0	168	
99050-1A	PI5C16211	TSSOP / A56	Z0007APY	98	0	168	
00038-1A	PI5C32200	TSSOP / A56	Y0022AOC	100	0	168	4 die/pads
00038-2A	PI5C32200	TSSOP / A56	Y0024AOC	100	0	168	4 die/pads
00038-3A	PI5C32200	TSSOP / A56	Y0026AOC	92	0	168	4 die/pads
00085-1A	PI74SSTV16859	TSSOP / A64	0039AJC	98	0	168	2 die/pads
00085-2A	PI74SSTV16859	TSSOP / A64	0041AJC	100	0	168	2 die/pads
00085-3A	PI74SSTV16859	TSSOP / A64	0042AJC	100	0	168	2 die/pads
02018-1B	PI5C16211A	TSSOP / A56	Z0220AXC	100	0	168	

Temperature Cycle (TMCL)

TSSOP

Lot #	Device	Package/Code	Date Code	SS	Rej.	Cycles	Remarks
98051-1B	PI74FCT162543	TSSOP / A56	9821ANC	100	0	100	
98051-2B	PI74FCT162543	TSSOP / A56	9822ANC	100	0	100	
98051-3B	PI74FCT162543	TSSOP / A56	9823ANC	94	0	100	
98059-B	PI5C16211	TSSOP / A56	Z9821AOC	100	0	100	
99016-1B	PI5C16211	TSSOP / A56	Z9924AJC	60	0	100	
99016-2B	PI5C16211	TSSOP / A56	Z9925AJC	100	0	100	
99016-3B	PI5C16211	TSSOP / A56	Z9926AJC	100	0	100	
99048-1B	PI5C16211	TSSOP / A56	Z0006AEC	100	0	100	
99048-2B	PI5C16211	TSSOP / A56	Z0007AEC	100	0	100	
99048-3B	PI5C16211	TSSOP / A56	Z0008AEC	100	0	100	
99050-1B	PI5C16211	TSSOP / A56	Z0007APC	100	0	100	
99050-2B	PI5C16211	TSSOP / A56	Z0009BPC	100	0	100	
00004-1A	PI5C16215	TSSOP / A48	9923ASC	80	0	500*	
00038-1B	PI5C32200	TSSOP / A56	Y0022AOC	100	0	100	
00038-2B	PI5C32200	TSSOP / A56	Y0024AOC	100	0	100	
00038-3B	PI5C32200	TSSOP / A56	Y0026AOC	100	0	100	
00085-2B	PI74SSTV16859	TSSOP / A64	0041AJC	79	0	100	2 die/pads
00085-3B	PI74SSTV16859	TSSOP / A64	0042AJC	68	0	100	2 die/pads
02018-1B	PI5C16211A	TSSOP / A56	Z0220AXC	100	0	500	

Note: the PI5C16215 device type uses the same design rules and CS2L313 SPTM process as the PI6CV857 product. The samples were subjected to 500 cycles of standard Temp Cycle at -65 C to +150 °C

Preconditioned Moisture Autoclave (PACLV)

TSSOP

<i>Lot #</i>	<i>Device</i>	<i>Package/Code</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>Hours</i>	<i>Remarks</i>
98102A	PI5C16212	TSSOP / A56	Z9835CNC	100	0	168	Level 1
98106A	PI5C16211	TSSOP / A56	Z9845ANC	99	0	168	Level 1
98113A	PI74LPT16501	TSSOP / A56	9849BNC	99	0	168	Level 1
99016PA	PI5C16211	TSSOP / A56	Z9924AJC	100	0	168	Level 1
99018A	PI74ALVCH162827	TSSOP / A56	Z9915CNT	99	0	168	Level 1
99036A	PI74FCT16374	TSSOP / A48	X9923BOC	100	0	168	Level 1
99038A	PI5C16292	TSSOP / A56	Z9923BNC	95	0	168	Level 1
99043A	PI74LPT16244	TSSOP / A48	Z9931COC	100	0	168	Level 1
99058A	PI5C16211	TSSOP / A56	Z9937ANC	100	0	168	Level 1
99061A	PI5C16211	TSSOP / A56	Z9948MOC	100	0	168	Level 1
00002A	PI5C16211A	TSSOP / A56	Z9948AOC	100	0	168	Level 1
00012A	PI74ALVC16835	TSSOP / A56	9942INT	100	0	168	Level 1
00014A	PI74ALVCT16260	TSSOP / A56	9950RNT	100	0	168	Level 1
00026A	PI74ALVCT1622601	TSSOP / A56	0006ANT	100	0	168	Level 1
00032A	PI74ALVCH16244	TSSOP / A48	0006BOC	100	0	168	Level 1
00036A	PI5C16211A	TSSOP / A56	Z0010DNC	100	0	168	Level 1
00048A	PI5C16211A	TSSOP / A56	Z0015DNC	100	0	168	Level 1
00057A	PI5C16861A	TSSOP / A48	0022BOG	99	0	168	Level 1
00070A	PI5C16211A	TSSOP / A56	Z0027COC	100	0	168	Level 1
00071A	PI5C16861A	TSSOP / A48	0029LOG	100	0	168	Level 1
00075A	PI5C16211A	TSSOP / A56	Z0025ANC	100	0	168	Level 1
01068B	PI74SSTV16857	TSSOP / A/48	0137AOC	100	0	168	Level 1
02018-1A	PI5C16211A	TSSOP / A56	Z0220AXC	100	0	168	Level 1

Preconditioned Temperature Cycle (PTMCL)

TSSOP

Lot #	Device	Package/Code	Date Code	SS	Rej.	Cycles	Remarks
98106B	PI5C16211	TSSOP / A56	Z9845ANC	75	0	200	Level 1
98113B	PI74LPT16501	TSSOP / A56	9849BNC	77	0	200	Level 1
99016-PB	PI5C16211	TSSOP / A56	Z9924AJC	97	0	100	Level 1
99018B	PI74ALVCHI162827	TSSOP / A56	Z9915CNT	76	0	200	Level 1
99023A	PI5C16211	TSSOP / A56	Z9918XNC	76	0	200	Level 1
99036B	PI74FCT16374	TSSOP / A48	X9923BOC	76	0	100	Level 1
99041B	PI74FCT16835	TSSOP / A56	9928ANT	76	0	200	Level 1
99043B	PI74LPT16244	TSSOP / A48	Z9931COC	76	0	100	Level 1
99058B	PI5C16211	TSSOP / A56	Z9937ANC	76	0	200	Level 1
00002B	PI5C16211	TSSOP / A56	Z9948AOC	76	0	100	Level 1
00004B	PI5C16215	TSSOP / A48	9923ASC	80	0	500*	Level 1
00012B	PI74ALVC16835	TSSOP / A56	9942INT	77	0	200	Level 1
00014B	PI74ALVCT16260	TSSOP / A56	9950RNT	75	0	200	Level 1
00026B	PI74ALVCT1622601	TSSOP / A56	0006ANT	76	0	200	Level 1
00036B	PI5C16211	TSSOP / A56	Z0010DNC	76	0	200	Level 1
00048B	PI5C16211	TSSOP / A56	Z0015DNC	74	0	200	Level 1
00057B	PI5C16861	TSSOP / A48	0022BOG	76	0	100	Level 1
00070B	PI5C16211	TSSOP / A56	Z0027COC	76	0	100	Level 1
00071B	PI5C16861	TSSOP / A48	0029LOG	76	0	100	Level 1
00075B	PI5C16211	TSSOP / A56	Z0025ANC	76	0	200	Level 1
00092B	PI5C16211	TSSOP / A56	Z0034GOC	76	0	100	Level 1
01068B	PI74SSTV16857	TSSOP / A48	0137AOC	76	0	500*	Level 1
02018-1A	PI5C16211	TSSOP / A56	Z0220AXC	100	0	500	Level 1

Note: the PI5C16215 device type uses the same design rules and CS2L313 SPTM process as the PI6CV857 product. The samples were subjected to 500 Preconditioned Temp Cycles at -65 C to +150 °C. The PI74SSTV16857 in a TSSOP-48 package uses the generically equivalent CS2L312 SPDM process, and was also subjected to 500 Preconditioned Temp Cycles at -65 C to +150 °C.

MOISTURE SENSITIVITY LEVEL OF PERICOM PACKAGES

Pericom's Integrated Circuit (IC) products are enclosed in plastic encapsulated or plastic covered substrate, Surface Mount Technology (SMT) packages. These have been evaluated by Moisture Sensitivity Testing (MST) and Moisture Resistance Testing (MRT) by Pericom and/or its assembly subcontractors and found to be in compliance with MSL requirements of the latest revisions to joint industry standards IPC/JEDEC J-STD-020A and JESD22-A113.

Pericom's SO (QSOP, SOIC (SOP), SSOP, TSSOP, SOT-23, and SC-70) and PLCC type packages have been determined to meet MSL 1 and therefore do not require any bake or dry pack prior to shipment. They are capable of withstanding 3 cycles of IR / Convection / Forced Air (N₂) reflow profiled to a recommended maximum peak temperature of 240°C. Customers do not need to store them in a specially controlled temperature and humidity environment prior to use. The floor life is unlimited at up to 30°C and 85% RH. No board mounting/reflow package damage should occur with product in these package types when utilizing industry standard SMT Reflow Solder profile methods and temperatures (including ramp rates and dwells).

Pericom's BGA (PBGA and LFBGA) and QFP (LQFP and TQFP) type packages have been determined to meet MSL 3 and therefore do require bake and dry pack prior to shipment. They are capable of withstanding three cycles of IR / Convection / Forced Air (N₂) reflow profiled to a recommended peak temperature of 225°C and a maximum peak temperature of 235°C. Customers do not need to store them in a specially controlled temperature and humidity environment prior to use provided they remain in tape and reel in a dry environment. The floor life is limited to 168 hours at up to 30°C and 60% RH. No board mounting/reflow package damage should occur with product in these package types when utilizing industry standard SMT Reflow Solder profile methods and temperatures (including ramp rates and dwells), if used within the shelf life period.

Pericom ensures maximum protection against moisture penetration because our plastic encapsulated/covered substrate packages are designed using the most appropriate epoxy and leadframe/substrate materials applicable to the type of package being assembled. Pericom's IC chips also use a silicon nitride (SN₂) topside passivation to help reduce the possibility of moisture corrosion to the device metallization.

PERICOM PLASTIC PACKAGE IMPROVEMENTS

Pericom pioneered the use of 240°C Moisture/Reflow Sensitivity testing back in 1998. Pericom is currently preparing to evaluate higher reflow temperatures up to 260°C to accommodate customer requirements for lead-free soldering. Pericom works very closely with our package assembly subcontractors to constantly improve the mechanical design of all plastic packages they supply. The following areas are addressed:

A. For Plastic Encapsulated SO/PLCC Packages:

- i) Mold Compound material changes to improve mechanical and moisture sensitivity*
- ii) Leadframe material/design changes to improve mechanical and thermal sensitivity*
- iii) Die Attach Epoxy material/process changes to improve mechanical sensitivity*

B. For Plastic Overmolded PBGA/LFBGA:

- i) Mold Compound material changes to improve mechanical and moisture sensitivity*
- ii) Substrate material changes to improve mechanical and moisture sensitivity*
- iii) Die Attach Epoxy material/process changes to improve mechanical sensitivity*

PACKAGE SOLDER REFLOW CONDITIONS

SO/PLCC Convection/Infrared/N₂ Reflow Soldering

Stage	Maximum	Recommended	Minimum
Ramp up (°C /sec)	3°C /sec.	<2°C /sec. *	**
Dwell Time @ 183°C	150 sec.	<120 sec. *	60 sec. **
Solder Temperature	240°C **	<240°C *	**
Dwell Time @ Max.	40 sec.	<20 sec.	**
Ramp Down (°C /sec.)	5°C /sec.	<4°C /sec.	**

PBGA/LFBGA Convection/Infrared/N₂ Reflow Soldering

Stage	Maximum	Recommended	Minimum
Ramp up (°C /sec)	3°C /sec	<2°C /sec *	**
Dwell Time @ 183°C	150 sec.	<60 sec. *	60 sec. **
Solder Temperature	235°C **	<225°C *	**
Dwell Time @ Max.	20 sec.	<10 sec.	**
Ramp Down (°C /sec.)	5°C /sec.	<4°C /sec.	**

Notes:

Temperature measured at the component lead area in degrees Celsius.

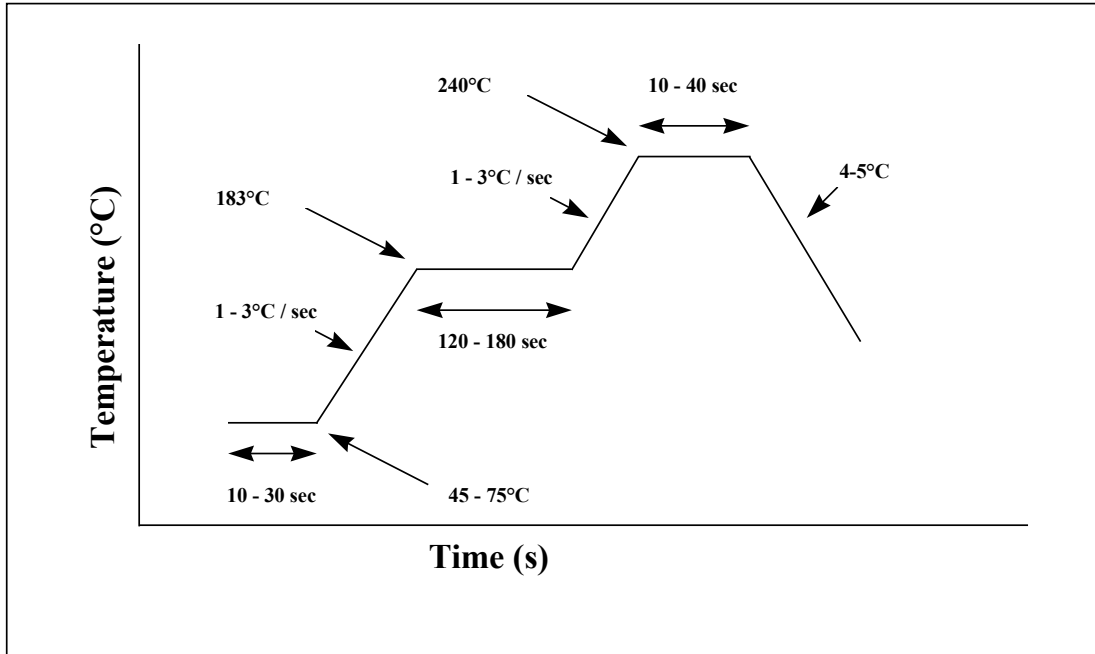
* Will vary depending on board density, geometry and package type; good for up to three cycles (2-reflow+1 rework)

** Will vary depending on package types and board density.

TYPICAL PACKAGE SOLDER REFLOW PROFILES



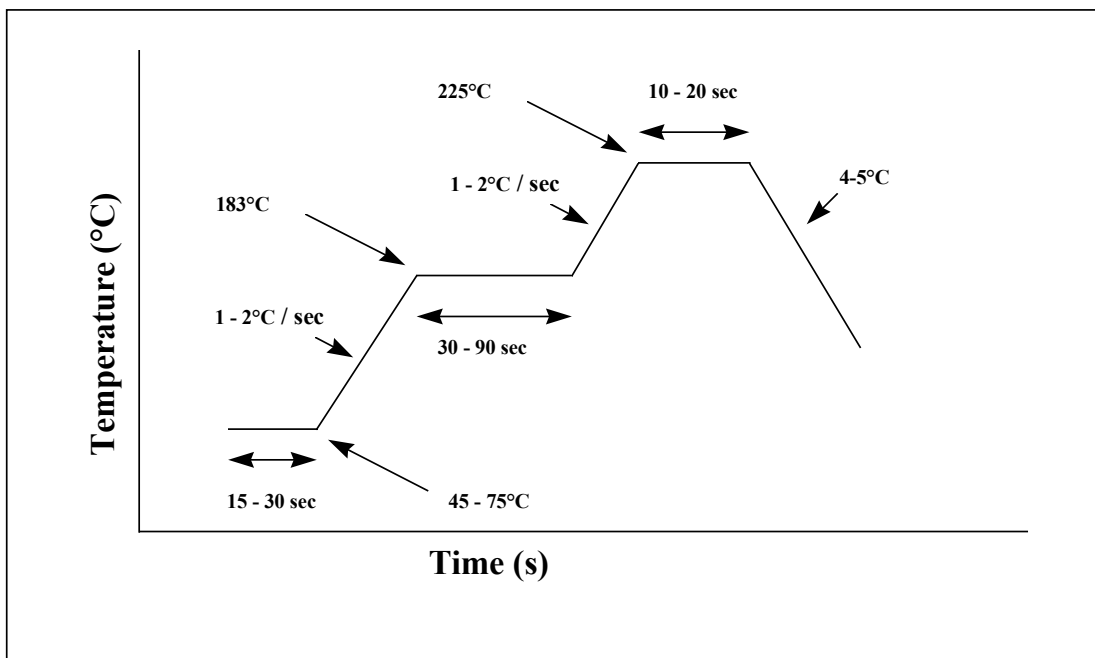
SO/PLCC Convection/IR +N₂ Solder Reflow Profile



01/01/01 issued by Pericom Semiconductor Corp.



PBGA/LFBGA Convection/IR Solder Reflow Profile



01/01/01 issued by Pericom Semiconductor Corp.