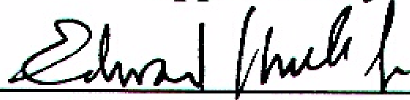
CSP Analog Switch Reliability Qualification Report

Built In Reliability

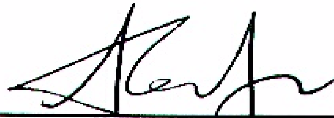
PH: 1.800.435.2336 | FX: 408.435.1100 | 3545 North First Street, San Jose, CA 95134

Reliability By Design

Approved by:



Edward J. Mello Jr., Director, Quality Systems



Alex Hui, President and CEO

INDEX:

Commitment To Quality: Page 4

Product Family:

- Wafer Fab Process: Page 5
- Wafer Fab Supplier: Page 5
- Assembly Subcontractor Page 5
- Process Technology: Page 5
- Product Group: Page 5
- Product Part Numbers & Descriptions (Table 1): Page 5
- Package Type Codes and Dimensions (Table 2): Page 6

Introduction:

- Analog Switches CSP (Figure [1]): Page 7

Reliability Testing Methodology: Page 7

- Reliability Process Qualification Tests: Page 8
- JEDEC Standard (Table 3): Page 8
- Test Condition (Table 4): Page 8

Process/Design Test Data:

- Latch-Up Test Data (Table 5): Page 9
- ESD Test Data (Table 6): Page 9
- Failure Rate Summary (Table 7) Page 10
- Dynamic High Temperature Operating Life (DHTOL)(Table 8): Page 11
- High Temperature Storage Test Data (HTSL) (Table 9): Page 11
- Temperature Cycle Test (TMCL) (Table 10): Page 11
- Biased Highly Accelerated Stress Testing (HAST) (Table 11): Page 11
- Un-biased Highly Accelerated Stress Testing (UHAST) (Table 12): Page 12

COMMITMENT TO QUALITY:

Pericom supports the Quality Systems and Management concepts of the ISO-9000 series of international standards for Quality. A corporate Quality Policy (detailed below) has been established as the basis of our commitment to maintain a world-class quality supplier status. Adhering to this policy is required for *all* employees, as Quality is not the responsibility of any one person or group; each and every employee shares it.

In recognition of our commitment, Pericom completed an ISO-9001 Registration Assessment Audit with Underwriter's Laboratories (UL), and Certificate Registration File Number A3151 was issued on March 27, 1995. We have successfully passed all Reassessment Audits since that time, and our Certificate is available for review on the Pericom website. For customers requiring Pericom's Commercial and Government Entity (CAGE) identification, our assigned code is 06MQ5

Quality Policy:

Pericom will deliver products and services that conform to customer requirements. We shall perform each job correctly the first time, emphasizing constant improvement in the quality of our work.

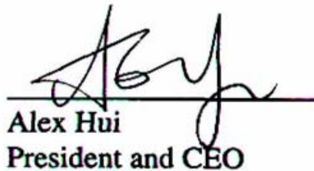
"Pericom will deliver..." - delivery, not just intentions, is one of the key measures of Pericom's commitment to deliver a quality product to customers.

"...products and services..." - quality performance is not limited to physical products; sending a letter without spelling errors, or promptly and politely answering a telephone are services which demand our best quality.

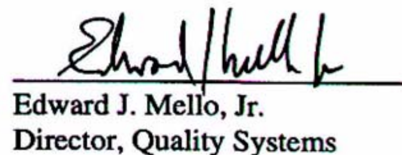
"...that conform to customer requirements." - a clear understanding of all requirements are needed *before* one can deliver quality products or services. This also signifies mutual agreement, with clear, two-way communications, which applies to customers within as well as outside the company. The entire Pericom team understands that each customer has a set of requirements and expectations that must be met.

"We shall perform each job correctly the first time, ..." - doing jobs correctly the first time means meeting agreements, that quality improvement measures are driven to determine the source of defects and preventing those defects from reoccurring. The continual *process* of preventing defects will drive down the costs we and our customer's experience, because costs associated with rework, redesign, etc. are dollars taken from being price competitive.

"...emphasizing constant improvement in the quality of our work." - each employee shall strive to find better, faster, more economical ways to perform their job, to ensure that quality continues to improve along with cost effectiveness.



Alex Hui
President and CEO



Edward J. Mello, Jr.
Director, Quality Systems

PERICOM PRODUCT FAMILY AND WAFER FAB PROCESS

The Pericom product data presented in this report qualifies the following products from a marketing defined product family manufactured on the following wafer fab process:

Product Family: ***Analog Switch***

Wafer Fab Process: ***MagnaChip, (ASP5)***

Wafer Supplier: ***MagnaChip (formerly Hynix Semiconductor), Korea***

Assembly Subcontractor: ***JCAP (Jiangyin Changdian Advanced Packaging Co., LTD, Jiangyin Jiangsu, China)***

Process Technology: ***0.5µm, 5.0V, Single-Poly Triple-Metal CMOS***

Product Group: ***5.0 Volt Analog Switch***

Table 1: List of Devices

Part Number*[1]	Product Description	Solder Balls	Packages*[2]
PI5A4213GAE*[3]	Dual SP3T Analog Switch, 3:1 Mux/DeMux Bus Switch, CSP – without backside coating	12	CSP
PI5A4213GBE*[3]	Dual SP3T Analog Switch, 3:1 Mux/DeMux Bus Switch, CSP – with backside coating	12	CSP
PI5A4684GAE	Dual SPDT Analog Switch, 2:1 Mux/DeMux Bus Switch, CSP - without backside coating	10	CSP
PI5A4684GBE	Dual SPDT Analog Switch, 2:1 Mux/DeMux Bus Switch, CSP - with backside coating	10	CSP
PI5A4763GAE	Dual SPDT Analog Switch with Headphone/Mute Detection, 2:1 Mux/DeMux Bus Switch (with Comparator), CSP - without backside coating	12	CSP
PI5A4764GAE	Dual SPDT Audio Clickless Analog Switch, 2:1 Mux/DeMux Bus Switch (with Shunt Switches), CSP - without backside coating	10	CSP
PI5A4764GBE	Dual SPDT Audio Clickless Analog Switch, 2:1 Mux/DeMux Bus Switch (with Shunt Switches), CSP – with backside Coating	10	CSP
PI5A4765GAE	Dual SPDT Audio Clickless Analog Switch with Headphone/Mute Detection, 2:1 Mux/DeMux Bus Switch with Comparator and Shunt, CSP- without backside coating	12	CSP

* Notes:

1. Part Number: 'E' indicate lead-free. All devices are only available with lead-free solder balls.
2. Package: 'CSP' Chip Scale Package. All devices are only sold in die form in tape and reel.
3. 'A' on the part numbers 'GAE' represents dies without backside coating. 'B' on the part numbers 'GBE' represents dies with backside coating.

AVAILABLE PACKAGE TYPE CODES AND DIMENSIONS

Table 2: List of Packages

CODE	TYPE	Solder Balls or Bump material and Dimensions
GA & GB	CSP- 10 & 12	Sn 96.8%, Ag 2.6%, Cu 0.6%, Bump Diameter: 370±20 µm, Bump Height: 285±20 µm, Die Thickness: 405±20 µm

PERICOM RELIABILITY TESTING METHODOLOGY

Pericom employs a commonly used industry method to generically qualify product. It is based on the premise that if one product of a specific wafer fab/package assembly process/materials is already qualified, then a second product that has similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second product without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.

The basis of this "qualification by similarity or extension" is the following rules:

A. For Wafer Fabrication Process and Materials:

- ***i) The wafer fabrication process technology and location are the same or similar***
- ***ii) The die array design rules and die size are the same or similar***
- ***iii) The standard and customized cell design and layout rules are the same or similar***
- ***iv) The density and complexity are the same or similar***
- ***v) The wafer fabrication materials are the same or similar***

B. For Package Assembly Process and Materials:

- ***i) The package assembly process technology and location are the same or similar***
- ***ii) The die paddle to package aspect ratio is the same or smaller***
- ***iii) The package dimensions width and thickness dimensions are the same or similar***
- ***iv) The leadframe/substrate design and lead/ball pitch are the same or similar***
- ***v) The package assembly materials are the same or similar***

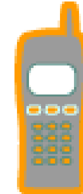
Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs. All parts within the same family are designed to the same rules, and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/ option, and only assembled on one package type process.

Introduction

PI5A4213, PI5A4684, PIA4763, PIA4764, and PIA4765: Analog Switch products based on the Chip Scale Package for mobile phone applications.

Pericom's family of analog switches are the highest performance, smallest switches available in the industry today. They are specifically designed for precision signal routing and switching in cell phones, wireless LAN, and any next-generation portable devices employing chip-scale package technology.

- Cellphone Application Notes
- Handheld Application Notes



Analog Switches is Cellular Phones

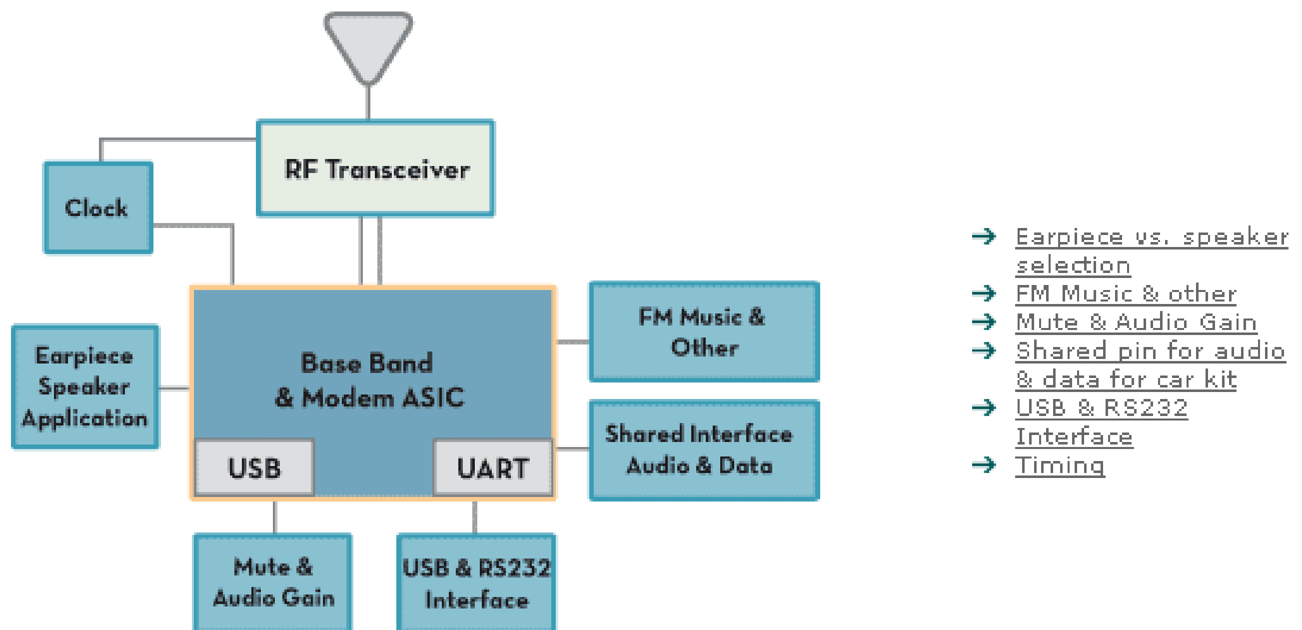


Figure [1]: Pericom Website: http://www.pericom.com/applications/cellphone.php

Reliability Process Qualification Tests

Table 3 – JEDEC Standard

PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)	PERICOM TEST CODE	EIA JEDEC STANDARD
Latch-Up Sensitivity	LU	JESD78
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	ESD – HBM	JESD22-A114-C
Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)	ESD – MM	JESD22-115-A
Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life)	DHTOL	JESD22-A108C
High Temperature Storage Life (Bake)	HTSL	JESD22-A103C
Unbiased Highly Accelerated Stress Testing	UHAST	JESD22-A118
Biased Highly Accelerated Stress Testing	HAST	JESD22-A118
Temperature Cycle Test	TMCL	JESD22-A104A

Table 4 – Test Condition

PERICOM Test Code (Refer to Table 3)	TEST Condition (Temp., Voltage, Cycles, Humidity, Time, Pressure)	Total Quantity/Number of Rejects (Number of Lots)	Amplitude or Duration Stress
LU	25°C	3/0 (1 lot)	≥200mA/ 5.5 V
ESD-HBM	25°C	3/0 (1 lot)	≥3000V(HBM)
ESD-MM	25°C	3/0 (1 lot)	≥200V(MM)
DHTOL	Temperature=150°C Voltage = 5.5 V (min. Bias: Vcc+10%)	274/0 (2 lots)	1000 & 500 Hrs.
HTSL	150°C (no bias)	91/0 (3 lots)	1000 Hrs.
TMCL	Condition C T_a = −65°C to +150°C 10 min dwell Cycles = 100 & 500 (Cumulative)	224/0 (3 lots)	100 & 500 Cycles (Cumulative)
HAST	T_a = 130°C RH= 85% P= 33.3 PSIG Voltage=5.5 V Time=96 hours	88/0 (2 lots)	96 Hrs.
UHAST	T_a = 130°C RH= 85% P= 33.3 PSIG Voltage=0 V Time=96 hours	48/0 (2 lots)	96 Hrs.

Process Latch-Up & ESD Characterization Data

Latch-Up Test (LU)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V Process

Table 5 – Latch-Up

Test	*Device*	*Date Code*	*SS*	*Rej.*	Vcc_{max}	T_a	*Remarks*
LU	PI5A4213	0505	3	0	5.5V	25°C	JESD78

ESD Test (ESD)
Human Body Model (HBM)
Machine Model (MM)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V

Table 6 – ESD

Test	*Device*	*Date Code*	*SS*	*Rej.*	V_{min}	T_a	*Remarks*
ESD-HBM	PI5A4213	0505	3	0	3000V	25°C	JESD22-A114-C
ESD-MM	PI5A4213	0505	3	0	200V	25°C	JESD22-115-A

Process High Temperature Biased & Storage Die Life Test Data

Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life) *(DHTOL)*

Reliability Failure Rate Summary

Table 7 – FIT & MTBF

Reliability Stress Test	REL Lot #	Devices Tested	Hours Tested	Device Hours	Number of Fails	Activation Energy (E_A) (ev)
DHTOL	QDG05003-1	126	1000	126,000	0	0.5
	QDG05003-2	148	500	74,000	0	0.5
Process Average	→	200	1000	200,000	0	0.5
FIT	→	→	→	→	→	***48.9***
MTBF / MTTF [1]	→	→	→	→	→	***20,449,898 Hrs.***

NOTES ON TABLE ABOVE AND ACCELERATION FACTORS:

1. *MTBF / MTTF* = Mean Time Between/To Failure = $1/F_r$ ($F_r \geq 1$)
2. *PPM* = parts per million = 10^{-6}
3. *FIT* = Failures In Time = $F_r \times 10^9$
4. F_r = Failure rate (% reject per 1000 hours) = $F_r \times 10^5 = \chi^2 (x, v)/2\ Ndt$
5. χ^2 = Chi-squared value
6. x = (1-CL) where CL = confidence level = 60%
7. v = (2N+2) = degrees of freedom where N is the number of rejects
8. *Ndt* = the equivalent device hours = device hours × AF
9. *Device hours* = devices tested × hours tested
10. *AF* = Acceleration Factor:
    - Arrhenius equation for accelerated temperature (A_t): $A_t = exp\{(-E_A/k)(1/T_2 - 1/T_1)\}$
    - Arrhenius equation for accelerated voltage (A_v): $A_v = exp\{C(V_S - V_o)\}$
11. A_t = thermal acceleration Factor
12. A_v = voltage acceleration Factor
13. E_A = average thermal activation energy for expected failure mechanisms = 0.5 eV
14. k = Boltzmann's constant = 8.62×10^{-5} eV/°K
15. T_1= life test operating temperature
16. T_2 = system use operating temperature = 55°C
17. C = constant that is a function of the dielectric thickness (t_{ox}) = $t_{ox}/100$
18. V_s = life test operating voltage
19. V_o = system use operating voltage

Dynamic High Temperature Operating Life Test (DHTOL)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V

Table 8 – DHTOL

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDG05003-1	PI5A4213GAE	GA-12	0509	126	0	1000	150°C	Vcc = 5.5 Volts
QDG05003-2	PI5A4213GAE	GA-12	0523	148	0	500	150°C	Vcc = 5.5 Volts

High Temperature Storage Life Test (HTSL)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V

Table 9 – HTSL

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDG05003-1B	PI5A4213GAE	GA-12	0509	45	0	1000	150°C	No Bias
QPA05009-1B	PI5A4684GAE	GA-10	0532	23	0	1000	150°C	No Bias
QPA05009-1B	PI5A4684GBE	GB-10	0532	23	0	1000	150°C	No Bias

Temperature Cycle Test (TMCL)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V

Table 10 – TMCL

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Cycles*	T_a	*Remarks*
QDG05003-2C	PI5A4213GAE	GA-12	0523	76	0	500	–65°C to +150°C	
QPA05009-1C	PI5A4684GAE	GA-10	0532	75	0	500	–65°C to +150°C	
QPA05009-1C	PI5A4684GBE	GB-10	0532	73	0	500	–65°C to +150°C	

Biased Highly Accelerated Stress Testing (HAST)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V

Table 11 – HAST

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDG05003-1D	PI5A4213GAE	GA-12	0509	43	0	96	130°C	Voltage=5.5 V RH= 85% P= 33.3 PSIG
QDG05003-2D	PI5A4213GAE	GA-12	0523	45	0	96	130°C	Voltage=5.5 V RH= 85% P= 33.3 PSIG

Un-biased Highly Accelerated Stress Testing (UHAST)

ASP5-ENG, MagnaChip 0.5um, 1P3M, 5V

Table 12 – UHAST

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QPA05009-1C	PI5A4684GAE	GA-10	0532	25	0	96	130°C	RH= 85% P= 33.3 PSIG Voltage=0 V
QPA05009-1C	PI5A4684GBE	GB-10	0532	23	0	96	130°C	RH= 85% P= 33.3 PSIG Voltage=0 V