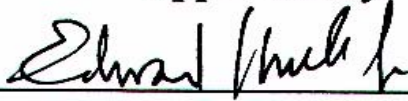


# **TSMC 0.35 $\mu\text{m}$ – 1Poly4Metal Wafer Fabrication Process Qualification Report**

*Built In Reliability*

# Reliability By Design

*Approved by:*



*Edward J. Mello Jr., Director, Quality Systems*



*Alex Hui, President and CEO*

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## COMMITMENT TO QUALITY:

Pericom supports the Quality Systems and Management concepts of the ISO-9000 series of international standards for Quality. A corporate Quality Policy (detailed below) has been established as the basis of our commitment to maintain a world-class quality supplier status. Adhering to this policy is required for *all* employees, as Quality is not the responsibility of any one person or group; each and every employee shares it.

In recognition of our commitment, Pericom completed an ISO-9001 Registration Assessment Audit with Underwriter's Laboratories (UL), and Certificate Registration File Number A3151 was issued on March 27, 1995. We have successfully passed all Reassessment Audits since that time, and our Certificate is available for review on the Pericom website. For customers requiring Pericom's Commercial and Government Entity (CAGE) identification, our assigned code is 06MQ5

### *Quality Policy:*

***Pericom will deliver products and services that conform to customer requirements. We shall perform each job correctly the first time, emphasizing constant improvement in the quality of our work.***


*"Pericom will deliver..."* - delivery, not just intentions, is one of the key measures of Pericom's commitment to deliver a quality product to customers.

*"...products and services..."* - quality performance is not limited to physical products; sending a letter without spelling errors, or promptly and politely answering a telephone are services which demand our best quality.

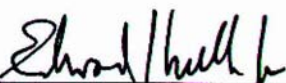
*"...that conform to customer requirements."* - a clear understanding of all requirements are needed *before* one can deliver quality products or services. This also signifies mutual agreement, with clear, two-way communications, which applies to customers within as well as outside the company. The entire Pericom team understands that each customer has a set of requirements and expectations that must be met.

*"We shall perform each job correctly the first time, ..."* - doing jobs correctly the first time means meeting agreements, that quality improvement measures are driven to determine the source of defects and preventing those defects from reoccurring. The continual *process* of preventing defects will drive down the costs we and our customer's experience, because costs associated with rework, redesign, etc. are dollars taken from being price competitive.

*"...emphasizing constant improvement in the quality of our work."* - each employee shall strive to find better, faster, more economical ways to perform their job, to ensure that quality continues to improve along with cost effectiveness.



Alex Hui  
President and CEO



Edward J. Mello, Jr.  
Director, Quality Systems

## PERICOM PRODUCT FAMILY AND WAFER FAB PROCESS

*The Pericom product data presented in this report qualifies the following products from a marketing defined product family manufactured on the following wafer fab process:*

<b><u>Product Family:</u></b>	<b><i>2-Port PCI-to-PCI Bridge</i></b>
<b><u>Wafer Fab Process:</u></b>	<b><i>TSMC (Taiwan Semiconductor Manufacturing Company Limited)</i></b>
<b><u>Wafer Supplier:</u></b>	<b><i>TSMC (Taiwan Semiconductor Manufacturing Company Limited)</i></b>
<b><u>Assembly Subcontractor:</u></b>	<b><i>ASE Electronics (M) (ASEM)</i></b>
<b><u>Process Technology:</u></b>	<b><i>0.35µm, 3.3V, Single-Poly Quadruple-Metal CMOS</i></b>
<b><u>Product Group:</u></b>	<b><i>3.3 Volt PCI-Express</i></b>

**Table 1: List of Devices**

Part Number* <sup>1</sup>	Product Description	Solder Balls	Packages* <sup>2</sup>
PI7C8150BND	Asynchronous 2-Port PCI-to-PCI Bridge	256	PBGA
PI7C8150BNDE		256	Pb-Free & Green PBGA
PI7C8150BMA		208	FQFP
PI7C8150BMAE		208	Pb-Free & Green FQFP

Note: Part Number: ‘E’ indicates lead-free and green.

### AVAILABLE PACKAGE TYPE CODES

**Table 2: List of Packages**

The following is the list of part number available for ordering. Refer to <http://www.pericom.com/pdf/datasheets/PI7C8150B.pdf>

## 18.3 PART NUMBER ORDERING INFORMATION

Part Number	Speed	Pin – Package	Temperature
PI7C8150BMA	66 MHz	208 – FQFP	0°C to 85°C
PI7C8150BND	66 MHz	256 – PBGA	0°C to 85°C
PI7C8150BMA-33	33 MHz	208 – FQFP	0°C to 85°C
PI7C8150BND-33	33 MHz	256 – PBGA	0°C to 85°C
PI7C8150BMAE	66 MHz	208 – FQFP (Pb-free & Green)	0°C to 85°C
PI7C8150BNDE	66 MHz	256 – PBGA (Pb-free & Green)	0°C to 85°C
PI7C8150BMAI	66 MHz	208 – FQFP	-40°C to 85°C
PI7C8150BNDI	66 MHz	256 – PBGA	-40°C to 85°C
PI7C8150BMAI-33	33 MHz	208 – FQFP	-40°C to 85°C
PI7C8150BNDI-33	33 MHz	256 – PBGA	-40°C to 85°C
PI7C8150BMAIE	66 MHz	208 – FQFP (Pb-free & Green)	-40°C to 85°C
PI7C8150BNDIE	66 MHz	256 – PBGA (Pb-free & Green)	-40°C to 85°C

## PERICOM RELIABILITY TESTING METHODOLOGY

*Pericom employs a commonly used industry method to generically qualify product. It is based on the premise that if one product of specific wafer fab/package assembly process/materials is already qualified, then a second product that has similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second product without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.*

*The basis of this “qualification by similarity or extension” is the following rules:*

*A. For Wafer Fabrication Process and Materials:*

- i) The wafer fabrication process technology and location are the same or similar*
- ii) The die array design rules and die size are the same or similar*
- iii) The standard and customized cell design and layout rules are the same or similar*
- iv) The density and complexity are the same or similar*
- v) The wafer fabrication materials are the same or similar*

*B. For Package Assembly Process and Materials:*

- i) The package assembly process technology and location are the same or similar*
- ii) The die paddle to package aspect ratio is the same or smaller*
- iii) The package dimensions width and thickness dimensions are the same or similar*
- iv) The leadframe/substrate design and lead/ball pitch are the same or similar*
- v) The package assembly materials are the same or similar*

*Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs. All parts within the same family are designed to the same rules, and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/option, and only assembled on one package type process.*

# Product Information

For further information on 2-Port PCI-to-PCI Bridge, products refer to Pericom website.

Pericom - Advanced Search - Part Number Search Results - Microsoft Internet Explorer

Address: <http://www.pericom.com/search/partIDsearch.php?partid=8150>

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### Search Results for "8150"

Part Number	Description	Family
<a href="#">PI7C8150A</a>	2-Port PCI-to-PCI Bridge	<a href="#">PCI Bridge</a>
<a href="#">PI7C8150A-33</a>	2-Port PCI-to-PCI Bridge	<a href="#">PCI Bridge</a>
<a href="#">PI7C8150B</a>	Asynchronous 2-Port PCI Bridge	<a href="#">PCI Bridge</a>
<a href="#">PI7C8150B-33</a>	Asynchronous 2-Port PCI Bridge	<a href="#">PCI Bridge</a>
<a href="#">PI7C8150BI</a>	Asynchronous 2-Port PCI Bridge	<a href="#">PCI Bridge</a>

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Figure [1]: Pericom Website: <http://www.pericom.com/search/partIDsearch.php?partid=8150>

## Reliability Process Qualification Tests

**Table 3 – JEDEC Standard**

<b>PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)</b>	<b>PERICOM TEST CODE</b>	<b>EIA JEDEC STANDARD</b>
Latch-Up Sensitivity	LU	JESD78
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	ESD – HBM	JESD22-A114-C
Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)	ESD – MM	JESD22-115-A
Electrostatic Discharge (ESD) Charged Device Model (CDM)	ESD – CDM	JESD22-C101C
Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life)	DHTOL	JESD22-A108C
High Temperature Storage Life (Bake)	HTSL	JESD22-A103C
Highly Accelerated Stress Testing	HAST	JESD22-A110-B
Temperature Cycle Test	TMCL	JESD22-A104C
Accelerated Moisture Resistance – Unbiased Autoclave	PCT	JESD22-A102-C

**Table 4 – Test Condition**

<b>PERICOM Test Code (Refer to Table 3)</b>	<b>TEST Condition (Temp., Voltage, Cycles, Humidity, Time, Pressure)</b>	<b>Total Quantity/Number of Rejects (Number of Lots)</b>	<b>Amplitude or Duration Stress</b>
LU	25°C	6/0 (1 lot)	≥200mA/ 4.0 V
ESD-HBM	25°C	5/0 (1 lot)	≥2000V(HBM)
ESD-MM	25°C	5/0 (1 lot)	≥200V(MM)
ESD-CDM	25°C	5/0 (1 lot)	≥500V(CDM)
DHTOL	Temperature=125°C Voltage = 3.6 V (min. Bias: Vcc+10%)	336/0 (3 lots)	168, 500, 1000 Hrs. (Cumulative)
HTSL	150°C (no bias)	45/0 (3 lots)	1000 Hrs.
HAST	T <sub>a</sub> = 130°C RH= 85% P= 33.3 PSIA Voltage=3.6 V Time=96 hours	45/0 (2 lots)	96 Hrs.
TMCL	Condition C T <sub>a</sub> = -65°C to +150°C 10 min dwell Cycles = 500	75/0 (3 lots)	500 Cycles
PCT	T <sub>a</sub> = 121°C RH= 100% P= 29.7 PSIA Voltage=0 V Time=96 hours	45/0 (2 lots)	96 Hrs.


# Process Latch-Up & ESD Characterization Data

## *Latch-Up Test (LU)*

*TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process*

**Table 5 – Latch-Up**

<i>Test</i>	<i>Device</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>V<sub>cc,max</sub></i>	<i>T<sub>a</sub></i>	<i>Remarks</i>
LU	PI7C8150B	B0610BT	6	0	4.0V	25°C	JESD78

*Refer to attachment for full report.* 

## *ESD Test (ESD)*




*Human Body Model (HBM)*

*Machine Model (MM)*

*Charged Device Model (CDM)*

*TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process*

**Table 6 – ESD**

<i>Test</i>	<i>Device</i>	<i>Date Code</i>	<i>SS</i>	<i>Rej.</i>	<i>V<sub>min</sub></i>	<i>T<sub>a</sub></i>	<i>Remarks</i>
ESD-HBM	PI7C8150B	B0610BT	5	0	2000V	25°C	JESD22-A114-C 
ESD-MM	PI7C8150B	B0610BT	5	0	200V	25°C	JESD22-115-A 
ESD-CDM	PI7C8150B	B0610BT	5	0	500V	25°C	JESD22-C101C 

*Refer to attachments for full report.*

# Process High Temperature Biased & Storage Die Life Test Data

## Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life) (DHTOL)

### Reliability Failure Rate Summary

**Table 7 – FIT & MTBF**

Reliability Stress Test	REL Lot #	Devices Tested	Hours Tested	Device Hours	Number of Fails	Activation Energy (E <sub>A</sub> ) (eV)
DHTOL	QDT06002-1	112	1000	112,000	0	0.5
DHTOL	QDT06002-2	112	1000	112,000	0	0.5
DHTOL	QDT06002-3	112	1000	112,000	0	0.5
Process Average	→	112	1000	112,000	0	0.5
<b>FIT</b>	→	→	→	→	→	<b>36.6</b>
<b>MTBF / MTTF<sup>1</sup></b>	→	→	→	→	→	<b>27,315,246 Hrs.</b>

### NOTES ON TABLE ABOVE AND ACCELERATION FACTORS:

1.  $MTBF / MTTF$  = Mean Time Between/To Failure =  $1/F_r$  ( $F_r \geq 1$ )
2.  $PPM$  = parts per million =  $10^{-6}$
3.  $FIT$  = Failures In Time =  $F_r \times 10^9$
4.  $F_r$  = Failure rate (% reject per 1000 hours) =  $F_r \times 10^5 = \chi^2(x, v)/2 Ndt$
5.  $\chi^2$  = Chi-squared value
6.  $x = (1-CL)$  where  $CL$  = confidence level = 60%
7.  $v = (2N+2)$  = degrees of freedom where  $N$  is the number of rejects
8.  $Ndt$  = the equivalent device hours = device hours  $\times$   $AF$
9.  $Device\ hours$  = devices tested  $\times$  hours tested
10.  $AF$  = Acceleration Factor:
  - Arrhenius equation for accelerated temperature ( $A_t$ ):  $A_t = \exp\{(-E_A/k)(1/T_2 - 1/T_1)\}$
  - Arrhenius equation for accelerated voltage ( $A_v$ ):  $A_v = \exp\{C(V_S - V_o)\}$
11.  $A_t$  = thermal acceleration Factor
12.  $A_v$  = voltage acceleration Factor
13.  $E_A$  = average thermal activation energy for expected failure mechanisms = 0.5 eV
14.  $k$  = Boltzmann's constant =  $8.62 \times 10^{-5}$  eV/°K
15.  $T_1$  = life test operating temperature
16.  $T_2$  = system use operating temperature = 55°C
17.  $C$  = constant that is a function of the dielectric thickness ( $t_{ox}$ ) =  $t_{ox}/100$
18.  $V_s$  = life test operating voltage
19.  $V_o$  = system use operating voltage

# Dynamic High Temperature Operating Life Test (DHTOL)

TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process

**Table 8 – DHTOL**

Lot #	Device	Date Code	Fab Lot	SS	Rej.	Hours	T <sub>a</sub>	Remarks
QDT06002-1	PI7C8150B	B0610BT	EH60175.1B	112	0	1000	125°C	Vcc = 3.6 Volts
QDT06002-2		B0633BT	H20402.4	112	0	1000		
QDT06002-3		B0641BT	H20905	112	0	1000		

# High Temperature Storage Life Test (HTSL)

TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process

**Table 9 – HTSL**

Lot #	Device	Date Code	SS	Rej.	Hours	T <sub>a</sub>	Remarks
QDT06002-1HTSL	PI7C8150B	B0610BT	15	0	1000	150°C	No Bias
QDT06002-2HTSL		B0633BT	15	0			
QDT06002-3HTSL		B0641BT	15	0			

# Highly Accelerated Stress Testing (HAST)

TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process

**Table 10 –HAST**

Lot #	Device	Package	Date Code	SS	Rej.	Hours	T <sub>a</sub>	Remarks
QDT06002-1HAST	PI7C8150B	PBGA-256 (ND-256)	B0610BT	15	0	96	130°C	RH= 85% P= 33.3 PSIA Voltage=3.6 V
QDT06002-2HAST			B0633BT	15	0			
QDT06002-3HAST			B0641BT	15	0			

# Temperature Cycle Test (TMCL)

TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process

**Table 11– TMCL**

Lot #	Device	Package	Date Code	SS	Rej.	Cycles	T <sub>a</sub>	Remarks
QDT06002-1TMCL	PI7C8150B	PBGA-256 (ND-256)	B0610BT	25	0	500	-65°C to +150°C	
QDT06002-2TMCL			B0633BT	25	0			
QDT06002-3TMCL			B0641BT	25	0			

# Accelerated Moisture Resistance – Unbiased Autoclave (PCT)

TSMC, 0.35 $\mu$ m 1P4M 3.3V CMOS Process

**Table 12 –PCT**

Lot #	Device	Package	Date Code	SS	Rej.	Hours	T <sub>a</sub>	Remarks
QDT06002-1PCT	PI7C8150B	PBGA-256 (ND-256)	B0610BT	15	0	96	121°C	RH= 100% P= 29.7 PSIA T = 121°C Voltage=0 V
QDT06002-2PCT			B0633BT	15	0			
QDT06002-3PCT			B0641BT	15	0			