PERICOM®
Enabling Serial Connectivity

TSMC 0.35µm – 2Poly3Metal

Wafer Fabrication Process

Qualification Report

Built In Reliability

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PERICOM PRODUCT FAMILY AND WAFER FAB PROCESS

The Pericom product data presented in this report qualifies the following products from a marketing defined product family manufactured on the following wafer fab process:

Product Family:	SerDes
Wafer Supplier:	Taiwan Semiconductor Manufacturing Corp – Taiwan (TSMC)
Process Technology:	0.35µm, Double-Poly Triple-Metal (2P3M) CMOS
Assembly Subcontractor:	ASE-Malaysia

Table 1: List of Devices

Part Number*[1]	Product Description	Solder Balls	Packages*[2]
PI90SD1636CFC	SerDes Gigabit Ethernet Transceiver	64	LQFP 10x10mm
PI90SD1636CFCE		64	LQFP 10x10mm
PI90SD1636CFD		64	LQFP 14x14mm
PI90SD1636CFDE		64	LQFP 14x14mm

Note: Part Number: 'E' indicates lead-free and green.

AVAILABLE PACKAGE TYPE CODES

Table 2: List of Packages

The following is the list of part number available for ordering. Refer to

http://www.pericom.com/pdf/datasheets/PI90SD1636C.pdf

Ordering Code	Package Code	Package Description
PI90SD1636CFC	FC	64-pin 10mm x10mm LQFP
PI90SD1636CFCE	FC	Pb-free & Green, 64-pin 10mm x10mm LQFP
PI90SD1636CFD	FD	64-pin 14mm x14mm LQFP
PI90SD1636CFDE	FD	Pb-free & Green, 64-pin 14mm x14mm LQFP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

Product Information

For further information on products refer to Pericom website.

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Search Results for "PI90SD1636C"

Part Number	Description	Family
PI90SD1636C	SerDes Gigabit Ethernet Transceiver	SerDes

» Products
» Cross-Reference Tools
» Packaging Information
» Product Change Notice
» Pb(Lead)-Free Info

Applications
» Market Segment Search
Search by Product Family
» Application Notes & Briefs
» Application Archive

» Technical Support
» Pb-free RoHS Help
» Contact Sales
» FAQ

Figure [1]: Pericom Website: http://www.pericom.com/products/serdes/PI90SD1636C/

PERICOM RELIABILITY TESTING METHODOLOGY

Pericom employs a commonly used industry method to generically qualify product. It is based on the premise that if one product of specific wafer fab/package assembly process/materials is already qualified, then a second product that has similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second product without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.

The basis of this "qualification by similarity or extension" is the following rules:

A. For Wafer Fabrication Process and Materials:

i) The wafer fabrication process technology and location are the same or similar

ii) The die array design rules and die size are the same or similar

iii) The standard and customized cell design and layout rules are the same or similar

iv) The density and complexity are the same or similar

v) The wafer fabrication materials are the same or similar

B. For Package Assembly Process and Materials:

i) The package assembly process technology and location are the same or similar

ii) The die paddle to package aspect ratio is the same or smaller

iii) The package dimensions width and thickness dimensions are the same or similar

iv) The leadframe/substrate design and lead/ball pitch are the same or similar

v) The package assembly materials are the same or similar

Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs. All parts within the same family are designed to the same rules, and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/ option, and only assembled on one package type process.

WAFER LEVEL RELIABILITY TESTING METHODOLOGY

WLR (Wafer Level Reliability) involves the valuation of a technology during the initial development and qualification, and ongoing monitors of these technologies at the wafer level to provide the earliest possible feedback. These evaluations are in addition to long-term operating life tests used to help qualify a wafer fabrication facility and process.

Special test structures have been developed between Pericom and our CMOS wafer fabrication subcontractors to evaluate the fundamental reliability of our design rules and technologies. Wafer Level Reliability test structures are designed to ensure reliability of thin oxides, metallization and dielectric structures, and basic transistor ruggedness.

The 2nd poly layer used for this process is for the PIP (Polysilicon-Insulator-Polysilicon) Capacitor, and has been evaluated by GOI test methods on this structure. Otherwise the process is exactly the same as it is for the Single poly process at TSMC.

Also evaluated as part of the WLR double poly process qualification was:

HCI (Hot Carrier Injection) testing is done on a test structure placed next to circuit die locations on the silicon wafer to confirm the reliability impact of highly energetic carriers into the gate oxide layer and the silicon substrate, resulting in volume charge build-up that can shift transistor threshold voltages.

GOI (Gate Oxide Integrity) tests performed on a test structure by stressing the oxide using the maximum allowable voltage across the oxide; it's comparing the measured leakage current to an acceptable limit that is based on the area of the gate oxide test device, and other factors which define acceptable versus unacceptable leakage levels.

VT (Threshold Voltage) Stability test is performed to determine if there's a voltage shift due to charge storage at the oxide-nitride interface, after exposure to high temperature for 168 hours.

The data summary in this report confirms the overall reliability of the CMOS 2P3M process used to manufacture this family of products.

Wafer Level Reliability Process Qualification Tests

(TSMC 0.35um, 2P3M)

Table 3 – Hot Carrier Injection (HCI) *(TSMC 0.35um, 2P3M)*

Description	**Condition**
Gate Oxide Thickness Channel Length	HV (12V): Tox=280A, 20/1.2_1.0_0.8um LV (3.3V): T0x=70A, 20/0.35um
Test Parameters	HV: A DUT is considered to fail if the Gm changes by more than 10%. Gm% change is defined as [(Gm(t=0)-Gm (t))/Gm(t=0)]*100 LV: A DUT is considered to fail if the Idsat changes by more that 10%. Idsat% change is defined as [(Idsat (t=0) - Idsat (t))/ Idsat (t=0)]*100, where Idsat (t=0) is the initial value and the Idsat(t) is the final values after stress time t. Idsat measured at Vgs=Vds=Vcc
Test Structure	HV: 20/1.2_1.0_0.8um (mask), oxide thickness: 280A with protection diode LV: 20/0.35 (mask), oxide thickness: 70A with protection diode
Vehicle	Packaged: DIP 18 ceramic package
Method	Temp: 25 +\-2 °C Duration: 168 hours Multiple stress cycles with a time accuracy of +/- 1% DC Bias Stress: Vgs are kept at Isub max. of Vds=1.1(Vcc), Vds<90% of breakdown. Vbs=0V
Model Used	1. HV device, Vds=13.2V, Vgs@Isub (max) 2. LV device, TTF =$(Isub^{-3})(Id^{2})$
Sample size	10 DUTs per lot. 3 lots.
Merit Number	Lifetime at 1.1Vcc
Spec	HV: AC TTF>100K hours @-55°C LV: DC (1.1Vcc) lifetime >0.2yrs @ 25°C

Conclusion: All samples passed qualification test.

Table 4 – Gate Oxide Integrity (GOI) *(TSMC 0.35um, 2P3M)*

Description	Condition
Test Vehicle	70A Bulk P-well: Area=1,000,000 um^2; edge length=4,000 um Bulk N-well: Area=1,000,000 um^2; edge length=4,000 um OD P-well: Area=633,600 um^2; OD Edge length=1,008,800um OD N-well: Area=633,600 um^2; OD Edge length=1,008,800um Poly Finger P-Well: Area=1,083,750 um^2; S/D edge length=722,500um Poly Finger N-Well: Area=1,083,750 um^2; S/D edge length=722,500um
	280A Bulk P-well: Area=1,000,000 um^2; edge length=4,000 um Bulk N-well: Area=1,000,000 um^2; edge length=4,000 um OD P-well: Area=1,000,000 um^2; OD Edge length=200,000um OD N-well: Area=1,000,000 um^2; OD Edge length=200,000um Poly Finger P-Well: Area=1,000,000 um^2; S/D edge length=202,000um Poly Finger N-Well: Area=1,000,000 um^2; S/D edge length=202,000um
Test Condition	70A Stress Mode: Accumulation Measurement Mode: Accumulation Ramp Rate (V/sec): 6.27V/sec (V_{step}=0.19V, T_{step}=0.03sec) Initial Voltage (V): 1.5V Measurement Voltage (V): 1.5V Failure is 15uA at 1.5V
	280A Stress Mode: Accumulation Measurement Mode: Accumulation Ramp Rate (V/sec): 6.27V/sec (V_{step}=0.19V, T_{step}=0.03sec) Initial Voltage (V): 12V Measurement Voltage (V): 12V Failure is 1uA at 12V
Failure Criteria	70A Mode A failure: Breakdown voltage (V_{bd}) </=3.3V Mode B failure: $3.3V<V_{bd}<8V$
	280A Mode A failure: Breakdown voltage (V_{bd}) </=12V Mode B failure: $12V<V_{bd}<29V$
Spec	Mode A: Do<5/cm^2 Mode B: Do<1/cm^2
Sample Size	Lot 1:(6 structure X 350 samples) + (8 structure X 350 samples)=4900 samples Lot 2:(6 structure X 250 samples) + (8 structure X 250 samples)=3500 samples Lot 2:(6 structure X 250 samples) + (8 structure X 250 samples)=3500 samples

Conclusion: All samples passed qualification test.

Table 5 – Polysilicon-Insulator-Polysilicon **(PIP)** *(TSMC 0.35um, 2P3M)*

Description	**Condition**
Test Vehicle	370A CAP8: Area=48,910um^2
Test Condition	370A Stress Mode: Accumulation Measurement Mode: Accumulation Ramp Rate (V/sec): 6.27V/sec (V_{step}=0.19V, T_{step}=0.03sec) Initial Voltage (V): 12V Measurement Voltage (V): 12V Failure is 1uA at 12V
Failure Criteria	370A Mode A failure: Breakdown voltage (V_{bd}) </=12V Mode B failure: $12V<V_{bd}<29V$
Spec	Mode A: Do<5/cm^2 Mode B: Do<1/cm^2
Sample Size	Lot 1: 1 structure x 350 samples =350 samples Lot 2: 1 structure x 250 samples= 250 samples Lot 3: 1 structure x 250 samples= 250 samples

Conclusion: All samples passed qualification test.

Table 6 – Voltage Threshold (VT) Stability *(TSMC 0.35um, 2P3M)*

Description	**Condition**
Test Parameters	A DUT is considered to fail if the Vt shifts by more than 15% Vt (ini) on active transistor.
Test Structure	N/P type: mask gate size: W/L=20/0.35um for 3.3V device N/P type: mask gate size: W/L=20/1.2_1.0um for 12V asymmetric and symmetric device
Vt Definition	Extrapolation method form |Ids| at Gm_{max} |Vds|=0.1V, Vs=Vb=GND
Method	1. Measure Vt(ini) at room temp 2. 168 hours stress (Vg=Vcc+10% @inversion mode, Vs=Vb=Vd=GND, oven temp at 150°C 3. Measure Vt(ini) at room temp 4. Vt shift percentage = [Vt(final)-Vt(ini)]/Vt(ini) x100
Sample Size	10 transistors for each test structure
Merit Number	Vt shift percentage

Conclusion: All samples passed qualification test.

SUPPLEMENTAL RELIABITIY DATA

TSMC, 0.35um, 1P4m 3.3V CMOS Process

The Pericom product data presented in this report qualifies the following products from a marketing defined product family manufactured on the following wafer fab process:

Product Family: ***2-Port PCI-to-PCI Bridge***

Wafer Fab Process: ***TSMC (Taiwan Semiconductor Manufacturing Company Limited)***

Wafer Supplier: ***TSMC (Taiwan Semiconductor Manufacturing Company Limited)***

Assembly Subcontractor: ***ASE Electronics (M) (ASEM)***

Process Technology: ***0.35µm, 3.3V, Single-Poly Quadruple-Metal CMOS***

Product Group: ***3.3 Volt PCI-Express***

Reliability Process Qualification Tests

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 7 – JEDEC Standard

PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)	PERICOM TEST CODE	EIA JEDEC STANDARD
Latch-Up Sensitivity	LU	JESD78
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	ESD – HBM	JESD22-A114-C
Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)	ESD – MM	JESD22-115-A
Electrostatic Discharge (ESD) Charged Device Model (CDM)	ESD – CDM	JESD22-C101C
Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life)	DHTOL	JESD22-A108C
High Temperature Storage Life (Bake)	HTSL	JESD22-A103C
Highly Accelerated Stress Testing	HAST	JESD22-A110-B
Temperature Cycle Test	TMCL	JESD22-A104C
Accelerated Moisture Resistance – Unbiased Autoclave	PCT	JESD22-A102-C

Table 8 – Test Condition

PERICOM Test Code (Refer to Table 3)	TEST Condition (Temp., Voltage, Cycles, Humidity, Time, Pressure)	Total Quantity/Number of Rejects (Number of Lots)	Amplitude or Duration Stress
LU	25°C	6/0 (1 lot)	≥200mA/ 4.0 V
ESD-HBM	25°C	5/0 (1 lot)	≥2000V(HBM)
ESD-MM	25°C	5/0 (1 lot)	≥200V(MM)
ESD-CDM	25°C	5/0 (1 lot)	≥500V(CDM)
DHTOL	Temperature=125°C Voltage = 3.6 V (min. Bias: Vcc+10%)	336/0 (3 lots)	168, 500, 1000 Hrs. (Cumulative)
HTSL	150°C (no bias)	45/0 (3 lots)	1000 Hrs.
HAST	T_a = 130°C RH= 85% P= 33.3 PSIA Voltage=3.6 V Time=96 hours	45/0 (2 lots)	96 Hrs.
TMCL	Condition C T_a = −65°C to +150°C 10 min dwell Cycles = 500	75/0 (3 lots)	500 Cycles
PCT	T_a = 121°C RH= 100% P= 29.7 PSIA Voltage=0 V Time=96 hours	45/0 (2 lots)	96 Hrs.

Process Latch-Up & ESD Characterization Data

Latch-Up Test (LU)

TSMC, 0.35μm 1P4M 3.3V CMOS Process

Table 9 – Latch-Up

Test	*Device*	*Date Code*	*SS*	*Rej.*	Vcc_{max}	T_a	*Remarks*
LU	PI7C8150B	B0610BT	6	0	4.0V	25°C	JESD78

ESD Test (ESD)
Human Body Model (HBM)
Machine Model (MM)
Charged Device Model (CDM)

TSMC, 0.35μm 1P4M 3.3V CMOS Process

Table 10 – ESD

Test	*Device*	*Date Code*	*SS*	*Rej.*	V_{min}	T_a	*Remarks*
ESD-HBM	PI7C8150B	B0610BT	5	0	2000V	25°C	JESD22-A114-C
ESD-MM	PI7C8150B	B0610BT	5	0	200V	25°C	JESD22-115-A
ESD-CDM	PI7C8150B	B0610BT	5	0	500V	25°C	JESD22-C101C

High Temperature Biased & Storage Die Life Test Data

Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life) *(DHTOL)*

Reliability Failure Rate Summary

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 11 – FIT & MTBF

Reliability Stress Test	**REL Lot #**	**Devices Tested**	**Hours Tested**	**Device Hours**	**Number of Fails**	**Activation Energy (E_A) (ev)**
DHTOL	QDT06002-1	112	1000	112,000	0	0.5
DHTOL	QDT06002-2	112	1000	112,000	0	0.5
DHTOL	QDT06002-3	112	1000	112,000	0	0.5
Process Average	→	112	1000	112,000	0	0.5
FIT	→	→	→	→	→	***36.6***
MTBF / MTTF [1]	→	→	→	→	→	***27,315,246 Hrs.***

NOTES ON TABLE ABOVE AND ACCELERATION FACTORS:

1. *MTBF / MTTF* = Mean Time Between/To Failure = $1/F_r$ ($F_r \geq 1$)
2. *PPM* = parts per million = 10^{-6}
3. *FIT* = Failures In Time = $F_r \times 10^9$
4. F_r = Failure rate (% reject per 1000 hours) = $F_r \times 10^5 = \chi^2$ (x, v)/2 Ndt
5. χ^2 = Chi-squared value
6. *x* = (1-CL) where CL = confidence level = 60%
7. *v* = (2N+2) = degrees of freedom where N is the number of rejects
8. *Ndt* = the equivalent device hours = device hours × AF
9. *Device hours* = devices tested × hours tested
10. *AF* = Acceleration Factor:
    - Arrhenius equation for accelerated temperature (A_t): $A_t = exp\{(-E_A/k)(1/T_2 - 1/T_1)\}$
    - Arrhenius equation for accelerated voltage (A_v): $A_v = exp\{C(V_S - V_o)\}$
11. A_t = thermal acceleration Factor
12. A_v = voltage acceleration Factor
13. E_A = average thermal activation energy for expected failure mechanisms = 0.5 eV
14. *k* = Boltzmann's constant = 8.62×10^{-5} eV/°K
15. T_1= life test operating temperature
16. T_2 = system use operating temperature = 55°C
17. *C* = constant that is a function of the dielectric thickness (t_{ox}) = $t_{ox}/100$
18. V_s = life test operating voltage
19. V_o = system use operating voltage

Dynamic High Temperature Operating Life Test (DHTOL)

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 12 – DHTOL

Lot #	*Device*	*Date Code*	*Fab Lot*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDT06002-1	PI7C8150B	B0610BT	EH60175.1B	112	0	1000	125°C	Vcc = 3.6 Volts
QDT06002-2		B0633BT	H20402.4	112	0	1000		
QDT06002-3		B0641BT	H20905	112	0	1000		

High Temperature Storage Life Test (HTSL)

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 13 – HTSL

Lot #	*Device*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDT06002-1HTSL	PI7C8150B	B0610BT	15	0	1000	150°C	No Bias
QDT06002-2HTSL		B0633BT	15	0			
QDT06002-3HTSL		B0641BT	15	0			

Highly Accelerated Stress Testing (HAST)

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 14 –HAST

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDT06002-1HAST	PI7C8150B	PBGA-256 (ND-256)	B0610BT	15	0	96	130°C	RH= 85% P= 33.3 PSIA Voltage=3.6 V
QDT06002-2HAST			B0633BT	15	0			
QDT06002-3HAST			B0641BT	15	0			

Temperature Cycle Test (TMCL)

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 15– TMCL

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Cycles*	T_a	*Remarks*
QDT06002-1TMCL	PI7C8150B	PBGA-256 (ND-256)	B0610BT	25	0	500	–65°C to +150°C	
QDT06002-2TMCL			B0633BT	25	0			
QDT06002-3TMCL			B0641BT	25	0			

Accelerated Moisture Resistance – Unbiased Autoclave (PCT)

TSMC, 0.35µm 1P4M 3.3V CMOS Process

Table 16 –PCT

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDT06002-1PCT	PI7C8150B	PBGA-256 (ND-256)	B0610BT	15	0	96	121°C	RH= 100% P= 29.7 PSIA T = 121°C Voltage=0 V
QDT06002-2PCT			B0633BT	15	0			
QDT06002-3PCT			B0641BT	15	0			