PERICOM®
Enabling Serial Connectivity

CSM 0.18 µm – 1Poly3Metal

Wafer Fabrication Process

Qualification Report

Built In Reliability

Prepared by: P. Finer Sr. Quality Engineer

PH: 1.800.435.2336 | FX: 408.435.1100 | 3545 North First Street, San Jose, CA 95134

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PERICOM PRODUCT FAMILY AND WAFER FAB PROCESS

The Pericom product data presented in this report qualifies the following products from a marketing defined product family manufactured on the following wafer fab process:

Product Family: Specialty Interface
Wafer Supplier: Charter Semiconductor Manufacturing – Singapore (C) (CSM)
Assembly Subcontractor: OSE – Taiwan (O)
Process Technology: 0.18µm, 1.8V, Single-Poly Triple-Metal (1P3M) CMOS
Product Group: Configurable Registered Buffer

Table 1: List of Devices

Part Number*[1]	Product Description	Solder Balls	Packages*[2]
PI74SSTU32866NB	Configurable Registered Buffer with Parity	96	LFBGA
PI74SSTU32866NBE		96	Pb-Free & Green LFBGA

Note: Part Number: 'E' indicates lead-free and green.

AVAILABLE PACKAGE TYPE CODES

Table 2: List of Packages

The following is the list of part number available for ordering. Refer to

http://www.pericom.com/pdf/datasheets/PI74SSTU32866.pdf

Ordering Information (1,2,3)

Ordering Code	Package Code	Package Type
PI74SSTU32866NB	NB	96-Ball LFBGA
PI74SSTU32866NBE	NB	Pb-free & Green, 96-Ball LFBGA

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. X suffix = Tape/Reel

PERICOM RELIABILITY TESTING METHODOLOGY

Pericom employs a commonly used industry method to generically qualify product. It is based on the premise that if one product of specific wafer fab/package assembly process/materials is already qualified, then a second product that has similar design, manufacturing process, and materials can be qualified by extending the data used to qualify the first product to the second product without generating additional data. This methodology allows the ability to benchmark suppliers to ensure continuous process improvements and minimize cost and time required for new product availability.

The basis of this "qualification by similarity or extension" is the following rules:

A. For Wafer Fabrication Process and Materials:

- ***i)*** The wafer fabrication process technology and location are the same or similar
- ***ii)*** The die array design rules and die size are the same or similar
- ***iii)*** The standard and customized cell design and layout rules are the same or similar
- ***iv)*** The density and complexity are the same or similar
- ***v)*** The wafer fabrication materials are the same or similar

B. For Package Assembly Process and Materials:

- ***i)*** The package assembly process technology and location are the same or similar
- ***ii)*** The die paddle to package aspect ratio is the same or smaller
- ***iii)*** The package dimensions width and thickness dimensions are the same or similar
- ***iv)*** The leadframe/substrate design and lead/ball pitch are the same or similar
- ***v)*** The package assembly materials are the same or similar

Where a product of interest is not sampled during this period, it is valid to use the reliability data of the particular process technology or package type family to which the part belongs. All parts within the same family are designed to the same rules, and manufacturing is controlled by SPC. Within a product family, a device can only be fabricated on one process technology/ option, and only assembled on one package type process.

Product Information

For further information on Configurable Registered Buffers, products refer to Pericom website.

PERICOM Enabling Serial Connectivity

Search Results for "pi74sstu32"

Part Number	Description	Family
PI74SSTU32864	DDR-II, 25-Bit 1:1 or 14-Bit 1:2 Configurable Registered Buffer	Specialty Interface
PI74SSTU32864A	DDR2, 25-Bit 1:1 or 14-Bit 1:2 Configurable Registered Buffer	Specialty Interface
PI74SSTU32866	DDR2, 25-Bit 1:1 or 14-Bit 1:2 Configurable Registered Buffer w/parity	Specialty Interface

Figure [1]: Pericom Website: http://www.pericom.com/search/partIDsearch.php?partid=pi74sstu32

Reliability Process Qualification Tests

Table 3 – JEDEC Standard

PERICOM RELIABILITY TEST DESCRIPTION (ALTERNATIVE NAME)	PERICOM TEST CODE	EIA JEDEC STANDARD
Latch-Up Sensitivity	LU	JESD78
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	ESD – HBM	JESD22-A114-E
Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)	ESD – MM	JESD22-A115-A
Electrostatic Discharge (ESD) Charged Device Model (CDM)	ESD – CDM	JESD22-C101-C
Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life)	DHTOL	JESD22-A108-C
High Temperature Storage Life (Bake)	HTSL	JESD22-A103-C
Temperature Cycle Test	TMCL	JESD22-A104-C

Table 4 – Test Condition

PERICOM Test Code (Refer to Table 3)	TEST Condition (Temp., Voltage, Cycles, Humidity, Time, Pressure)	Total Quantity/Number of Rejects (Number of Lots)	Amplitude or Duration Stress
LU	25°C	6/0 (1 lot)	≥200mA/ 1.98 V
ESD-HBM	25°C	3/0 (1 lot)	≥2000V(HBM)
ESD-MM	25°C	3/0 (1 lot)	≥200V(MM)
ESD-CDM	25°C	3/0 (1 lot)	≥500V(CDM)
DHTOL	Temperature =125°C Voltage = 3.6 V (min. Bias: Vcc+10%)	149/0 (1 lot)	168, 500, 1000 Hrs. (Cumulative)
HTSL	150°C (no bias)	40/0 (2 lots)	1000 Hrs.
TMCL	Condition C T_a = −65°C to +150°C 10 min dwell Cycles = 500	75/0 (2 lots)	500 Cycles

Process Latch-Up & ESD Characterization Data

Latch-Up Test (LU)

CSM-S, 0.18µm, 1P3M, 1.9V CMOS Process

Table 5 – Latch-Up

Test	*Device*	*Date Code*	*SS*	*Rej.*	*Vcc_{max}*	*T_a*	*Remarks*
LU	PI74SSTU32866	0547OC	6	0	4.0V	25°C	JESD78

Refer to attachment for full report.

ESD Test (ESD)
Human Body Model (HBM)
Machine Model (MM)
Charged Device Model (CDM)

CSM-S, 0.18µm, 1P3M, 1.9V CMOS Process

Table 6 – ESD

Test	*Device*	*Date Code*	*SS*	*Rej.*	*V_{min}*	*T_a*	*Remarks*
ESD-HBM	PI74SSTU32866	0547OC	3	0	2000V	25°C	JESD22-A114-E
ESD-MM	PI74SSTU32866	0547OC	3	0	200V	25°C	JESD22-A115-A
ESD-CDM	PI74SSTU32866	0547OC	3	0	500V	25°C	JESD22-C101-C

Refer to attachments for HBM and CDM reports.

Process High Temperature Biased & Storage Die Life Test Data

Temperature, Bias, and Operating Life (Dynamic High Temperature Operating Life) *(DHTOL)*

Reliability Failure Rate Summary

Table 7 – FIT & MTBF

Reliability Stress Test	REL Lot #	Devices Tested	Hours Tested	Device Hours	Number of Fails	Activation Energy (E_A) (ev)
DHTOL	QDC08001-1	149	1000	149,000	0	0.5
FIT	→	→	→	→	→	104
MTBF / MTTF [1]	→	→	→	→	→	9.624E+06

NOTES ON TABLE ABOVE AND ACCELERATION FACTORS:

1. *MTBF / MTTF* = Mean Time Between/To Failure = $1/F_r$ ($F_r \geq 1$)
2. *PPM* = parts per million = 10^{-6}
3. *FIT* = Failures In Time = $F_r \times 10^9$
4. F_r = Failure rate (% reject per 1000 hours) = $F_r \times 10^5 = \chi^2$ (x, v)/2 Ndt
5. χ^2 = Chi-squared value
6. *x* = (1-CL) where CL = confidence level = 60%
7. *v* = (2N+2) = degrees of freedom where N is the number of rejects
8. *Ndt* = the equivalent device hours = device hours × AF
9. *Device hours* = devices tested × hours tested
10. *AF* = Acceleration Factor:
    - Arrhenius equation for accelerated temperature (A_t): $A_t = exp\{(-E_A/k)(1/T_2 - 1/T_1)\}$
    - Arrhenius equation for accelerated voltage (A_v): $A_v = exp\{C(V_S - V_o)\}$
11. A_t = thermal acceleration Factor
12. A_v = voltage acceleration Factor
13. E_A = average thermal activation energy for expected failure mechanisms = 0.5 eV
14. *k* = Boltzmann's constant = 8.62×10^{-5} eV/°K
15. T_1= life test operating temperature
16. T_2 = system use operating temperature = 55°C
17. *C* = constant that is a function of the dielectric thickness (t_{ox}) = $t_{ox}/100$
18. V_s = life test operating voltage
19. V_o = system use operating voltage

Dynamic High Temperature Operating Life Test (DHTOL)

CSM-S, 0.18µm, 1P3M, 1.9V CMOS Process

Table 8 – DHTOL

Lot #	*Device*	*Date Code*	*Fab Lot*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDC08001-1	PI74SSTU32866	0547OC	6PIB21097.1	149	0	1000	150°C	Vcc = 1.9 Volts

High Temperature Storage Life Test (HTSL)

CSM-S, 0.18µm, 1P3M, 1.9V CMOS Process

Table 8 – HTSL

Lot #	*Device*	*Date Code*	*SS*	*Rej.*	*Hours*	T_a	*Remarks*
QDC08001-1	PI74SSTU32866	0547OC	40	0	1000	150°C	No Bias

Temperature Cycle Test (TMCL)

CSM-S, 0.18µm, 1P3M, 1.9V CMOS Process

Table 9 – TMCL

Lot #	*Device*	*Package*	*Date Code*	*SS*	*Rej.*	*Cycles*	T_a	*Remarks*
QDC08001-1	PI74SSTU32866	LFBGA-96 (NB-96)	0547OC	75	0	500	–65°C to +150°C	

TO: All
FROM: Pericom Semiconductor Corporation
SUBJECT: PI74SSTU32866 Charged Device Mode (CDM) ESD Test Results
DATE: 03/20/08

Part ID:

Part Number: PI74SSTU32866
Date code: D/C: 0547OC
Lot #: 6PIB21097.1

Process:

Wafer Foundry: Charter Semiconductor Corp., Singapore
Process: 0.18um 1P3M process

Summary

3 samples of PI74SSTU32866 devices were used for CDM ESD testing with RCDM ESD machine per EIA/JESD22-C101C standard at 500V. Post-ESD parts were tested with the standard Production Test Program.

Unit #	ESD Voltage (V)	Pass / Fail	Production Test Program and Bench Test Failure Modes
1	500	Pass	None
2	500	Pass	None
3	500	Pass	None

Conclusions

We confirmed that PI74SSTU32866 (CSM 0.18um, SPTM) from Lot# 6PIB21097.1 D/C: 0547OC passed the CDM-ESD test at 500V per EIA/JESD22-101C.

TO: All
FROM: Pericom Semiconductor Corporation
SUBJECT: PI74SSTU32866 Latch-up Test Results
DATE: 03/20/08

Part ID:

Part Number: PI74SSTU32866
Date code: D/C: 0547OC
Lot #: 6PIB21097.1
Quantity: 6

Test Instruments:

E3610A. DC power supply. Vcc=1.98V. Icc is clamped at 220mA.
HP4145B. Trigger current source. Max current +/-200mA (two channels in parallel).

Summary:

Device PI74SSTU32866 is subjected to latch-up test with HP4145B and E3610A DC power supply. Prior to current injection, there is no perceivable Icc current flowing when power supply is on Max Icc current during the injection for all the pins is about 90mA, but it will come back to initial value when injection current stops. There is no latch-up issue for PI74SSTU32866.

Conclusion

We confirmed that device PI74SSTU32866 from lot# 6PIB21097.1, date code: 0547OC does not have latch-up issue under +/- 200mA current injection according to EIA/JESD78.

TO: All
FROM: Pericom Semiconductor Corporation
SUBJECT: PI74SSTU32866 Human Body Model (HBM) ESD Test Results
DATE: 03/20/08

Part ID:

Part Number: PI74SSTU32866
Date code: D/C: 0547OC
Lot #: 6PIB21097.1

Process:

Wafer Foundry: Charter Semiconductor Corp., Singapore
Process: 0.18um 1P3M process

Summary

3 samples of PI74SSTU32866 devices were used for HBM ESD testing with ZapMaster ESD machine per EIA/JESD22-A114E standard at 2000V. Post-ESD parts were tested with the standard Production Test Program.

Unit #	ESD Voltage (V)	Pass / Fail	Production Test Program and Bench Test Failure Modes
1	2000	Pass	None
2	2000	Pass	None
3	2000	Pass	None

Conclusions

We confirmed that PI74SSTU32866 (CSM 0.18um, SPTM) from Lot# 6PIB21097.1 D/C: 0547OC passed the HBM-ESD test at 2000V per EIA/JESD22-A114E.