



PI7C8150B
ASYNCHRONOUS 2-PORT
PCI-to-PCI BRIDGE
ERRATA
Revision 1.01

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REVISION HISTORY

DATE	REVISION	DESCRIPTION
06/18/2003	1.0	First release of errata
08/27/2003	1.01	Added Errata #2 – Incorrect Master Abort Status

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INTRODUCTION

This document is a summary of known errata for the PI7C8150B, 2-port PCI-to-PCI Bridge. It describes what each erratum is and provides the status of whether or not it will be corrected. As the device is used in more applications, this document is subject to change.

SILICON REVISIONS

REVISION	DESCRIPTION	
2.0	PI7C8150B initial release	

SUMMARY OF ERRATA

ERRATA #	DESCRIPTION	STATUS
1	Subtractive Decode misinterpreted as a Master Abort	No current workarounds.
2	Incorrect Master Abort Status	No current workarounds.

1. Subtractive Decode Mistaken as a Master Abort.

Problem: The PI7C8150B cannot accept any subtractive decode target transactions on the bus. Any subtractive decode target transactions through the bridge will be interpreted incorrectly as a master abort by the PI7C8150B. When PI7C8150B does not see any assertion for fast decoding, medium decoding, or slow decoding, PI7C8150B will interpret the transaction as a master abort.

Workaround: There are currently no workarounds for this issue.

Status: Issue will be addressed in the next revision of silicon.

2. Incorrect Master Abort Status

Problem: When a device wants to issue a broadcast transaction through the PI7C8150B, it sends a Type 1 transaction to the PI7C8150B. The PI7C8150B then converts that to a Special Cycle transaction. No other device will claim the transaction because it is a broadcast transaction. However, the PI7C8150B may misinterpret this as a master abort and as a result, may incorrectly set the master abort status bits (bit[29] at offset 04h or 1Ch).

Workaround: There are currently no workarounds for this issue.

Status: Issue will be addressed in the next revision of silicon.