



3-PORT PCI-to-PCI BRIDGE  
PI7C7300A  
ERRATA

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## REVISION HISTORY

<b>DATE</b>	<b>REVISION</b>	<b>DESCRIPTION</b>
8/13/01	1.0	Added errata 1.
11/27/01	1.1	Added errata 2.
5/6/04	1.2	Added errata 3.

## INTRODUCTION

This document is a summary of known errata for the 3-Port PCI-to-PCI Bridge (PI7C7300A). It describes what each erratum is and provides the status of whether or not it will be corrected. As the device is used in more applications, this document may change.

## SILICON REVISIONS

REVISION	DESCRIPTION	
PI7C7300E	First Engineering Samples	
PI7C7300A	Revised Silicon to correct errata 1	

## SUMMARY OF ERRATA

ERRATA #	DESCRIPTION	STATUS
1	The Read Data Buffer can be overwritten causing the data provided to the initiator to be incorrect.	Fixed in latest revision of silicon.
2	Possible issue may result when there are upstream write cycles and the bridge is running at 66MHz primary and 33MHz secondary	No workarounds available
3	Data Parity Error does not behave correctly	No workarounds available

1. The Read Data Buffer can be overwritten causing the data provided to the initiator to be incorrect.

**Problem:** For this issue to occur, the following must take place. There must be two delayed transactions going to the same destination. The first transaction must fill the Read Data Buffer and the second transaction must be a single transaction.

After the first transaction executes and fills the Read Data Buffer, the PI7C7300E will still have GNT asserted on the destination bus. The second delayed transaction will overwrite the Read Data Buffer from the initiator side, causing incorrect data to be passed.

**Workaround:** There is no current workaround on the PI7C7300E revision of silicon.

**Status:** Fixed in the PI7C7300A revision of silicon.

2. Possible issue may result when there are upstream write cycles and the bridge is running at 66MHz primary and 33MHz secondary

**Problem:** When an upstream write cycle is initiated and the initiator is slow or adds wait states, the 7C7300A may issue a REQUEST for the bus before the cache is full. When the GRANT is received from the arbiter, the 7C7300A will not drive FRAME until either all of the data is in the cache or the cache is full. If FRAME is not driven within 16 clocks of receiving the GRANT, the arbiter may de-assert GRANT. 7C7300A will be left requesting the bus unsuccessfully, possibly hanging the system.

**Workaround:** Program register offset 74h bit 10 and bit 11 both to '0'. By default, both values are '1'. In this mode, the 7C7300A will de-assert REQUEST on every transaction. As a result, the 7C7300A will be able to drive FRAME within the 16 clocks in most cases. There is still a very slim possibility that FRAME will not be driven within the 16 clocks (extreme cases), but the de-assertion and re-assertion of REQUEST will cause the arbiter to issue another GRANT.

**Status:** Fix will be implemented should there be a future revision of silicon.

### 3. Data Parity Error does not behave correctly

**Problem:** The data parity error checking may not yield the proper status on both the primary and secondary buses. The bridge may not assert the P\_PERR#, S1\_PERR#, or S2\_PERR# signals if there is a data parity error on any of the buses.

**Workaround:** There is no workaround at this time. However, the user may check the status of bit [24] and bit [31] of the respective Status Registers to detect a parity error. If both bits [24] and [31] are set to 1, then there is a parity error on the bus. Data parity errors on the primary bus can be determined by checking bits [24] and [31] at offset 04h, and data parity errors on the secondary buses can be determined by checking bits [24] and [31] at offset 1Ch.

**Status:** Fix will be implemented should there be a future revision of silicon.