

PI7C21P100 PCI-X Bridge: Preliminary Errata

INTRODUCTION

This document is a summary of known potential issues and errata for the PI7C21P100, 2-port PCI-X to PCI-X Bridge. It describes what each erratum or issue is and provides the status of whether or not it will be corrected. As the device is used in more applications, this document is subject to change.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
03/24/04	1.0	First release of preliminary errata sheet
05/06/04	1.1	Added errata issues #3 - #6
05/07/04	1.2	Added errata issue #7

SILICON REVISIONS

REVISION	DESCRIPTION
1.0	PI7C21P100 initial release

SUMMARY OF ERRATA

ERRATA #	DESCRIPTION	STATUS
1	Secondary configuration access may yield incorrect register information	Workaround available.
2	Cascading of two PI7C21P100's running in a 133MHz to 133MHz to 33MHz configuration may produce a system hang	Issue closed. Test configuration led to the determination of issues 3 – 5.
3	Two DWORD Writes from PCI to PCI-X may produce incorrect data	No workarounds available
4	Input setup time (T _{SU}) may exceed PCI specification	No workarounds available
5	Clock to Output Delay (T _{VAL}) may exceed PCI specification	No workarounds available
6	Arbiter may not issue a GNT to a secondary device	Workaround available
7	Bridge may not initiate a transaction within 8 clocks after receiving a GNT	No workarounds available

1. Secondary configuration access may yield incorrect register information

Problem: When a configuration read transaction is generated from the secondary side of the bridge, the register information returned may be incorrect.

Workaround: To ensure the proper register information is received, P_CFG_BUSY must be HIGH during a P_RST# assertion. And, S_IDSEL must be held HIGH during the configuration cycle. If P_CFG_BUSY cannot be set HIGH during a primary reset, then another option is to set bit [2] offset 44h HIGH. S_IDSEL still needs to be HIGH during the configuration cycle. After bit[2] offset 44h is set HIGH, the configuration read access is enabled. To enable back the primary configuration access, bit[2] offset 44h needs to be reset back to LOW.

Status: Issue may be addressed in potential, future silicon revisions.

2. Cascading of two PI7C21P100's running in a 133MHz to 133MHz to 33MHz configuration may produce a system hang

Problem: A system hang could occur in a cascading configuration (a bridge behind a bridge) when the following conditions are met:

1. The first bridge must be running 133MHz on the primary and 133MHz on the secondary.
2. The second bridge must be running 133MHz on the primary and 33MHz on the secondary

Workaround: Non-issue.

Status: Issue closed. Test configuration lead to the determination of issues 3 – 5.

3. Two DWORD Writes from PCI to PCI-X may produce incorrect data

Problem: Incorrect data may be written if two DWORD writes are initiated from PCI to PCI-X with the frequency ratio equal to or greater than 4 to 1 (i.e. PCI at 33MHz writing to PCI-X at 133MHz).

Workaround: There are currently no workarounds for this issue. Designers should limit the frequency ratio between the primary and secondary buses to less than 4 to 1.

Status: Issue may be addressed in potential, future silicon revisions.

4. Input setup time (T_{SU}) may exceed PCI-X specification

Problem: Under worst case conditions (defined as 90°C, VDD=2.3V, VDD2=3.0V), the input setup time may violate PCI-X specifications by up to 0.5ns. The PCI-X specification calls out a minimum value of 1.2ns for T_{SU} . The worst case for the AD and control signals is 1.7ns.

Workaround: There are currently no workarounds for this issue.

Status: Issue may be addressed in potential, future silicon revisions.

5. Clock to Output Delay (T_{VAL}) may exceed PCI-X specification

Problem: Under worst case conditions (defined as 90°C, VDD=2.3V, VDD2=3.0V), the clock to output delay time may violate PCI-X specifications by up to 0.5ns. The PCI-X specification calls out a maximum value of 3.8ns for T_{VAL} . The worst case for the AD and control signals is 4.3ns.

Workaround: There are currently no workarounds for this issue.

Status: Issue may be addressed in potential, future silicon revisions.

6. Arbiter may not issue a GNT to a secondary device

Problem: If there are at least two masters on the secondary bus of the bridge, and the default conditions (bridge is set as HIGH priority) are utilized, one of the devices may not be issued a GNT by the internal arbiter in a timely manner.

Workaround: There are 2 workarounds available for this issue. Implementing one of the workarounds will alleviate the issue.

- (1) Set all devices to HIGH priority in the Arbiter Priority Register (FFh to offset 58h)
- (2) Set all devices to LOW priority in the Arbiter Priority Register (00h to offset 58h)

Status: Issue may be addressed in potential, future silicon revisions.

7. Bridge may not initiate a transaction within 8 clocks after receiving a GNT

Problem: After receiving a GNT from the arbiter, the bridge may not initiate a transaction within the specified 8 clocks.

Workaround: There are no workarounds for this issue. However, if the arbiter does not treat this condition as a broken master, this condition becomes a non-issue.

Status: Issue may be addressed in potential, future silicon revisions.