

# 3.3V PECL Low Jitter XO

**SD**



5.0 x 3.2mm Ceramic SMD

### Product Features

- 50 to 220 MHz Frequency Range
- <1 ps RMS jitter with advanced non-PLL, patented design (U.S. Patent #7002423)
- Thicker crystal for improved reliability
- RoHS compliant

### Product Description

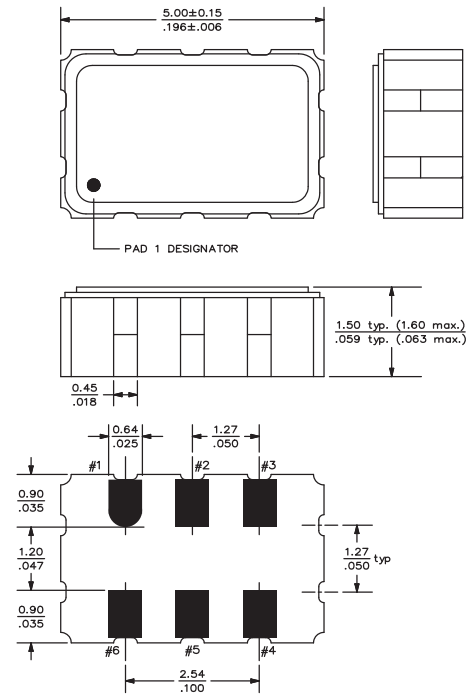
The SD Series 3.3V crystal clock oscillator achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a patented oscillator design, is compatible with LVPECL logic levels. The device is available on tape and reel, is contained in a 5.0 x 3.2mm surface-mount ceramic package.

### Applications

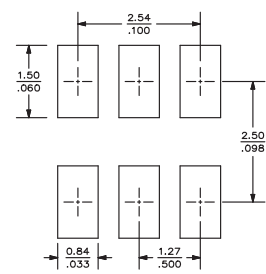
The SD Series is ideal for high-speed applications requiring low jitter, including:

- 1/10 Gigabit Ethernet
- 2/4/10G Fibre Channel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH linecards
- Passive Optical network (PON) Systems
- HDD, Storage
- SFP Module

### Package:



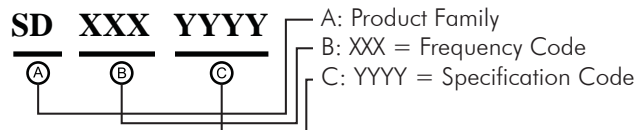
### Recommended Land Pattern:



### Pin Functions:

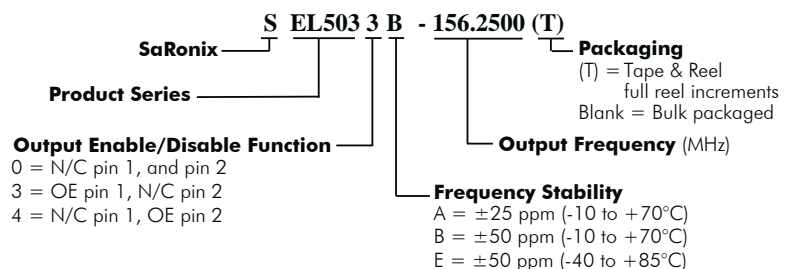
Pin	Function
1	OE or NC
2	OE or NC
3	V <sub>EE</sub>
4	Q Output
5	$\bar{Q}$ Output
6	V <sub>CC</sub>

### Part Ordering Information:



Following the above format, Saronix-eCera part numbers will be assigned upon confirmation of exact customer requirements.

### Legacy Ordering Information - For Reference Only:



### Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output Frequency	50		220	MHz	As specified
Supply Voltage	2.97	3.3	3.63	V	
Supply Current, Output Enabled		60	70	mA	
Supply Current, Output Disabled			25	μA	
Frequency Stability			±20 to ±50	ppm	See Note 1 below
Operating Temperature Range	-40		+85	°C	As specified
Output Logic 0, V <sub>OL</sub>			V <sub>CC</sub> – 1.620	V	0 to +85°C
			V <sub>CC</sub> – 1.555	V	-40 to 0°C
Output Logic 1, V <sub>OH</sub>	V <sub>CC</sub> – 1.025			V	0 to +85°C
	V <sub>CC</sub> – 1.085			V	-40 to 0°C
Output Load	50Ω to V <sub>CC</sub> – 2V				output requires termination
Duty Cycle	45		55	%	measured 50% of waveform
Rise and Fall Time		500	850	ps	measured 20/80% of waveform
Jitter, Phase			1	ps RMS (1-σ)	12kHz to 20MHz frequency band
Jitter, Total			40	ps pk-pk	1000 random periods

#### Notes:

- Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (5 year at 40°C average effective ambient temperature), shock and vibration.
- For specifications other than those listed, please contact sales.

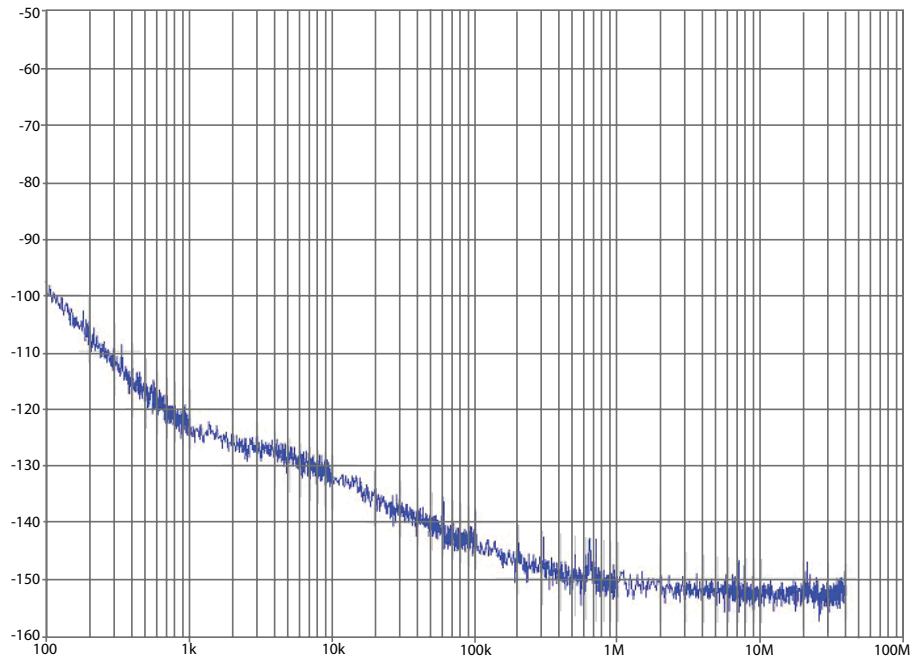
### Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin OE), Output Enable	2.2			V	or open
Input Voltage (pin OE), Output Disable (low power standby)			0.8	V	Outputs disabled to Hi-Z
Internal Pullup Resistance	50			kΩ	
Output Disable Delay			200	ns	
Output Enable Delay			10	ms	

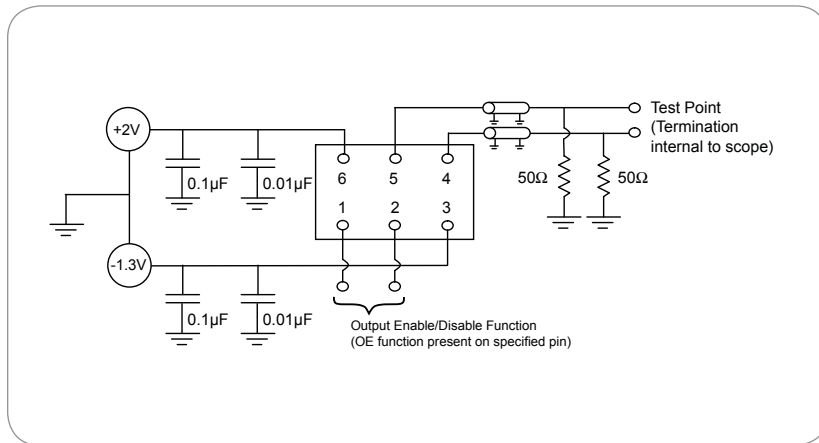
### Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage Temperature	-55		+125	°C	

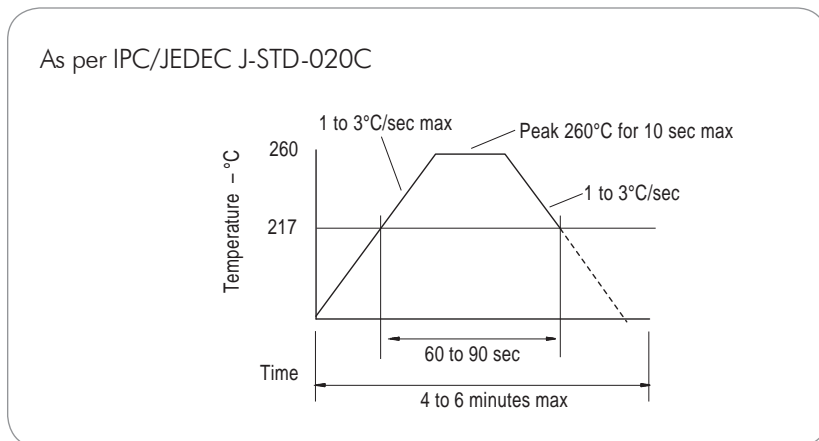
### Typical Phase Noise



### Test Circuit



### Reflow Soldering Profile



### Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ( $R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)