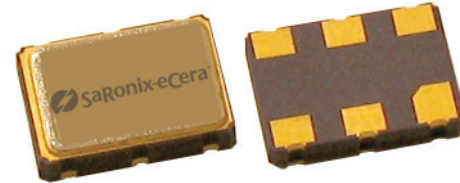
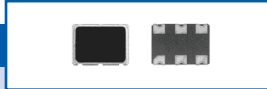


3.3V HCSL PCI-Express Gen2 Low Jitter, XO

SH



Actual Size = 7 x 5mm



Product Features

- Thicker crystal than conventional overtone for improved reliability
- Less than 3.1 ps RMS jitter (measured per PCI-SIG for PCIeG2 reference clock) with advanced non-PLL, patented XP Technology (U.S. Patent #7002423)
- Tight stability over a broad range of operating conditions
- HCSL differential output
- Pin-compatible with standard 7x5mm packages
- Designed for standard reflow & washing techniques
- IBIS models available
- RoHS compliant **

**per #7, Annex of Directive 2002/OS/EC

Product Description

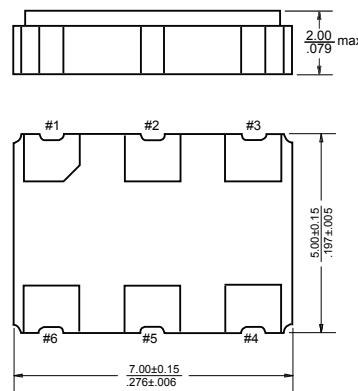
The SH Series includes a 3.3V HCSL PCIeG2 crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a patented oscillator design, provides HCSL differential levels. The device, available on tape and reel, is contained in a 7x5mm surface-mount ceramic package.

Applications

The SH Series is an ideal reference clock for high-speed applications requiring low jitter, 100 MHz HCSL Reference Clock, including:

- Server
- SAS
- SATA
- Graphics Card
- Network Switch/Router
- PTelecom Switch
- Media Box

Packaging Outline



Pin Functions

Pin	Function
1	OE
2	NC
3	V _{EE}
4	Q Output
5	\bar{Q} Output
6	V _{CC}

Part Number

SH **A00** **0001** A = Product Family
 Ⓐ Ⓑ Ⓒ B = Frequency Code
 C = Specification Code

Electrical Performance (Over -40 to 85°C)

Parameter	Min.	Typ.	Max.	Units	Notes
Output frequency		100		MHz	As specified
Supply voltage	2.97	3.3	3.63	V	
Supply current		50	60	mA	100 MHz (enabled)
Supply current			25	mA	100 MHz (disabled)
Frequency stability			±50	ppM	See Note 1 below
Operating temperature	-40		+85	°C	As specified
Output logic 0, V _{OL}	-0.15		0.15	V	
Output logic 1, V _{OH}		0.7	0.85	V	
Output load	See Test Diagram				output requires termination
Duty cycle	45		55	%	measured 50% of waveform
Rise and fall time			700	ps	measured from V _{OL} =0.175V to V _{OH} =0.525V
Jitter, phase			3.1	ps RMS	As defined by PCI-SIG for PCIeG2 reference clock

Notes:

- As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (5 years at 40°C average effective ambient temperature), shock and vibration
- Note: For specifications other than those listed, please contact sales.

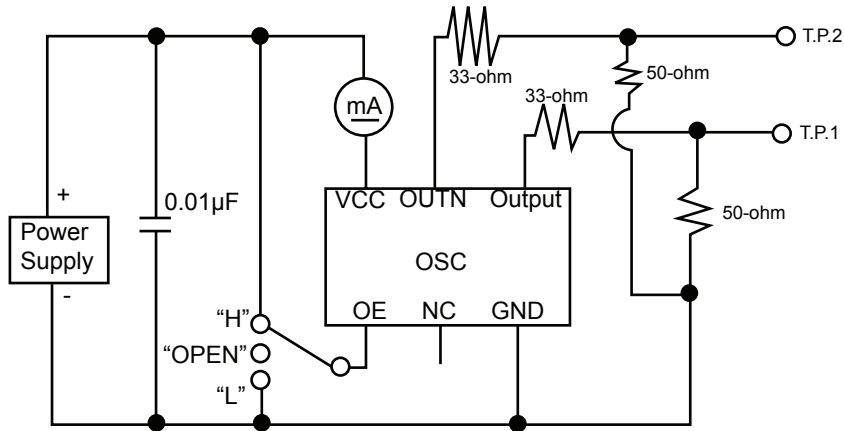
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (OE pin), Output Enable	2.2			V	or open
Input voltage (OE pin), Output Disable			0.8	V	Outputs disabled to Hi-Z
Internal Pull-up Resistance	50			kΩ	
Output disable delay			200	ns	
Output enable delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Diagram



Reset Function:

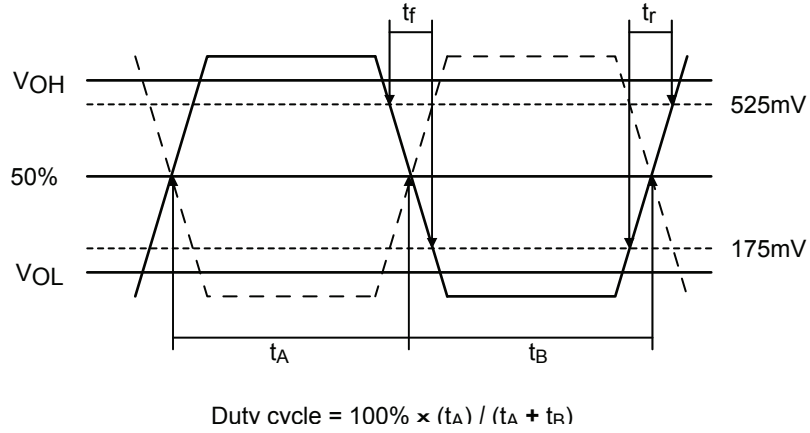
Logic 0 On Pad 1 - Disable Output to High Impedance
Logic 1 or Open On Pad 1 - Oscillator Output Enabled

Reliability Test Ratings

This product is rated to meet the following test conditions:

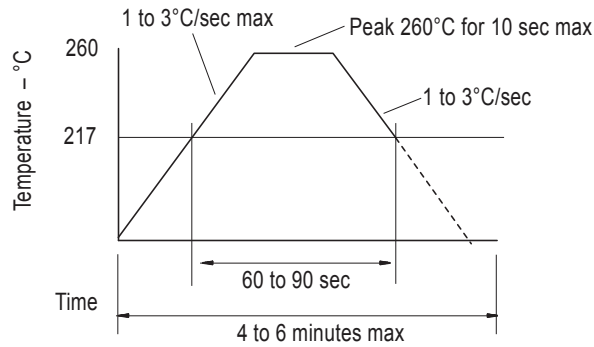
Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

Output Waveform



Reflow Soldering Profile

As per IPC/JEDEC J-STD-020C



Mechanical Drawing:

