

Features

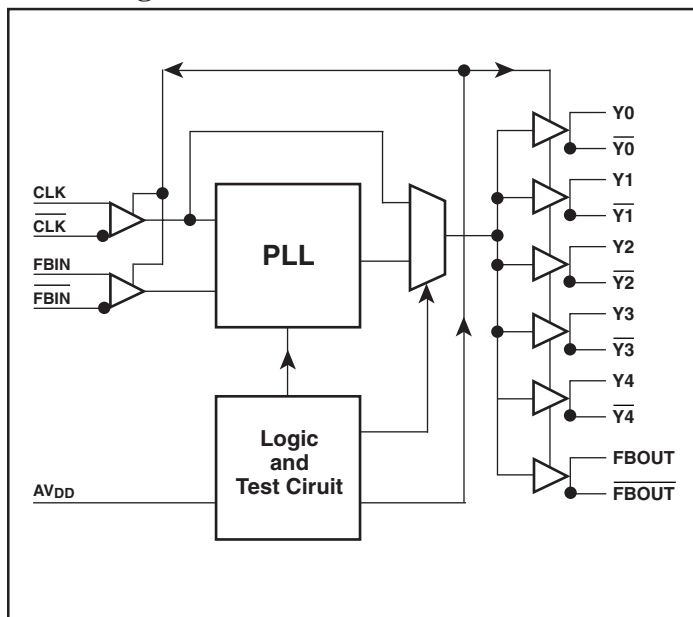
- PLL clock distribution optimized for SSTL_2
- Distributes one differential clock input pair to five differential clock output pairs.
- Inputs (CLK, $\overline{\text{CLK}}$) and (FBIN, $\overline{\text{FBIN}}$): SSTL_2
- Outputs (Yx, $\overline{\text{Yx}}$), (FBOUT, $\overline{\text{FBOUT}}$): SSTL_2
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the input clocks.
- Operates at $\text{AV}_{\text{DD}} = 2.5\text{V}$ for core circuit and internal PLL, and $\text{V}_{\text{DD}} = 2.5\text{V}$ for differential output drivers
- Packaging (Pb-free & Green available):
-24-pin TSSOP (L24)

Description

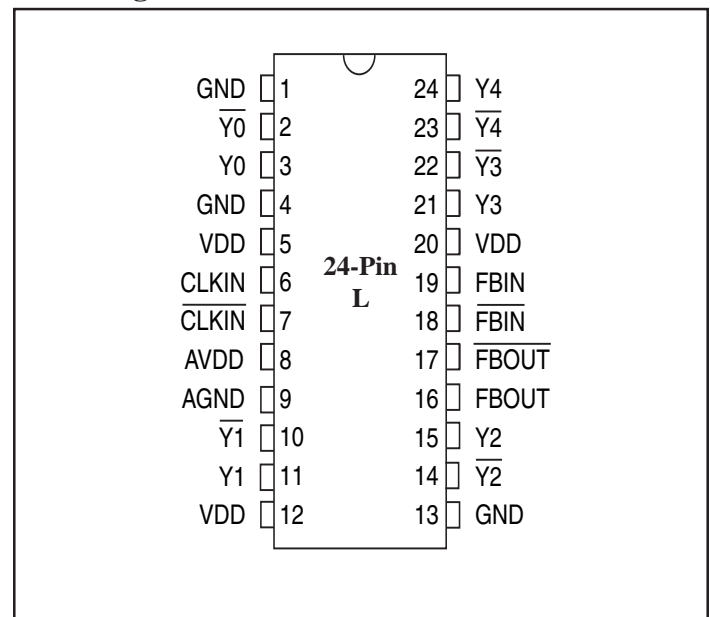
The PI6CV847 PLL Clock Buffer is designed for 2.5 V_{DDQ} and 2.5V AV_{DD} operation and differential data input and output levels. The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to five differential pairs of clock outputs (Y[0:4], $\overline{\text{Y}}[0:4]$) and one differential pair feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the Analog Power input (AV_{DD}). When the AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

The PI6CV847 is able to track Spread Spectrum Clocking to reduce EMI.

Block Diagram



Pin Configuration



Pinout Table

Pin Name	Pin No.	I/O Type	Description
CLK CLK	6 7	I	Reference Clock, and Complement Reference Clock input.
Y[0:4]	3,11,15,21,24	O	Clock outputs.
$\overline{Y[0:4]}$	2,10,14,22,23		Complement Clock outputs.
FBOUT FBOUT	16 17		Feedback output, and Complement Feedback Output
FBIN FBIN	19 18	I	Feedback input, and Complement Feedback input
V _{DD}	5,12,20	Power	Power Supply for I/O pins.
AV _{DD}	8		Analog/core power supply. AV _{DD} can be used to bypass the PLL for testing purposes. When AV _{DD} is strapped to ground, PLL is bypassed & CLK is buffered directly to the device outputs.
AGND	9	Ground	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	1,14,13		Ground for I/O pins.

Function Table

Inputs			Outputs				PLL State
AV _{DD}	CLK	\overline{CLK}	Y[0:4]	$\overline{Y[0:4]}$	FBOUT	\overline{FBOUT}	
GND	L	H	L	H	L	H	Bypassed/Off
GND	H	L	H	L	H	L	Bypassed/Off
2.5V(nom)	L	H	L	H	L	H	On
2.5V(nom)	H	L	H	L	H	L	On

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{DD}	I/O supply voltage range and analog/core supply voltage range	- 0.5	4.6	V
V_I	Input voltage range	- 0.5	$V_{DDQ}+0.5$	
V_O	Output voltage range	- 0.5		
Tstg	Storage temperature	- 65	150	°C
Ta	Ambient Operating Temperature	0	85	

Note: Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Timing Requirements ($T_a=0-85^{\circ}\text{C}$)

Symbol	Description	$AV_{DD}, V_{DDQ} = 2.5V \pm 0.2V$		Units
		Min.	Max.	
f_{CK}	Operating clock frequency , 25 °C	95	200	MHz
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	PLL stabilization time after powerup		15	μs

DC Specifications

Recommended Operating Conditions (please refer to note 1)

Symbol	Parameter	Min.	Nom.	Max.	Units
V_{DD}	Analog core supply voltage	2.3	2.5	2.7	V
V_{DD}	Output supply voltage	2.3	2.5	2.7	
V_{IX}	Input differential-pair crossing voltage (note 4)	$(V_{DD}/2) - 0.2$		$(V_{DD}/2) + 0.2$	
V_{OX}	Output differential-pair crossing voltage (note 4)	$(V_{DD}/2) - 0.15$		$(V_{DD}/2) + 0.15$	
V_{IN}	DC Input voltage level (note 2)	-0.3		$V_{DD} + 0.3$	
V_{ID} (note 3)	DC Input differential voltage	0.36		$V_{DD} + 0.6$	
	AC Input differential voltage	0.7		$V_{DD} + 0.6$	
V_{OD}	Output differential voltage	0.7		$V_{DD} + 0.6$	
T_A	Operating free air temperature	0		85	°C

Notes:

1. Unused inputs must be held high or low, do not leave them floating.
2. DC input voltage specifies the DC component of the differential inputs.
3. Vid specifies the differential amplitude ($V_{true} - V_{complement}$) needed for switching.
4. Vox is expected to track Vdd variations. It is the expected crossing voltage required by the input.

Electrical Characteristics ($T_a = 0 - 85^{\circ}C$, $V_{dd} = 2.5V \pm 0.2V$)

Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{IK}	All inputs	$I_I = -18mA$			-1.2	V
I_I	CLK, FBIN	$V_I = V_{DDQ}$ or GND			± 10	μA
$I_{DD2.5}$	Operating Supply Current	$C_L = 0pF, 200MHz$			200	mA
I_{DDPD}		$C_L = 0pF$			100	μA
I_{OZ}	High Impedance Output Current	$V_{DD} = 2.7V, V_{OUT} = V_{DD}$ or GND			± 10	mA
V_{OL}	Low Output Voltage	$I_{OL} = 1mA$			0.1	V
		$I_{OL} = 12mA$			0.6	
V_{OH}	High Output Voltage	$I_{OH} = -1mA$	$V_{DD} - 0.1$			V
		$I_{OH} = -12mA$	1.7			
$C_I^{(1)}$	CLK and \overline{CLK}	$V_I = V_{DD}$ or GND	2.5		3.5	pF
	FBIN and \overline{FBIN}					

Notes:

1. Guaranteed by design @ 233MHz, not production tested

AC Specifications (see Note 3)

Switching characteristics over recommended operating free-air temperature range, $f_{CLK} > 100$ MHz (unless otherwise noted).
(See Figure 1 and 2)

Parameter	Description	Diagram	AVCC, VDDQ = 2.5V ±0.2V			Units
			Min.	Nom.	Max.	
t(O)	Phase Offset ⁽⁴⁾	Figure 4	-50	0	50	ps
tjit(cc)	Cycle-to-cycle jitter ⁽⁴⁾ (100 MHz to 200 MHz)	Figure 3			60	
tjit(per)	Period jitter (100 MHz to 200MHz)	Figure 6	-30		30	
tjit(hper)	Half-period jitter (100 MHz to 200MHz)	Figure 7	-75		30	
tsl(i)	Input clock slew rate	Figure 8	1		4	V/ns
tsl(o)	Output clock slew rate	Figure 8	1		2.5	
tsk(o)	Output clock skew	Figure 5			60	ps
tplh ⁽¹⁾	Low to high propagation delay			3.5		ns
tphl ⁽¹⁾	High to low propagation delay			3.5		ns

Notes:

1. Transition of non-inverting output in PLL bypass mode
2. Pulse skew is constant over the application frequency range, but duty cycle error increases with frequency.
[duty cycle = t_{wH}/t_c (high pulse width / cycle period); t_c decreases as frequency increases]
3. Switching characteristics is guaranteed over application frequency range
4. Static phase offset shifted by design
5. Spread spectrum off

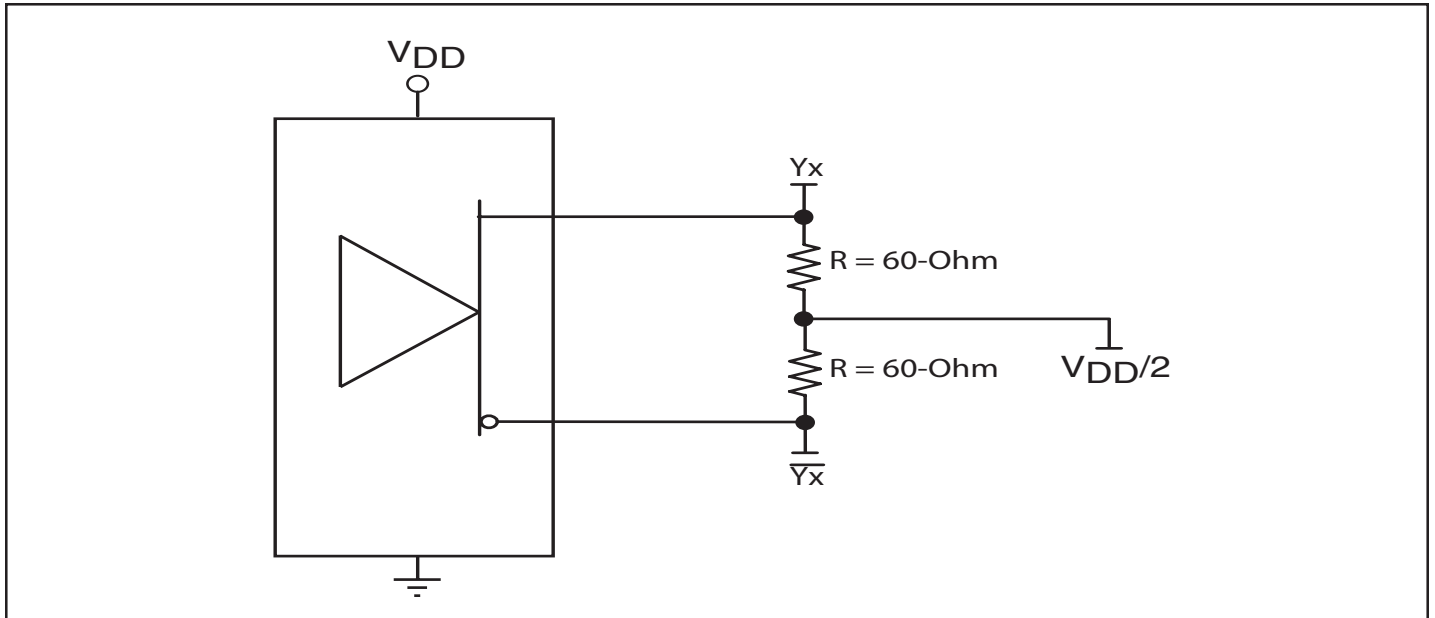


Figure 1. IBIS Model Output Load

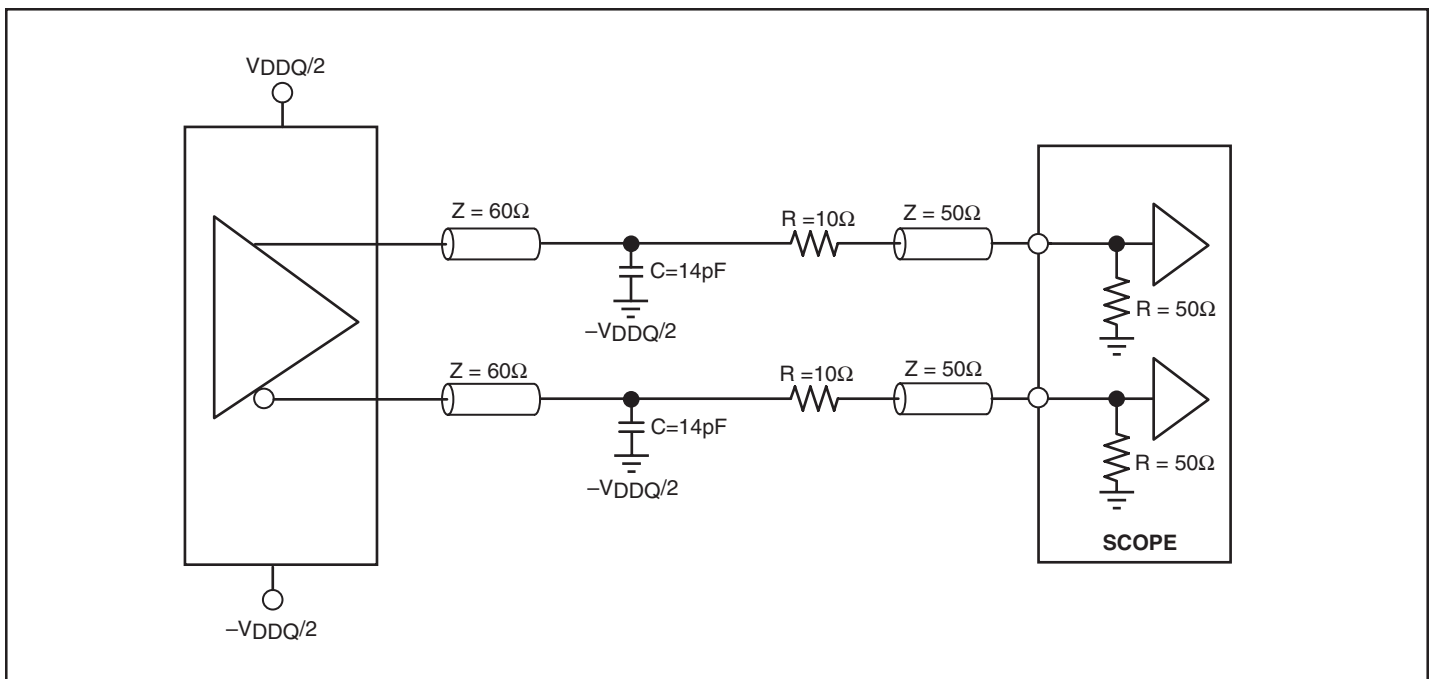


Figure 2. Output Load Test Circuit

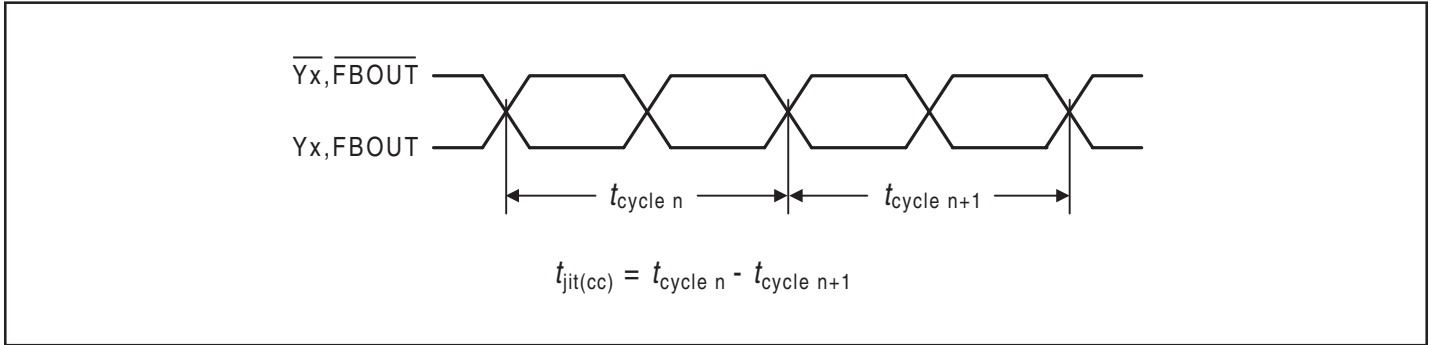


Figure 3. Cycle-to-Cycle Jitter

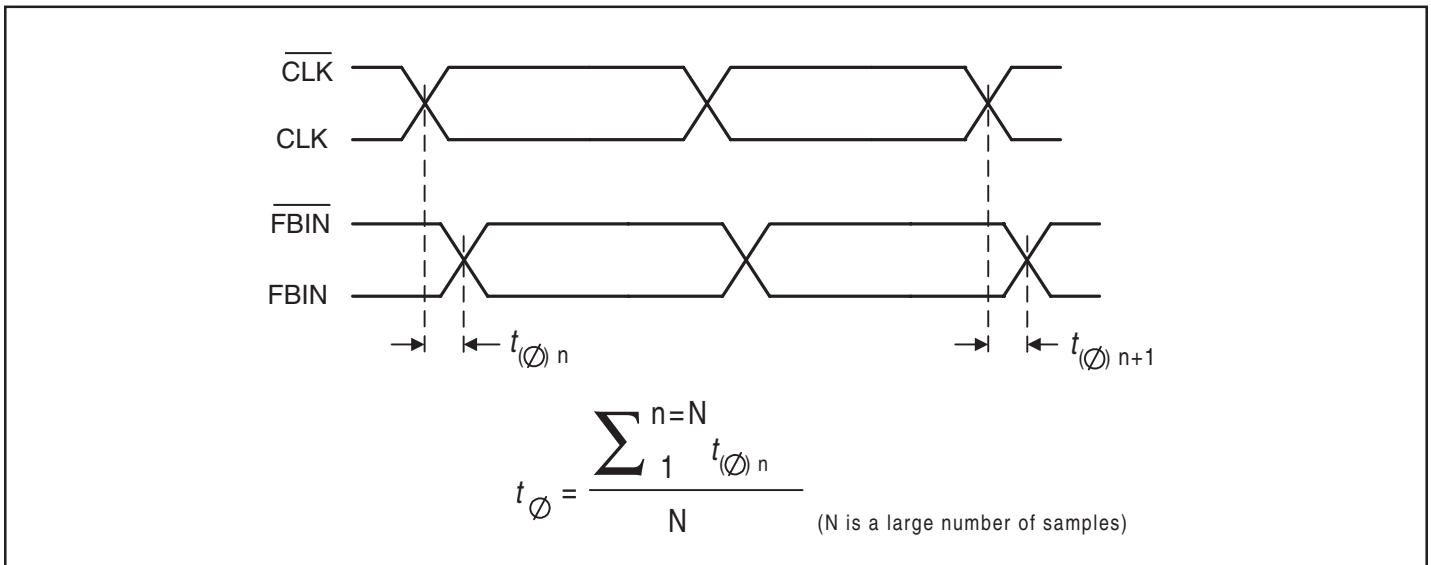


Figure 4. Static Phase Offset

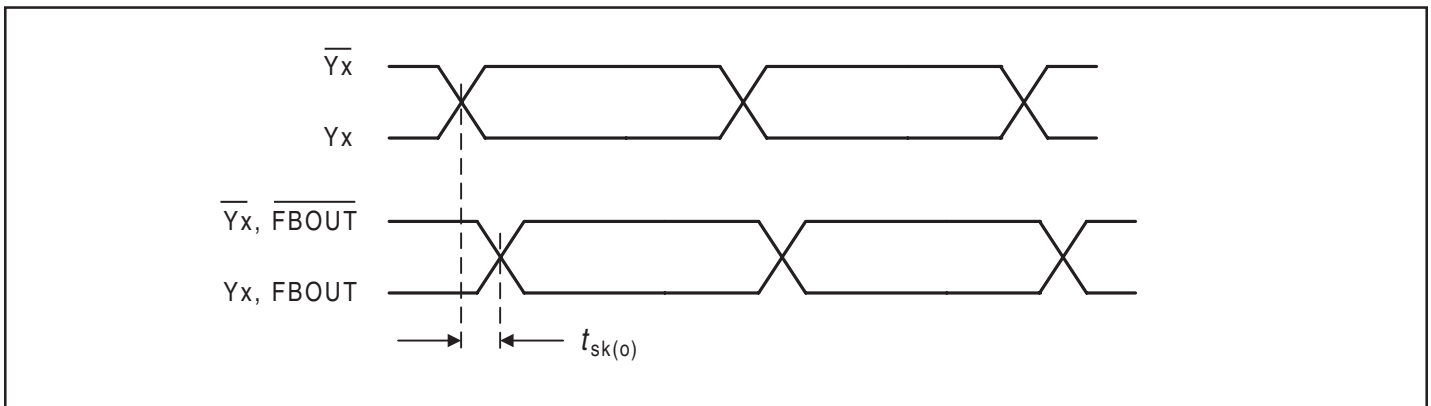


Figure 5. Output Skew

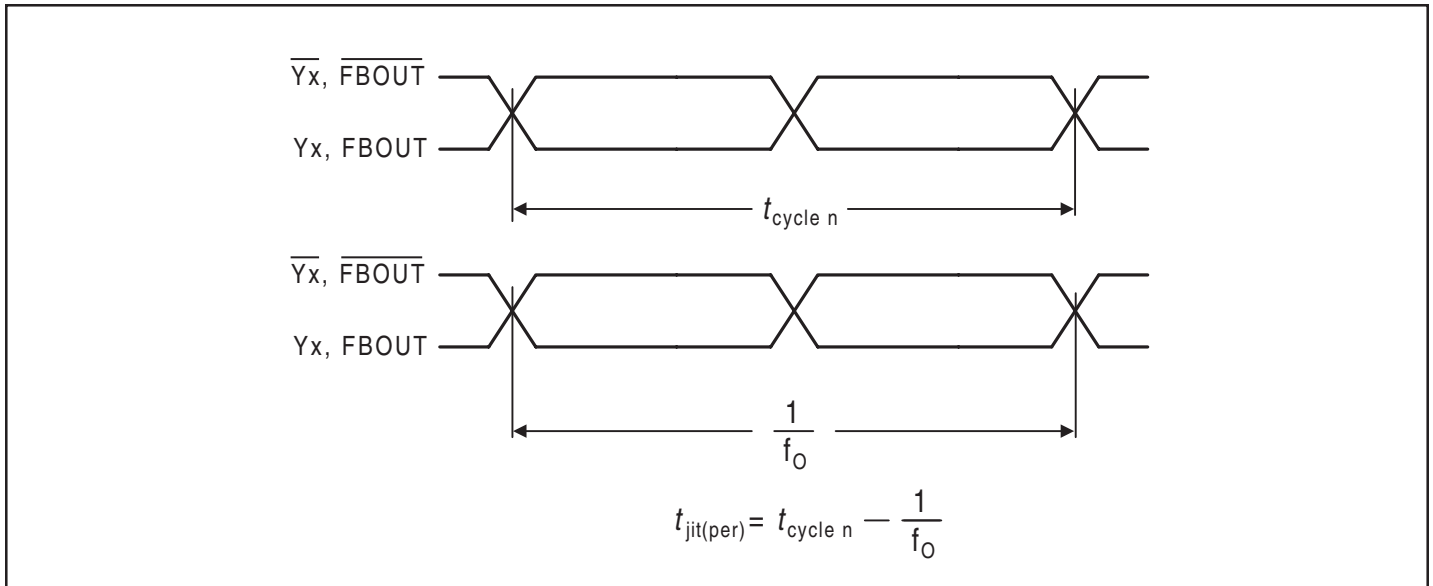


Figure 6. Period Jitter

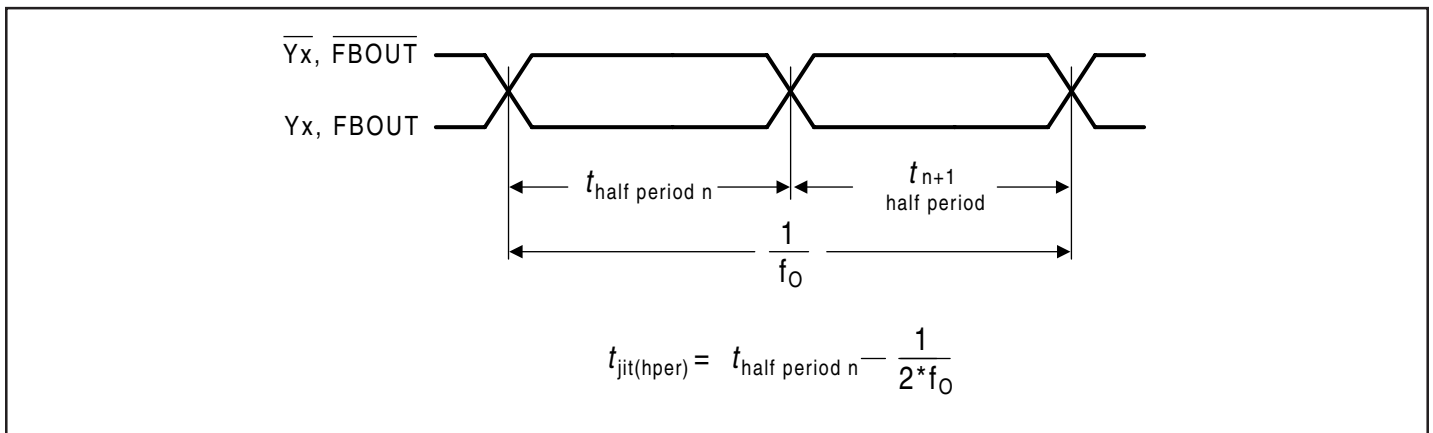


Figure 7. Half-Period Jitter

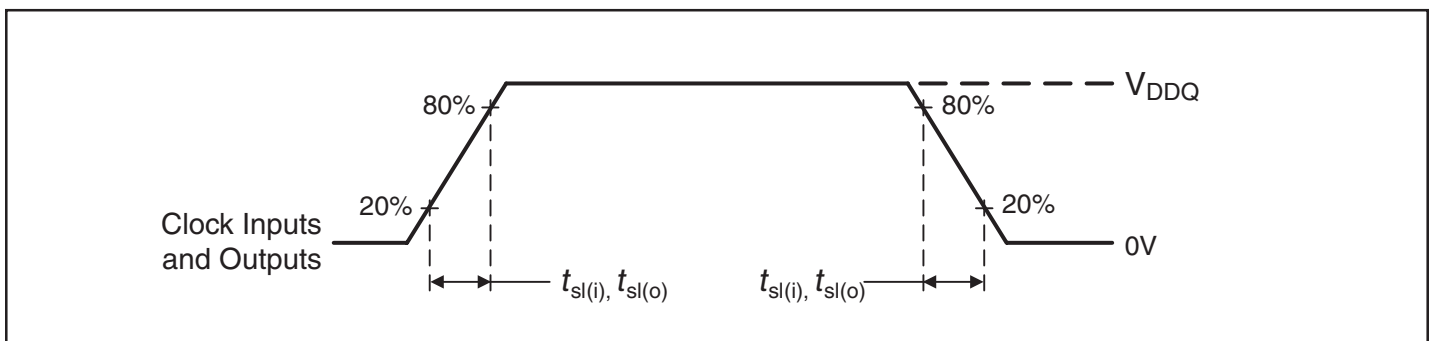
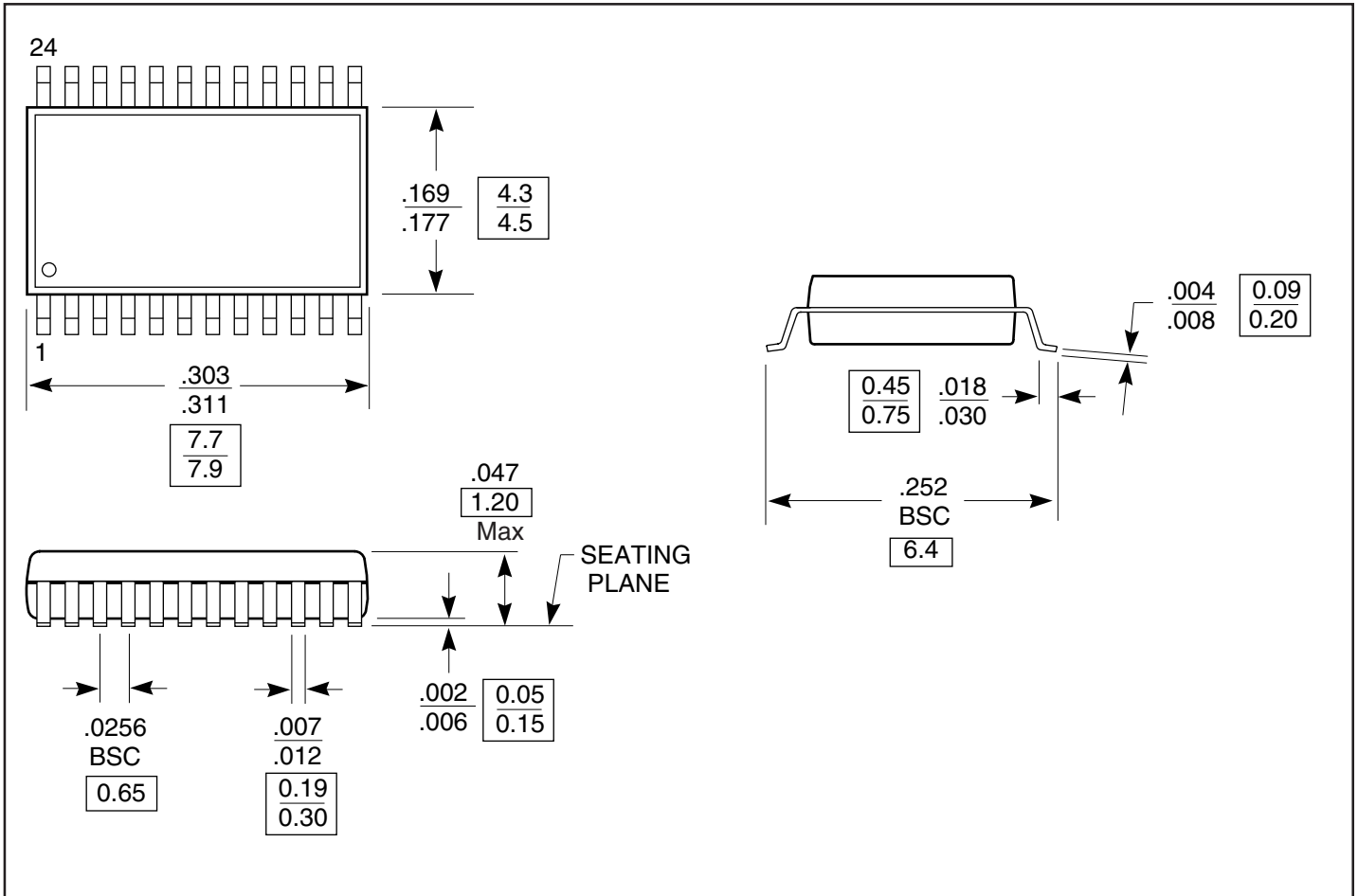


Figure 8. Input and Output Slew Rates

Packaging Mechanical: 24-Pin TSSOP (L24)



Ordering Information

Ordering Code	Package Code	Package Type
PI6CV847L	L	24-pin 173-mil wide TSSOP
PI6CV847LE	L	Pb-free & Green, 24-pin 173-mil wide TSSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/