

## Features

- PLL clock distribution for DDR2 DIMM applications.
- Distributes one differential clock input pair to eleven differential clock output pairs.
- Differential Inputs (CLK,  $\overline{\text{CLK}}$ ) and (FBIN,  $\overline{\text{FBIN}}$ )
- Input OE/OS: LVC MOS
- Differential Outputs (Y[0:9],  $\overline{\text{Y}}[0:9]$ ) and (FBOU $\overline{\text{T}}$ ,  $\overline{\text{FBOU}}\overline{\text{T}}$ )
- External feedback pins (FBIN,  $\overline{\text{FBIN}}$ ) are used to synchronize the outputs to the clock input.
- Operates at  $\text{AV}_{\text{DD}} = 1.8\text{V}$  for core circuit and internal PLL, and  $\text{V}_{\text{DDQ}} = 1.8\text{V}$  for differential output drivers
- Available Packages (Pb-free & Green):
  - 52-ball VFBGA (NF)
- PI6CUA878 is for DDR2-800/667/533/400 applications

## Pin Configuration

	1	2	3	4	5	6
A	Y1	Y0	$\overline{\text{Y}}0$	$\overline{\text{Y}}5$	Y5	Y6
B	$\overline{\text{Y}}1$	GND	GND	GND	GND	$\overline{\text{Y}}6$
C	$\overline{\text{Y}}2$	GND	NB	NB	GND	$\overline{\text{Y}}7$
D	Y2	VDDQ	VDDQ	VDDQ	OS	Y7
E	CK	VDDQ	NB	NB	VDDQ	FBIN
F	$\overline{\text{CK}}$	VDDQ	NB	NB	OE	$\overline{\text{FBIN}}$
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	$\overline{\text{FBOU}}\overline{\text{T}}$
H	AVDD	GND	NB	NB	GND	FBOU $\overline{\text{T}}$
J	Y3	GND	GND	GND	GND	Y8
k	$\overline{\text{Y}}3$	$\overline{\text{Y}}4$	Y4	Y9	$\overline{\text{Y}}9$	$\overline{\text{Y}}8$

## Description

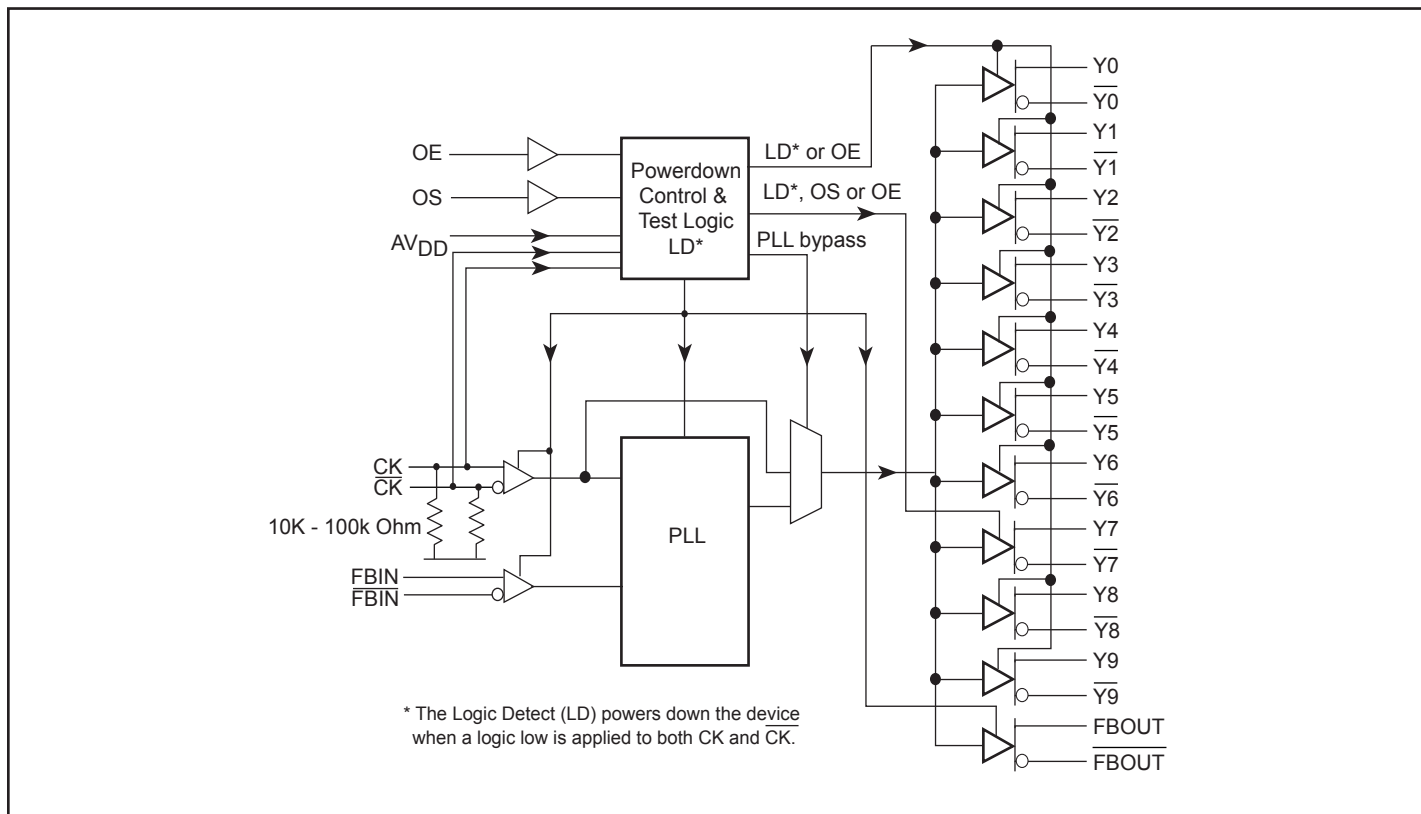
PI6CUA878 PLL clock driver is developed for Registered DDR2 DIMM applications with 1.8V operation and differential data input and output levels.

The device is a zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to eleven differential pairs of clock outputs which includes feedback clock (Y[0:9],  $\overline{\text{Y}}[0:9]$ ; FBOU $\overline{\text{T}}$ ,  $\overline{\text{FBOU}}\overline{\text{T}}$ ).

The clock outputs are controlled by CLK/ $\overline{\text{CLK}}$ , FBOU $\overline{\text{T}}$ ,  $\overline{\text{FBOU}}\overline{\text{T}}$ , the LVC MOS inputs (OE, OS) and the Analog Power input ( $\text{AV}_{\text{DD}}$ ). When OE is LOW, all the outputs except for FBOU $\overline{\text{T}}$ ,  $\overline{\text{FBOU}}\overline{\text{T}}$ , are disabled while the internal PLL continues to maintain its locked-in frequency. OS is a program pin that must be tied to GND or  $\text{V}_{\text{DD}}$ . When OS is high, OE will function as described above. When OS is low, OE has no effect on Y7/ $\overline{\text{Y}}7$ , they are free running. When  $\text{AV}_{\text{DD}}$  is grounded, the PLL is turned off and bypassed for test purposes.

When CLK/ $\overline{\text{CLK}}$  are logic LOW, the device will enter a low power mode. An input logic detection circuit will detect the logic low level and perform a low power state where all Y[0:9],  $\overline{\text{Y}}[0:9]$ ; FBOU $\overline{\text{T}}$ ,  $\overline{\text{FBOU}}\overline{\text{T}}$ , and PLL are OFF.

The PI6CUA878 is a high performance, low skew, and low jitter PLL clock driver, and is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

**Block Diagram**


**Pinout Table**

Pin Name	Characteristics	Description
AGND	Ground	Analog ground
AV <sub>DD</sub>	1.8V nominal	Analog power
CK	Differential Input	Clock input with a (10k - 100kΩ) pulldown resistor
$\overline{\text{CK}}$	Differential Input	Complementary clock input with a (10k - 100kΩ) pulldown resistor
$\overline{\text{FBIN}}$	Differential Input	Complementary feedback clock input
FBIN	Differential Input	Feedback clock input
$\overline{\text{FBOU}}$	Differential Output	Complementary Feedback clock output
FBOU	Differential Output	Feedback clock output
OE	LVC MOS input	Output enable (async.)
OS	LVC MOS input	Output select (tied to GND or V <sub>DDQ</sub> )
GND	Ground	Ground
V <sub>DDQ</sub>	1.8V nominal	Logic and Output power
Y[0:9]	Differential Outputs	Clock outputs
$\overline{\text{Y}}[0:9]$	Differential Outputs	Complementary clock outputs
NB		No Ball

**Function Table**

Inputs					Outputs				PLL State
AV <sub>DD</sub>	OE	OS	CK	$\overline{\text{CK}}$	Y	$\overline{\text{Y}}$	FBOU	$\overline{\text{FBOU}}$	
GND	H	X	L	H	L	H	L	H	Bypass/Off
GND	H	X	H	L	H	L	H	L	Bypass/Off
GND	L	H	L	H	L(Z) <sup>(1)</sup>	L(Z) <sup>(1)</sup>	L	H	Bypass/Off
GND	L	L	H	L	L(Z) <sup>(1)</sup> , Y7 active	L(Z) <sup>(1)</sup> , Y7 active	H	L	Bypass/Off
1.8V (nom)	L	H	L	H	L(Z) <sup>(1)</sup>	L(Z) <sup>(1)</sup>	L	H	On
1.8V (nom)	L	L	H	L	L(Z) <sup>(1)</sup> , Y7 active	L(Z) <sup>(1)</sup> , Y7 active	H	L	On
1.8V (nom)	H	X	L	H	L	H	L	H	On
1.8V (nom)	H	X	H	L	H	L	H	L	On
1.8V (nom)	X	X	L	L	L(Z) <sup>(1)</sup>	L(Z) <sup>(1)</sup>	L(Z) <sup>(1)</sup>	L(Z) <sup>(1)</sup>	Off
1.8V (nom)	X	X	H	H	Reserved				

**Notes:**

1. L(Z) means the outputs are disabled to a low state meeting the I<sub>ODL</sub> limit on DC Specification

**Absolute Maximum Ratings** (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V <sub>DDQ</sub> , AV <sub>DD</sub>	I/O supply voltage range and analog /core supply voltage range	-0.5	2.5	V
V <sub>I</sub>	Input voltage range <sup>(2, 3)</sup>	-0.5	V <sub>DDQ</sub> +0.5	
V <sub>O</sub>	Output voltage range <sup>(2, 3)</sup>	-0.5	V <sub>DDQ</sub> +0.5	
I <sub>IK</sub>	Input clamp current	-50	50	mA
I <sub>OK</sub>	Output clamp current	-50	50	
I <sub>O</sub>	Continuous output current	-50	50	
I <sub>O(PWR)</sub>	Continuous current through each V <sub>DDQ</sub> or GND	-100	100	
T <sub>STG</sub>	Storage temperature	-65	150	°C

**Notes:**

1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

**DC Specifications Recommended Operating Conditions**

Symbol	Parameter		Min.	Typ.	Max.	Units
V <sub>DDQ</sub>	Output supply Voltage		1.7	1.8	1.9	V
AV <sub>DD</sub>	Supply voltage <sup>(4)</sup>			V <sub>DDQ</sub>		
V <sub>IL</sub>	Low-level input voltage <sup>(5)</sup>	OE, OS, CK, $\overline{\text{CK}}$			0.35 x V <sub>DDQ</sub>	
V <sub>IH</sub>	High-level input voltage <sup>(5)</sup>	OE, OS, CK, $\overline{\text{CK}}$	0.65 x V <sub>DDQ</sub>			
I <sub>OH</sub>	High-level output current, see Fig 2		-		-9	mA
I <sub>OL</sub>	Low-level output current, see Fig. 2		-		9	
V <sub>IX</sub>	Input differential-pair crossing voltage		(V <sub>DDQ</sub> /2) -0.15		(V <sub>DDQ</sub> /2) +0.15	
V <sub>IN</sub>	Input voltage level		-0.3		V <sub>DDQ</sub> +0.3	V
V <sub>ID</sub>	Input differential voltage, See Fig 9 <sup>(5)</sup>	DC	0.3		V <sub>DDQ</sub> +0.4	
		AC	0.6		V <sub>DDQ</sub> +0.4	
T <sub>A</sub>	Operating free air temperature		0		70	°C

**Notes:**

4. The PLL is turned off and bypassed for test purposes when AV<sub>DD</sub> is grounded. During this test mode, V<sub>DDQ</sub> remains within the recommended operating conditions and no timing parameters are guaranteed.
5. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on  $\overline{\text{CK}}$ , see Figure 9 for definition. The CK and  $\overline{\text{CK}}$ , V<sub>IH</sub> and V<sub>IL</sub> limits are used to define the DC low and high levels for the logic detect state.

**Timing Requirements** (Over recommended operating free-air temperature)

Symbol	Description	AVDD, VDDQ = 1.8V ±0.1V		Units
		Min.	Max.	
f <sub>CK</sub>	Operation clock frequency <sup>(7, 9)</sup>	125	410	MHz
	Application clock frequency <sup>(7, 9)</sup>	160	410	
t <sub>L</sub>	Stabilization time <sup>(10)</sup>   f <sub>CK</sub> = 160 - 410 MHz		6	μs
t <sub>DC</sub>	Input clock duty cycle	40	60	%
t <sub>OFF</sub>	Device power down <sup>(10)</sup>		8	ns

**Notes:**

- The PLL is able to handle spread spectrum induced skew.
- Operating clock frequency indicates a range over which the PLL is able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed debug).
- Application clock frequency indicates a range over which the PLL must meet all timing parameters.
- Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and CK go to a logic low state, enter the power-down mode and later return to active operation. CK and CK maybe left floating after they have been driven low for one complete clock cycle.

**DC Specifications**

Parameter	Description	Test Condition	AVDD, VDDQ	Min.	Typ.	Max.	Units	
V <sub>IK</sub>	All Inputs	I <sub>I</sub> = -18mA	1.7V			1.2	V	
V <sub>OH</sub>	HIGH output voltage	I <sub>OH</sub> = -100μA	1.7 to 1.9V	V <sub>DDQ</sub> -0.2				
		I <sub>OH</sub> = -9mA	1.7	1.1				
I <sub>ODL</sub>	Output disabled low current	OE = L, V <sub>ODL</sub> = 100mV	1.7V	100			μA	
V <sub>OD</sub>	Output differential voltage, the magnitude of the difference between the true and complimentary outputs, see fig. 9 for dimentions			0.6			V	
I <sub>I</sub>	CK, $\overline{CK}$	V <sub>I</sub> = V <sub>DDQ</sub> or GND	1.9V			±250	μA	
	OE, OS, FBIN, $\overline{FBIN}$	V <sub>I</sub> = V <sub>DDQ</sub> or GND				±10		
I <sub>DDLD</sub>	Static Supply current, I <sub>DDQ</sub> + I <sub>ADD</sub>	CK and $\overline{CK}$ = L				500		
I <sub>DD</sub>	Dynamic supply current, I <sub>DDQ</sub> + I <sub>ADD</sub> , see note 6 for CPD calculation	CK and $\overline{CK}$ = 410 MHz, all outputs are open (not connected to a PCB)				300	mA	
C <sub>I</sub>	CK, $\overline{CK}$	V <sub>I</sub> = V <sub>DDQ</sub> or GND	1.8V	2		3	pF	
	FBIN, $\overline{FBIN}$	V <sub>I</sub> = V <sub>DDQ</sub> or GND		2		3		
C <sub>I(Δ)</sub>	CK, $\overline{CK}$	V <sub>I</sub> = V <sub>DDQ</sub> or GND						0.25
	FBIN, $\overline{FBIN}$	V <sub>I</sub> = V <sub>DDQ</sub> or GND						0.25

**Notes:**

- Total I<sub>DD</sub> = I<sub>DDQ</sub> + I<sub>ADD</sub> = F<sub>CK</sub> \* C<sub>PD</sub> \* V<sub>DDQ</sub>, solving for C<sub>PD</sub> = (I<sub>DDQ</sub> + I<sub>ADD</sub>) / (F<sub>CK</sub> \* V<sub>DDQ</sub>) where F<sub>CK</sub> is the input frequency, V<sub>DDQ</sub> is the power supply and C<sub>PD</sub> is the Power Dissipation Capacitance.

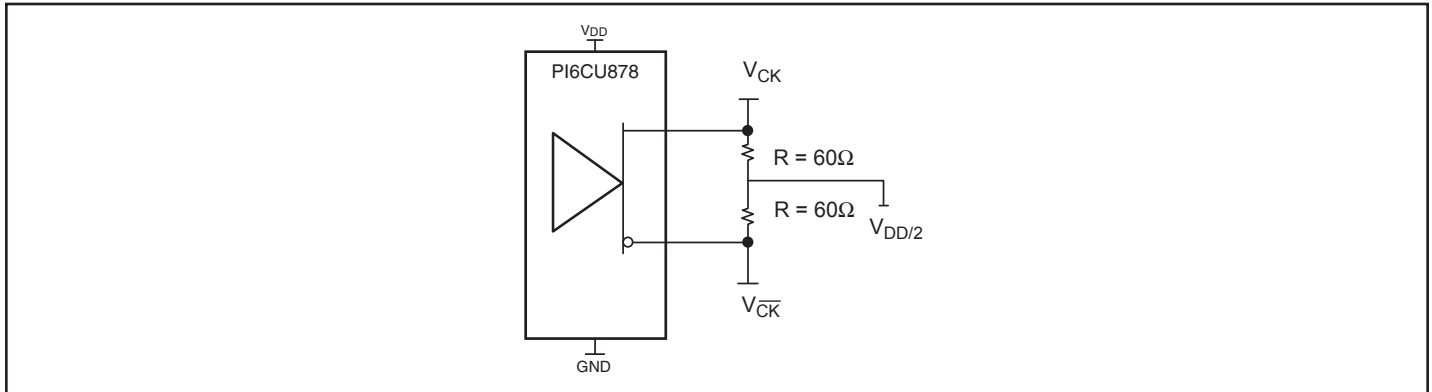
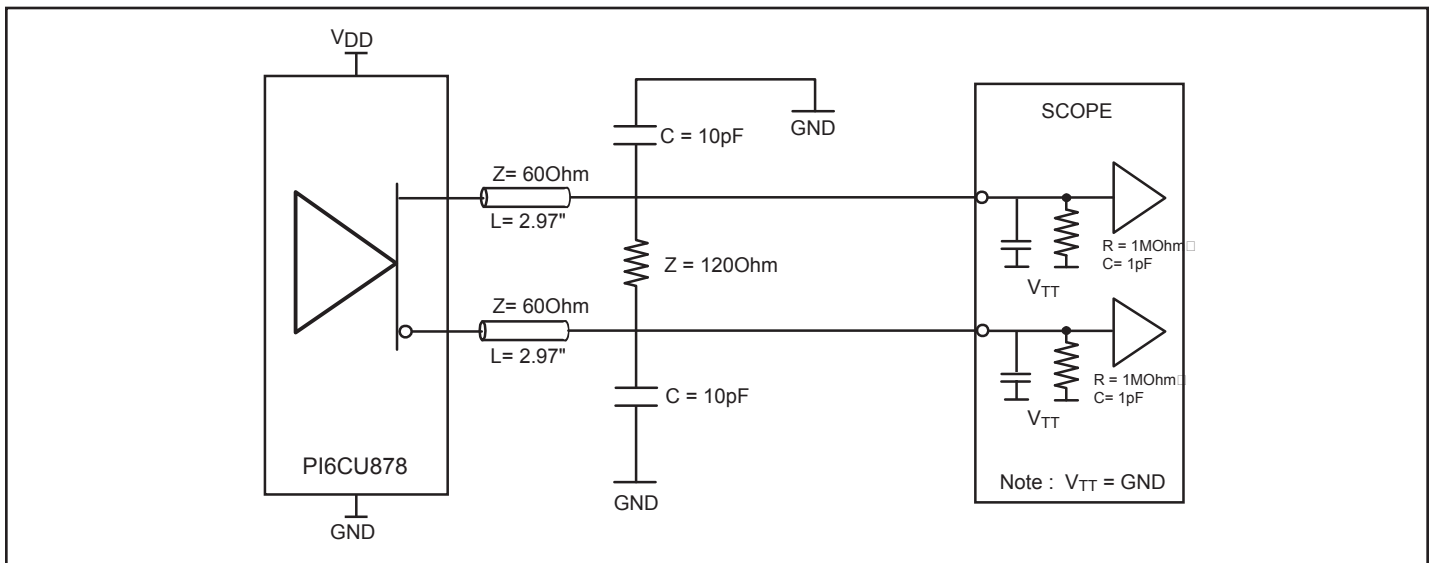
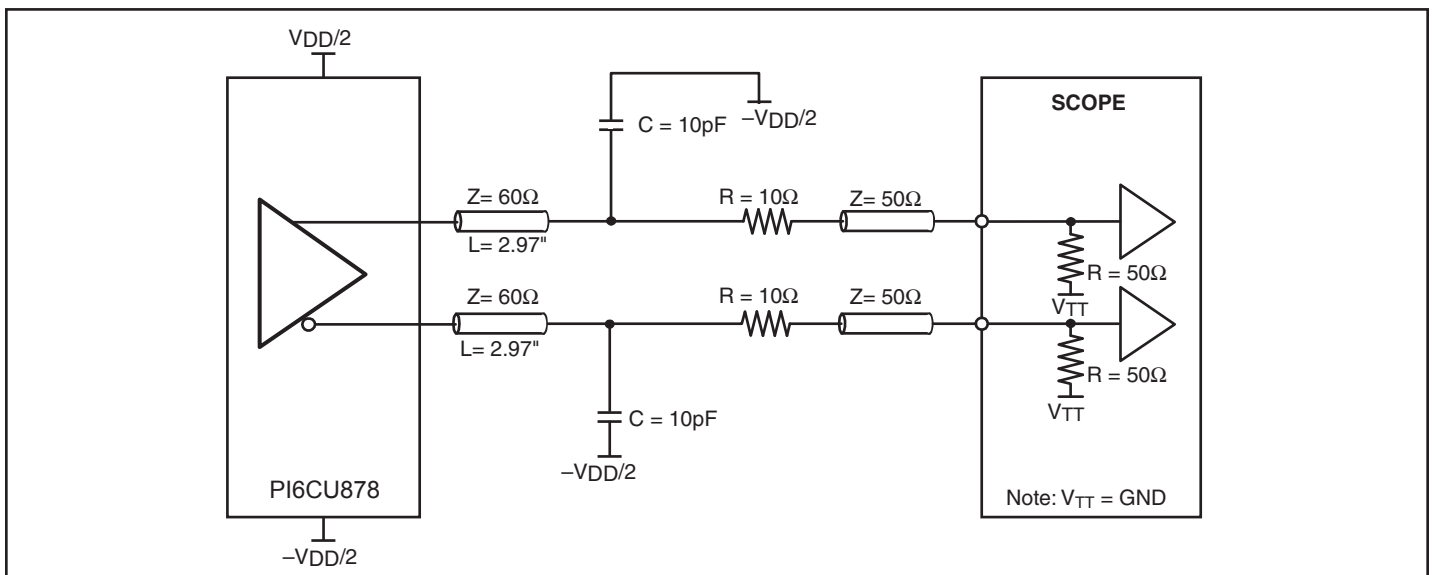
## AC Specifications

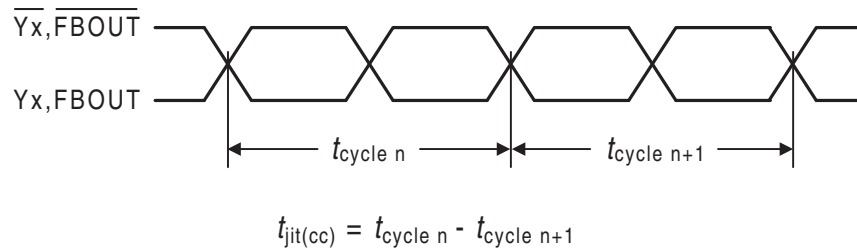
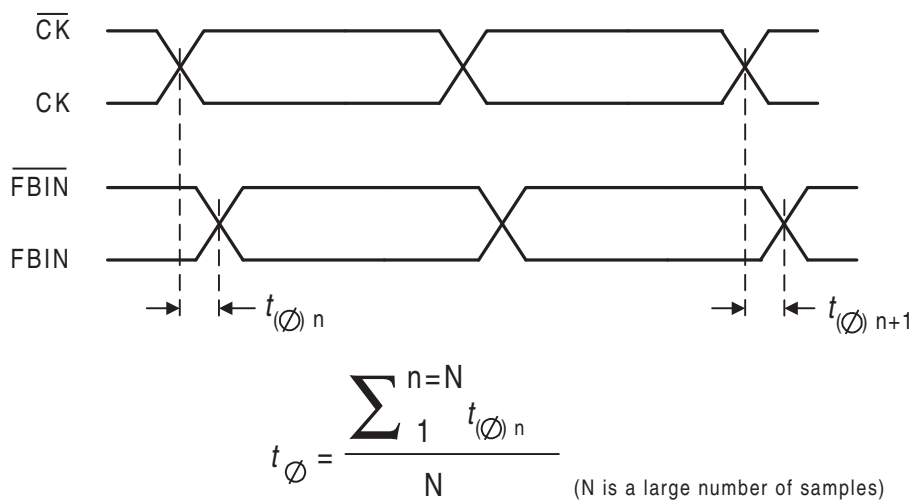
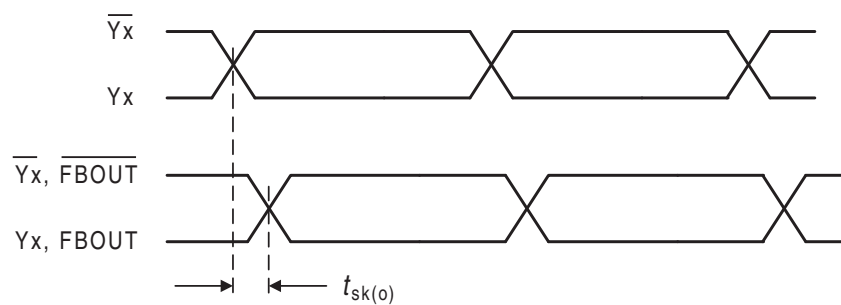
Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)<sup>(15)</sup>

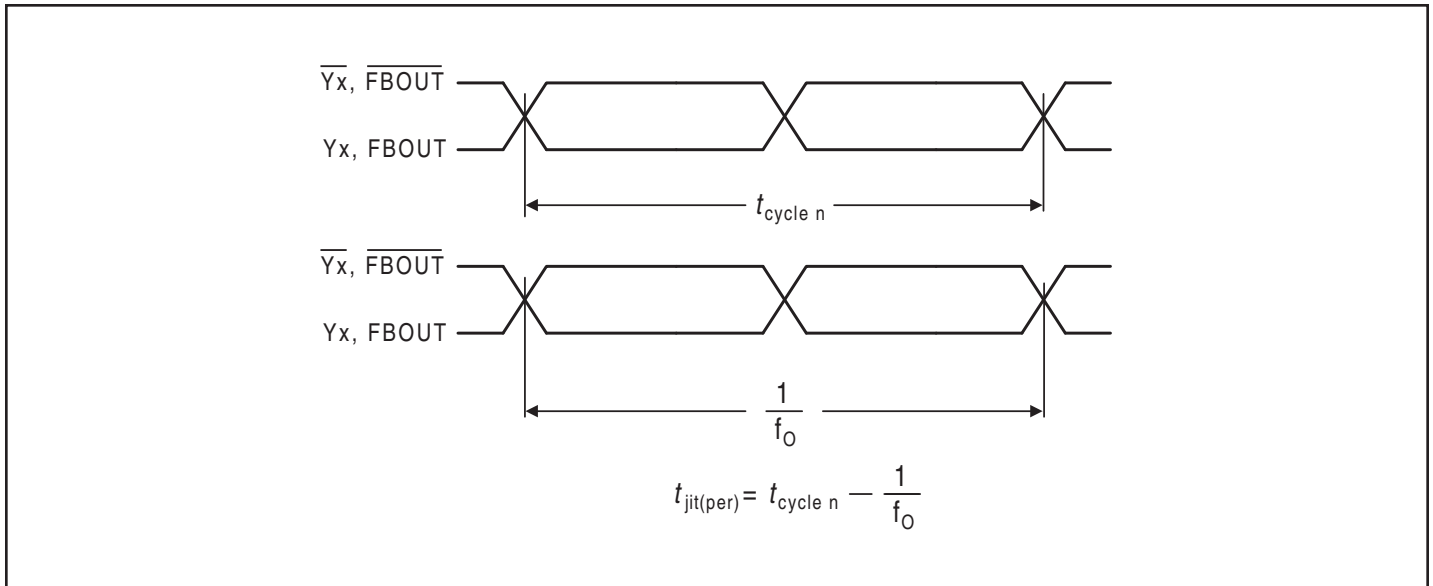
Parameter	Description	Diagram	f <sub>CK</sub> (MHz)	AV <sub>DD</sub> , V <sub>DDQ</sub> = 1.8V ±0.1V			Units
				Min.	Nom.	Max.	
ten	OE to and Y/ $\bar{Y}$	see Fig 11				8	ns
t <sub>dis</sub>	OE to and Y/ $\bar{Y}$	see Fig 11				8	
t <sub>jit(cc+)</sub>	Cycle-to-cycle jitter	see Fig 4		0		40	ps
t <sub>jit(cc-)</sub>				0		-40	
t( $\emptyset$ )	Static phase offset <sup>(11)</sup>	see Fig 5		-50		50	
t( $\emptyset$ ) <sub>dyn</sub>	Dynamic phase offset	see Fig 10		-50		50	
tsk(o)	Output clock skew	see Fig 6				40	
t <sub>jit(per)</sub>	Period jitter <sup>(12)</sup>	see Fig 7		-40		40	
t <sub>jit(hper)</sub>	Half period jitter <sup>(12)</sup>	see Fig 8	160 to 270	-75		75	
	Half period jitter <sup>(12)</sup>	see Fig 8	271 to 350	-50		50	
$\sum t$ (su)	t <sub>jit(per)</sub>   +   t( $\emptyset$ ) <sub>dyn</sub>   + tsk(o) (see note 17)		271 to 410			80	
$\sum t$ (h)	t( $\emptyset$ ) <sub>dyn</sub>   + tsk(o) (see note 17)		271 to 410			60	
slr(i)	Input clock slew rate	see Fig 9		1	2.5	4	V/ns
	Output enable (OE)	see Fig 9		0.5			
slr(o)	Output clock slew rate <sup>(14, 16)</sup>	see Fig 1, 9		1.5	2.5	3	
V <sub>OX</sub>	Output differential-pair cross voltage <sup>(13)</sup>	see Fig 2		(V <sub>DDQ</sub> /2) -0.1		(V <sub>DDQ</sub> /2) +0.1	V
The PLL on the PI6CUA878 is capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:							
	SSC modulation frequency			30.00		33	kHz
	SSC clock input frequency deviation			0.00		-0.50	%
PI6CUA878 PLL design should target the values below to minimize the SCC induced skew:							
	PLL Loop Bandwidth			2.0			MHz

### Notes:

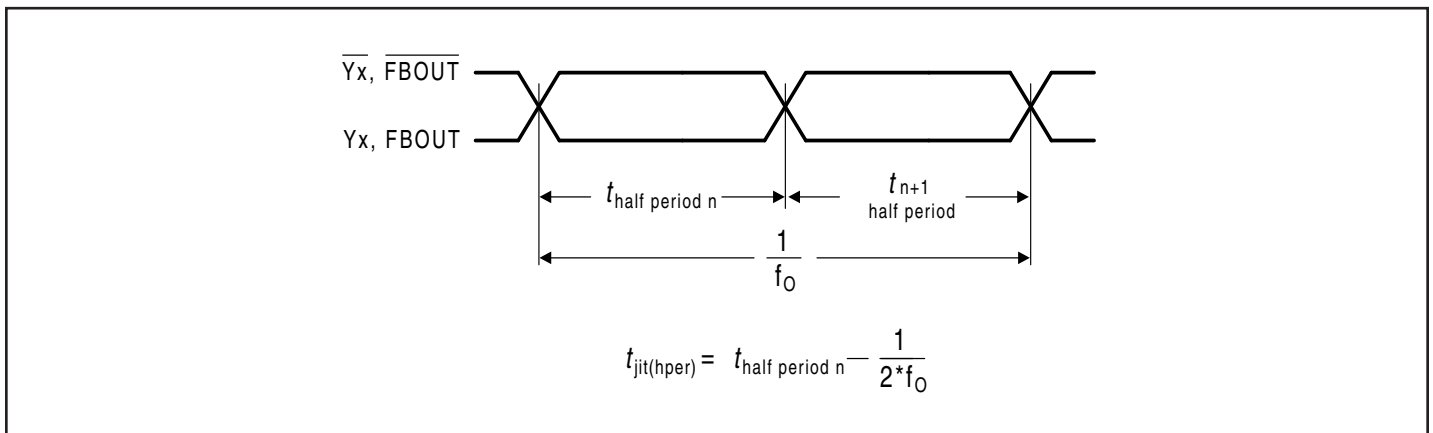
- Static Phase Offset does not include Jitter
- Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
- VOX specified at the DRAM clock input or the test load.
- To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK,  $\bar{CK}$  and Feedback Clock Input FBIN,  $\bar{FBIN}$  are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these Nom values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- There are two terminations that are used with the above ac tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross-voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables should be used.
- The Output slew rate is determined from IBIS model load shown in Figure 1. It is measured single-ended.
- In the Frequency Range of 271 MHz to 410 MHz, the minimum and maximum values for t<sub>jit(per)</sub> and t( $\emptyset$ )<sub>dyn</sub> and the minimum value for tsk(o) must not exceed the corresponding minimum and maximum values of the 160 MHz to 270 MHz range and sum of the specified values for | t<sub>jit(per)</sub> |, | t( $\emptyset$ )<sub>dyn</sub> | and tsk(o) must meet the requirement for  $\sum t$ (su) and the sum of the specified values for | t( $\emptyset$ )<sub>dyn</sub> | and tsk(o) must meet the requirement for  $\sum t$ (h).


**Figure 1. IBIS Model Output Load**

**Figure 2. Output Load Test Circuit 1**

**Figure 3. Output Load Test Circuit 2**

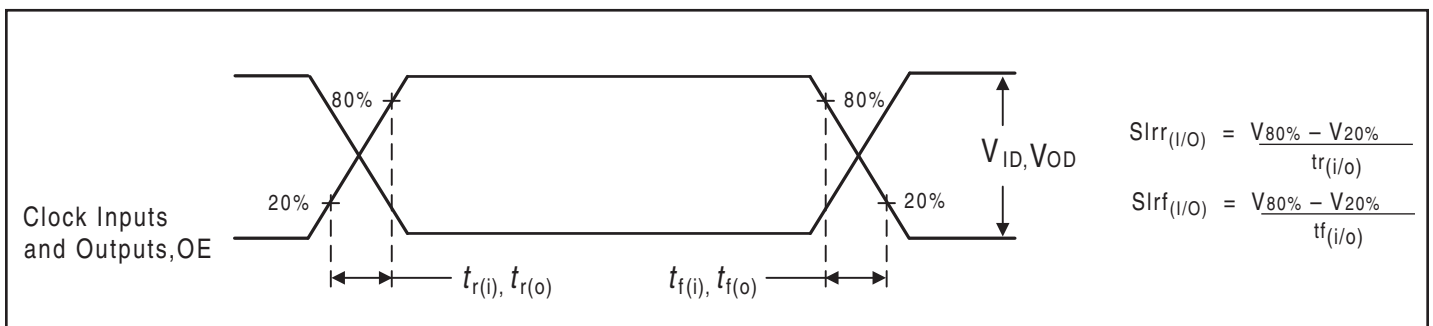

**Figure 4. Cycle-to-Cycle Jitter**

**Figure 5. Static Phase Offset**

**Figure 6. Output Skew**



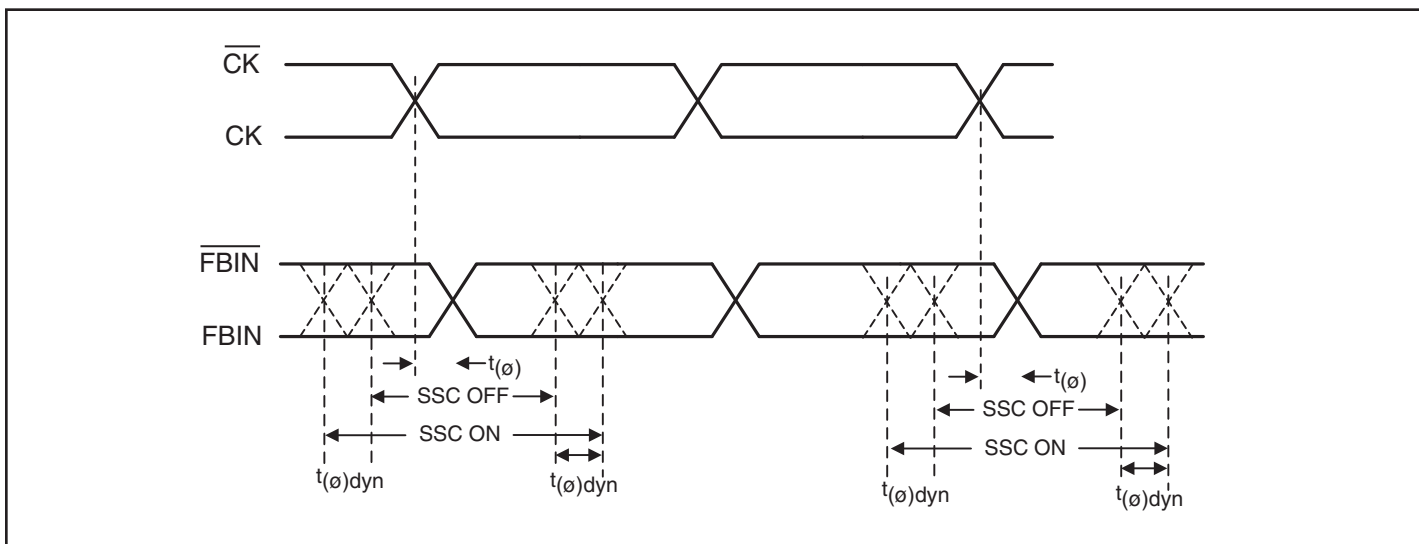
**Figure 7. Period Jitter** (fo = average input frequency measured at CK/CK)



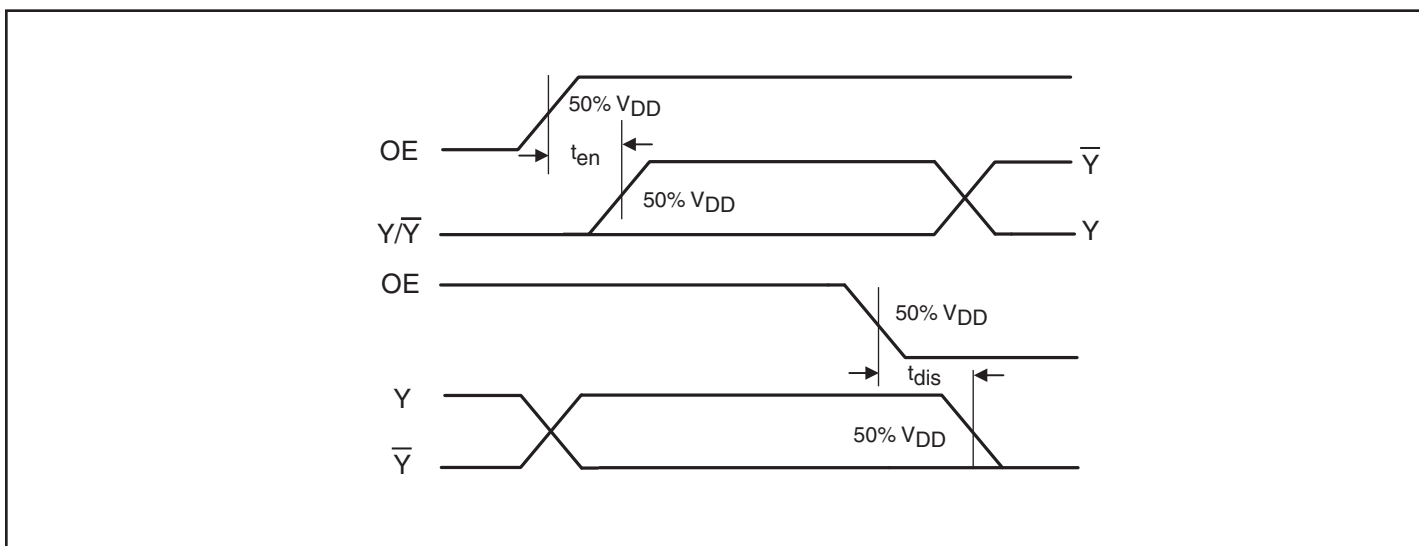
**Figure 8. Half-Period Jitter**



**Figure 9. Input and Output Slew Rates**



**Figure 10. Dynamic Phase Offset**



**Figure 11. Time Delay Between Output Enable (OE) and Clock Output ( $\overline{Y}$ , Y)**

