

Low Power Spread Spectrum Frequency Multiplier SSCG-GP Family

Features

- 10 to 30MHz input frequency range
- 4x frequency multiplication
- Operating voltages of 2.5 V or 3.3V
- Selectable Spreading Ratio : -1.20%, -1.40%, $\pm 0.60\%$, $\pm 0.70\%$ and 0% typical at 14MHz/28MHz input
- Modulation Rate: $F_{in} / 320 (10 \text{ MHz} \leq F_{in} \leq 20 \text{ MHz})$
 $F_{in} / 640 (20 \text{ MHz} \leq F_{in} \leq 30 \text{ MHz})$
- Low power dissipation
- Low jitter
- 8-pin SOIC Packages

Applications

The PI6C3614 can be used in most multimedia applications and embedded systems including but not limited to the following:

- PDAs
- DSCs
- Printers/ MFPs
- Media players
- Portable-TVs
- Embedded digital video devices
- CD-ROM, VCD and DVD players
- LCD Panel Modules
- Automotive components
- Networking devices

Description

The PI6C3614 is a Low Power Spread Spectrum Frequency Multiplier and part of the Pericom SSCG-GP family. The part generates one 4x modulated output from a single clock source or a crystal, and is designed to reduce electromagnetic interference (EMI) by spreading the clock. This reduction in EMI can result in significant system cost saving and less design complexity by reducing the number of circuit board layers ferrite beads and shielding. In the absence of a spread spectrum clock, other EMI-reducing components are required in order to comply with regulatory agency requirements.

The 4x frequency multiplication output can reduce the system design complexity by eliminating higher frequency order crystals. This reduction in system complexity can result in faster design time, cost saving, higher system accuracy and performance.

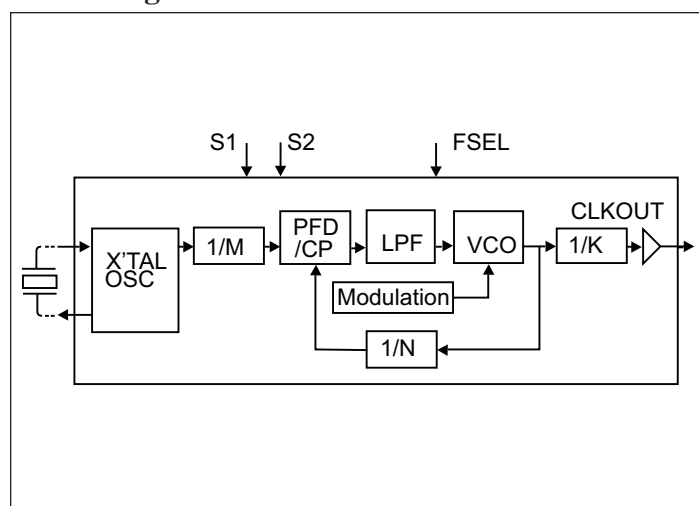
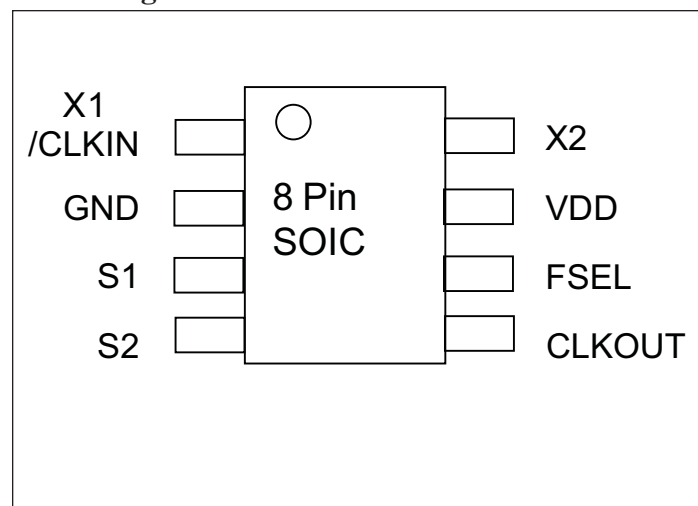
The Spreading Ratio is selectable using the selection pins. The PI6C3614 provides -1.20%, -1.40%, $\pm 0.60\%$, $\pm 0.70\%$ diversified and 0% spread modulation through external logic stage setting.

The chip is packaged in the 8-pin SOIC. The reduced size of the package outline can save precious board space and make layout easier.

PI6C3614 is one of the clock products provided by Pericom. If your application needs a clock product with a different specification not currently provided, please contact us for further information or custom design.

Benefits

- Reduction in EMI
- System cost saving
- Reduced system complexity
- faster time to market

Block Diagram

Pin Configuration


Pin Description

Pin Name	Pin No.	IO Type	Description
X1/CLKIN	1	I	Crystal connection or reference frequency input. This pin has multiple functions. It can be connected either to an external crystal or an external reference clock.
GND	2	GND	Ground.
S1	3	I	Spreading Ratio Selection (0, 1); Default = 1; Internal 60K Ω pull-up included.
S2	4	I	Spreading Ratio Selection (0, 1, M); M: Mid-level; Default = 1; Internal 60K Ω pull-up included.
CLKOUT	5	O	Spread spectrum clock output.
FSEL	6	I	Frequency Range Selection (0, 1); Default = 1; Internal 60K Ω pull-up included
VDD	7	PWR	Power Supply
X2	8	O	Crystal connection. If using an external reference, this pin must be left unconnected.

Spreading Ratio Configuration

VDD = 2.5V \pm 5%, 3.3V \pm 10%, Ambient Temperature 25°C

Fin (MHz)	FSEL	(S1,S2) = (0,0)	(S1,S2) = (0,1)	(S1,S2) = (1,0)	(S1,S2) = (1,1)	(S1,S2) = (1,M)	Modulation Rate (KHz)
		Down	Down	Center	Center		31.25~62.5
11	0	-1.50%	-1.70%	\pm 0.75%	\pm 0.85%	No Spread	Fin/320
14	0	-1.20%	-1.40%	\pm 0.60%	\pm 0.70%	No Spread	Fin/320
15	0	-1.20%	-1.40%	\pm 0.60%	\pm 0.70%	No Spread	Fin/320
19	0	-1.00%	-1.20%	\pm 0.50%	\pm 0.60%	No Spread	Fin/320
20	1	-1.50%	-1.80%	\pm 0.75%	\pm 0.90%	No Spread	Fin/640
25	1	-1.30%	-1.60%	\pm 0.65%	\pm 0.80%	No Spread	Fin/640
28	1	-1.20%	-1.45%	\pm 0.60%	\pm 0.75%	No Spread	Fin/640
30	1	-1.10%	-1.40%	\pm 0.55%	\pm 0.70%	No Spread	Fin/640

Electrical Specification

Maximum Ratings

Supply Voltage to Ground.....	5.5V
All Inputs and Outputs.....	-0.5V to VDD+0.5V
Storage Temperature.....	-65 to +150°C
Junction Temperature.....	150°C
Soldering Temperature.....	260°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC Characteristics

VDD = 2.5V ±5%, Ambient Temperature 0 to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{DD}	Operating voltage		2.375	2.5	2.625	V
V _{IH}	Input high voltage		2.0	–	–	V
V _{IL}	Input low voltage		–	–	0.8	V
V _{OH}	Output high voltage	I _{OH} =-8mA	1.8	–	–	V
V _{OL}	Output low voltage	I _{OL} =8mA	–	–	0.6	V
I _{DD}	Supply current	14MHz / 28MHz input and no load	–	–	4 / 7	mA
Z _{OUT_DOWN}	Nominal output impedance	Down side buffer	–	50	–	Ω
Z _{OUT_UP}	Nominal output impedance	Up side buffer	–	50	–	Ω
C _{IN}	Input capacitance	X1 input pin	–	5	–	pF

AC Characteristics

VDD = 2.5V ±5%, Ambient Temperature 0 to +70°C, Fin=14MHz/28MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
CLKIN	Input Frequency	FSEL=0 => 10 MHz ≤ Fin ≤ 20 MHz	10	–	30	MHz
		FSEL=1 => 20 MHz ≤ Fin ≤ 30 MHz				
CLKOUT	Output Frequency (4X)	FSEL=0 => 10 MHz ≤ Fin ≤ 20 MHz	40	–	120	MHz
		FSEL=1 => 20 MHz ≤ Fin ≤ 30 MHz				
S _{Ratio}	Spreading Ratio	(S1,S2)=(0,0)		-1.20		%
		(S1,S2)=(0,1)		-1.40		
		(S1,S2)=(1,0)		±0.60		
		(S1,S2)=(1,1)		±0.70		
		(S1,S2)=(1,M)		0		
t _{Rise}	Output rise time	Measured from 20% to 80% VDD, 15pF load.	–	1.9	–	ns
t _{Fall}	Output fall time	Measured from 80% to 20% VDD, 15pF load	–	1.9	–	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
t _{j_Short}	Short term jitter	Cycle to cycle jitter	–	200	350	ps
T _{DCIN}	Input duty cycle		40	50	60	%
T _{DCOUT}	Output duty cycle		45	50	55	%

DC Characteristics

VDD = 3.3V ±10%, Ambient Temperature 0 to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{DD}	Operating voltage		3.0	3.3	3.6	V
V _{IH}	Input high voltage		2.0	–	–	V
V _{IL}	Input low voltage		–	–	0.8	V
V _{OH}	Output high voltage	I _{OL} = -8mA	2.5	–	–	V
V _{OL}	Output low voltage	I _{OL} = 8mA	–	–	0.5	V
I _{DD}	Supply current	14MHz/ 28MHz input and no load	–	–	6 / 10	mA
Z _{OUT_DOWN}	Nominal output impedance	Down side buffer	–	45	–	Ω
Z _{OUT_UP}	Nominal output impedance	Up side buffer	–	45	–	Ω
C _{IN}	Input capacitance	X1 input pins	–	5	–	pF

AC Characteristics

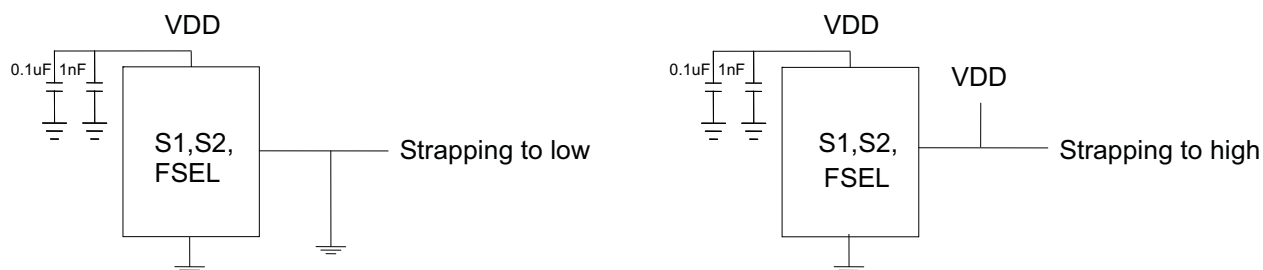
VDD = 3.3V ±10%, Ambient Temperature 0 to +70°C, Fin=14MHz/28MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
CLKIN	Input Frequency	FSEL=0 => 10 MHz ≤ Fin ≤ 20 MHz	10	–	30	MHz
		FSEL=1 => 20 MHz ≤ Fin ≤ 30 MHz				
CLKOUT	Output Frequency(4x)	FSEL=0 => 10 MHz ≤ Fin ≤ 20 MHz	40	–	120	MHz
		FSEL=1 => 20 MHz ≤ Fin ≤ 30 MHz				
S _{Ratio}	Spreading Ratio	(S1,S2)=(0,0)		-1.20		%
		(S1,S2)=(0,1)		-1.40		
		(S1,S2)=(1,0)		±0.60		
		(S1,S2)=(1,1)		±0.70		
		(S1,S2)=(1,M)		0		
t _{Rise}	Output rise time	Measured from 20% to 80% VDD, 15pF load.	–	1.6	–	ns
t _{Fall}	Output fall time	Measured from 80% to 20% VDD, 15pF load	–	1.6	–	ns
t _{j_Short}	Short term jitter	Cycle to cycle jitter	–	200	250	ps
T _{DCIN}	Input duty cycle		40	50	60	%
T _{DCOUT}	Output duty cycle		45	50	55	%

Application Information

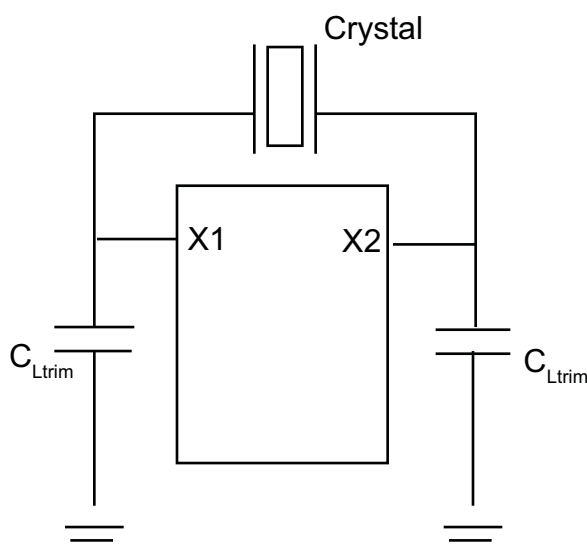
Decoupling Capacitor

Two decoupling capacitors of 0.1 μ F and 1nF must be connected in parallel between VDD and GND. To optimize device performance and to lower output noise, the coupling capacitors should be placed on the component side of the board as close to these pins as possible. There should be no vias placed between the decoupling capacitors and VDD pin. The PCB trace to VDD pin should be as short as possible, and no vias should be placed between VDD and the capacitors in the decoupling circuit.



Crystal Load Capacitor

If a crystal is used with the device, two external trim capacitors, CLtrim, are used to adjust the effective capacitance to match the required crystal load capacitance. The CLtrim value can be derived from formula $CL_{trim} = 2 * CL - (C_s + C_i)$. The typical $CL_{trim} = 28\text{pF}$ when crystal load = 18pF, stray capacitance $C_s = 3\text{pF}$ and XTAL pins capacitance = 5pF.



PCB Layout Recommendation

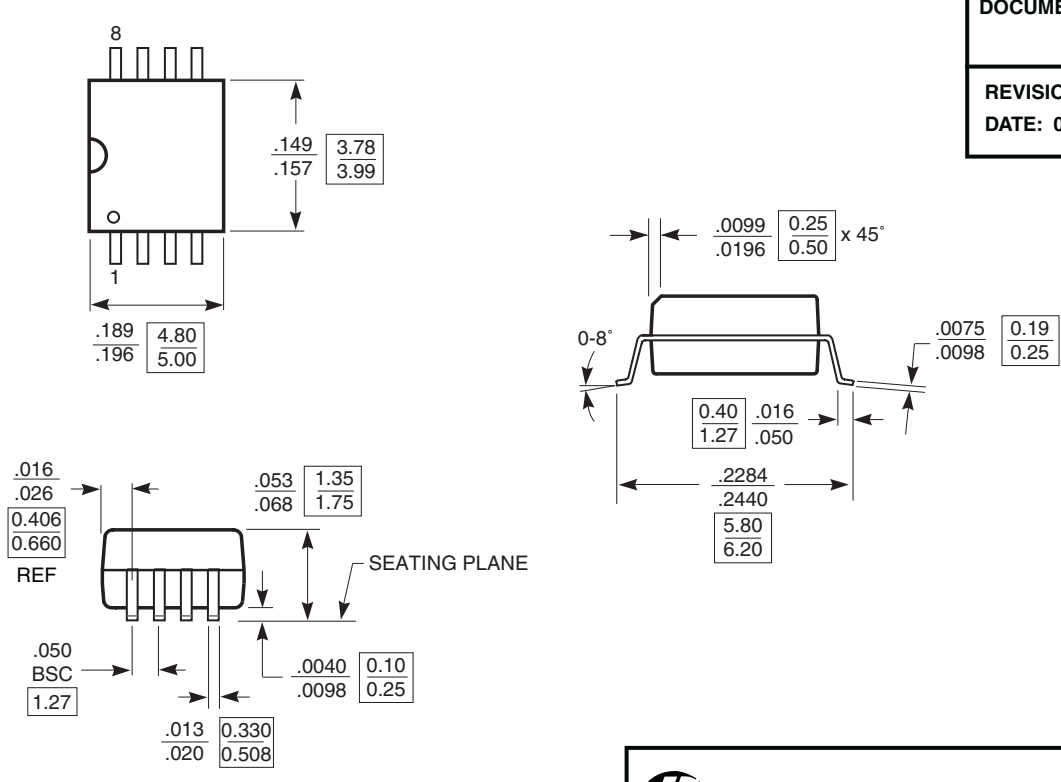
To optimize device performance, all components should be placed on the same side of the board and, therefore, no vias are used through other signal layers. The part should be kept away from other signal traces including ones just underneath the part or on layers adjacent to the ground plane layer used by the part. The PCB trace from the part to the ground via should be kept as short as possible.

Physical Dimensions

Packaging Mechanical: 8-pin, SOIC


DOCUMENT CONTROL NO.
PD - 1001

REVISION: F
DATE: 03/09/05



Notes:

1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012D/AA



Pericom Semiconductor Corporation
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DESCRIPTION: 8-Pin, 150-Mil Wide, SOIC

PACKAGE CODE: W

X.XX DENOTES DIMENSIONS
X.XX IN MILLIMETERS

Ordering Information

Ordering Code	Package Code	Package Description
PI6C3614WE	W	Pb-Free & Green, 8-Pin SOIC

Notes:

1. Thermal characteristics and package top marking information can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green Package
3. Adding an X suffix = Tape/Reel



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