



Actual Size = 7 x 5mm



Product Features

- Less than 1 ps RMS jitter with non-PLL design
- Tight stability over a broad range of operating conditions
- 2.5V LVDS compatible logic levels
- Pin-compatible with standard 7x5mm packages
- Designed for standard reflow & washing techniques
- IBIS models available
- Pb-free & RoHS/Green compliant

Product Description

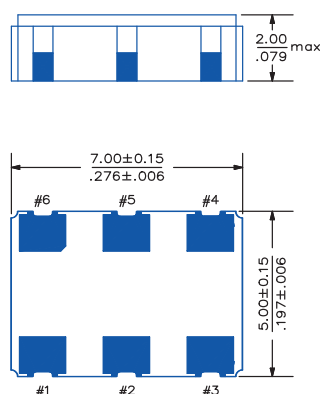
The SDS382 Series is a 2.5V crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVDS logic levels. The device, available on tape and reel, is contained in a 7x5mm surface-mount ceramic package.

Applications

The SDS382 Series is an ideal reference clock for high-speed applications requiring low jitter, including:

- 1/10 Gigabit Ethernet
- 2/4/10G FibreChannel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH linecards
- Passive Optical Network (PON) devices
- HD Video Systems

Packaging Outline



Pin Functions

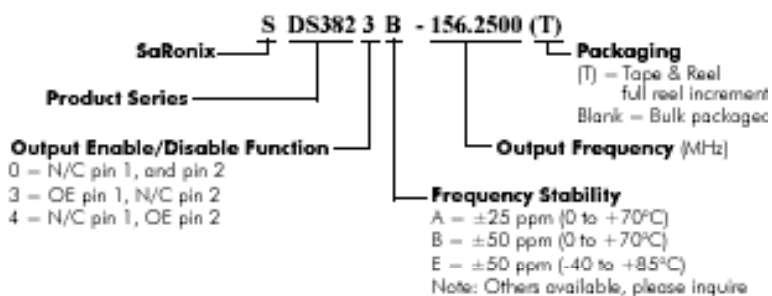
Pin	Function
1	OE or NC
2	OE or NC
3	V _{EE}
4	Q Output
5	\bar{Q} Output
6	V _{CC}

Common Frequencies

Contact SaRonix for additional frequencies

38.8800 MHz	100.0000 MHz	156.2500 MHz
50.0000 MHz	106.2500 MHz	159.3750 MHz
62.5000 MHz	125.0000 MHz	160.0000 MHz
66.0000 MHz	133.0000 MHz	161.1328 MHz
66.6667 MHz	148.3516 MHz	
74.1758 MHz	148.5000 MHz	
75.0000 MHz	150.0000 MHz	
77.7600 MHz	155.5200 MHz	

Ordering Information



Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output frequency	38.88		162	MHz	As specified
Supply voltage	2.375	2.5	2.625	V	
Supply current		50	75	mA	Enabled
Supply current			0.03	mA	Disabled
Frequency stability			±25 to ±50	ppM	See Note 1 below
Operating temperature	-40		+85	°C	As specified
Output amplitude differential	500		900	mVpp	
Output load	100Ω and 5pF LVDS				output requires termination
Duty cycle	45		55	%	measured 50% of waveform
Rise and fall time		500	850	ps	measured 20/80% of waveform
Jitter, phase		0.5	1	ps RMS (1-σ)	12kHz to 40MHz frequency band
Jitter, total			25	ps pk-pk	100,000 random periods

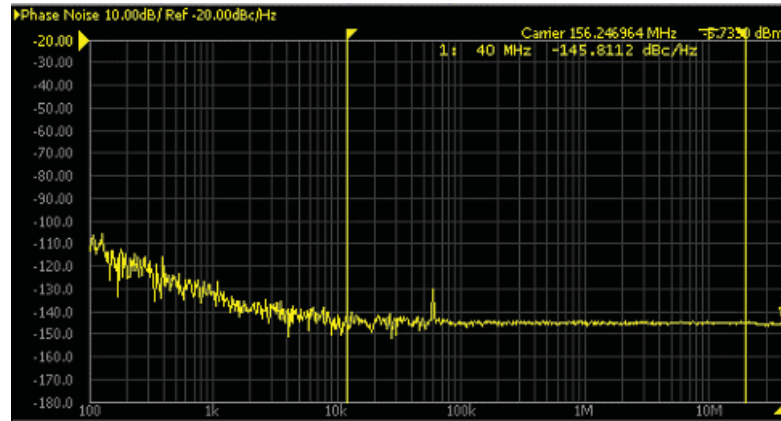
Notes:

- As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (5 years at 40°C average effective ambient temperature), shock and vibration.

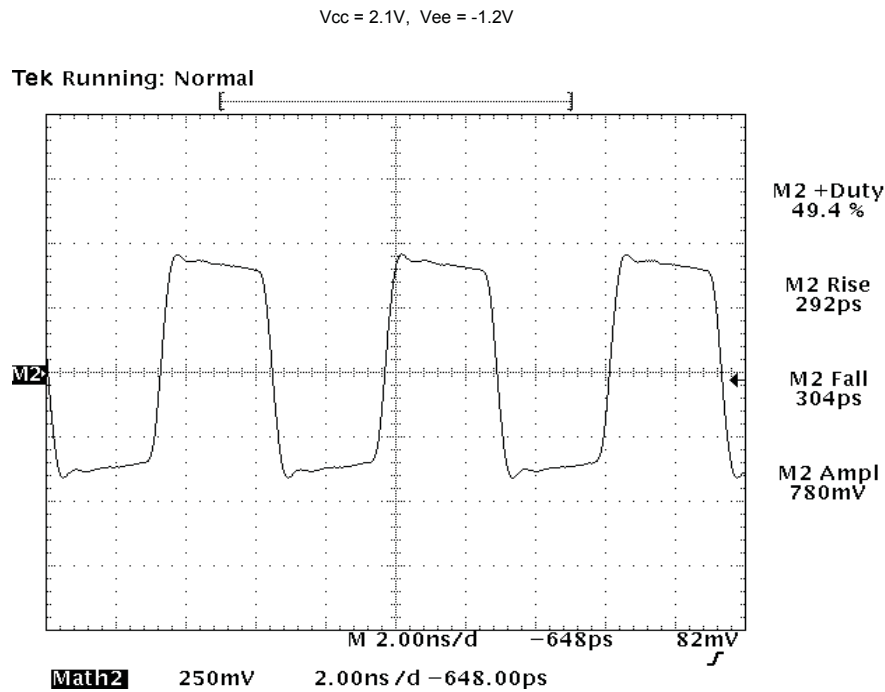
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (OE pin), Output Enable	70% V _{CC}			V	or open
Input voltage (OE pin), Output Disable			30% V _{CC}	V	Outputs disabled to Hi-Z
Internal Pull-up Resistance	50			kΩ	
Output disable delay			200	ns	
Output enable delay			10	ms	

Typical Phase Noise



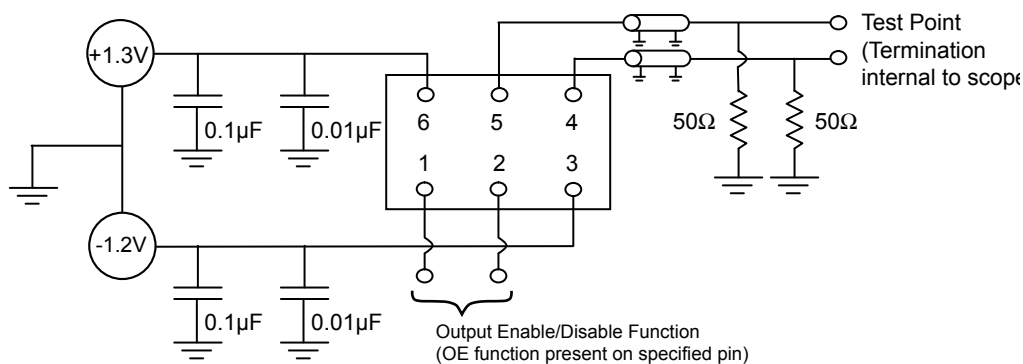
Typical Output Waveform



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

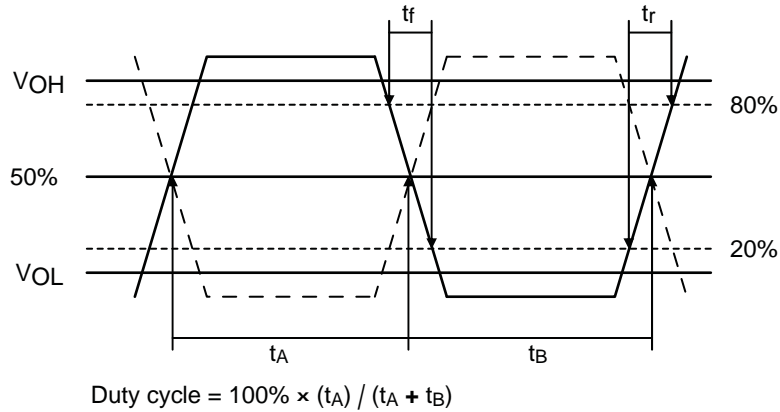


Reliability Test Ratings

This product is rated to meet the following test conditions:

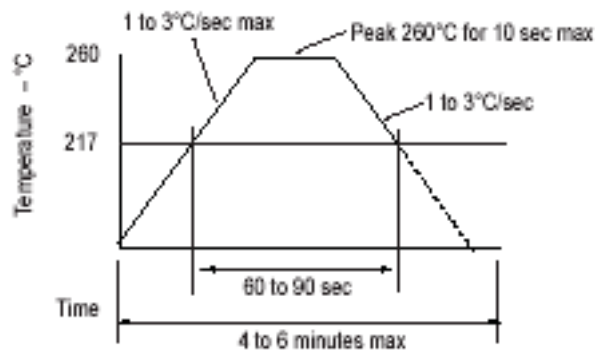
Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

Output Waveform

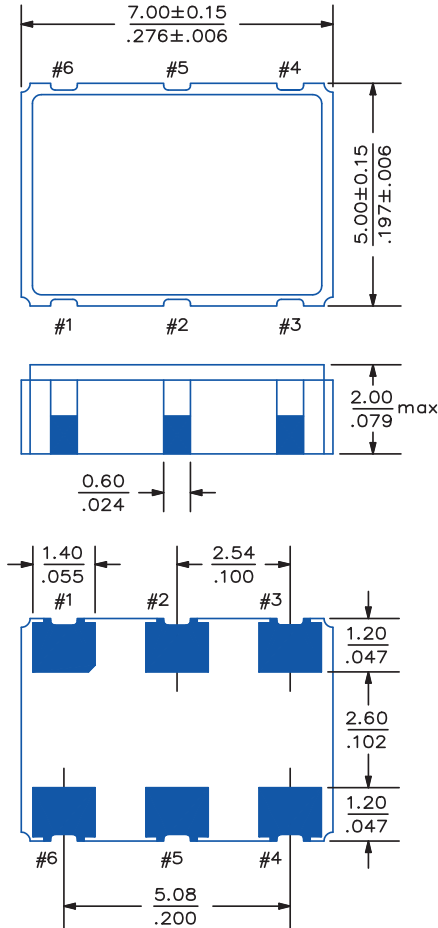


Reflow Soldering Profile

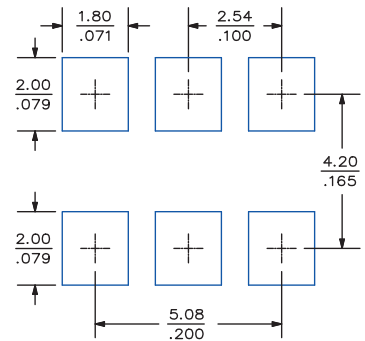
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended. (see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1: SDS382 X (SaRonix, Model, Stability code)
Marking LINE 2: Frequency (Frequency code)
Marking LINE 3: ● YY WW X (Pin 1, Year, Week, Origin)

**** Exact location of markings may vary**