

**Product:** PCIe<sup>®</sup> Packet Switch – 4-port / 24-lane

**Part Numbers:** PI7C9X20424

## Product Description

The PI7C9X20424 is a 4-port, 24-lane, PCI Express<sup>®</sup> Packet Switch conforming to the *PCI Express Base Specification* Revision 1.1. Part of Pericom's *Packet24* Series of PCI Express switches, the PI7C9X20424 may be configured through hardware to provide a single upstream port supporting x8, x4, x2 or x1 operation, with 3 downstream ports supporting x8, x4, x2 or x1 operation. This provides users the flexibility to expand or fanout a PCI Express port for applications such as motherboards, add-in cards, and docking stations.

## Industry Specifications Compliance

- PCI Express<sup>®</sup> Base Specification, Revision 1.1
- PCI Express CEM Specification, Revision 1.0
- PCI-to-PCI Bridge Architecture, Revision 1.2
- Advanced Configuration Power Interface (ACPI) Specification
- PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification, Revision 1.0

## Enhanced Features

- Under 160ns latency for packet running through switch without blocking
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for switching packets
- Supports up to 256-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port

## Features

- Non-blocking full-wired switching capability at 96Gbps when all 24 lanes are enabled
- Peer-to-peer switching between any 2 downstream ports
- 409-pin PBGA 31 x 31mm package, 1.27mm ball pitch
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
  - Hot Plug support
  - IEEE 1149.6 JTAG interface support

- Link Power Management
  - Supports L0, L0s, L1, L2, L2/L3<sub>Ready</sub> and L3 link power state
  - Active state power management for L0s and L1 state
  - Beacon or Wake# support in L2 state
- Device State Power Management
  - Supports D0, D3Hot and D3Cold device power state
  - 3.3V Aux Power support in D3Cold power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended virtual channel capability
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Non-enabled VC buffer assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping per each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
  - Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Header/Data queue at each VC of each port
  - Four-entry non-posted request header and data (VC0 only) queue
  - Four-entry posted request header queue
  - Four-entry completion header queue
  - 512-byte posted write data buffer
  - 512-byte completed read data buffer

### PI7C9X20424 - Application

