

Product: PCI Express®-to-PCI/PCIX Reversible Bridge

Part Numbers: PI7C9X130

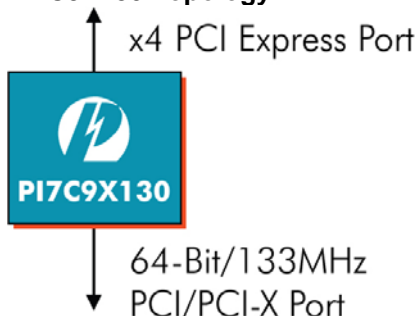
Product Description

As one of the leading PCI Express® Solution Providers, Pericom is committed to introducing a line of performance tuned PCI Express Bridge Products. The PI7C9X130 is composed of one x4 PCI Express port and one standard 64-bit /133 MHz PCIX port. The versatile PI7C9X130 is capable of both “forward” and “reverse” bridging. In “forward” mode, the PI7C9X130 is configured with the PCI Express port on the primary and the PCI/PCIX port on the downstream side. The typical usage in this configuration is to “bridge” legacy PCI/PCIX product to PCI Express systems. In “reverse” mode, the PI7C9X130 is configured with the PCIX port on the primary and the PCI Express port on the downstream side. The “reverse” configuration will be mainly used to “bridge” new PCI Express products to legacy PCI/PCIX systems.

Industry Specifications Compliance

- PCI Express® Base Specification, Revision 1.1
- PCI Express CEM Specification, Revision 1.1
- PCI Express to PCI/PCI-X Bridge Specification, Rev 1.0
- PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a
- PCI-to-PCI Bridge Architecture Specification, Rev 1.2
- PCI Local Bus Specification, Revision 3.0
- PCI Hot-Plug Specification, Revision 1.1
- PCI SHPC and Subsystem Specification, Revision 1.0
- PCI Mobile Design Guide, Version 1.1
- System Management (SM) Bus, Version 2.0
- PCI Bus PM Interface Specification, Revision 1.1

PI7C9X130 Topology



Features

- Fully Reversible
 - Forward – PCIe primary, PCIX secondary
 - Reverse – PCIX primary, PCIe secondary
- Maximum Payload Size – Up to 512 bytes
- Transparent and Non-transparent mode
- GPIO Support
 - 7 dedicated bi-directional
 - When external arbiter is used:
 - 4 additional outputs
 - 4 additional inputs
- Masquerade support
 - User defined vendor, device, revision, subsystem device, and subsystem vendor ID
- Large 8KB Buffer
 - 2 KB for reads & 2 KB for writes per port
- 17 x 17m, 256-pin PBGA, 1MM Ball Pitch

PCI Express Features

- Virtual Isochronous Support
 - Upstream TC 1 – 7 generation
 - Downstream TC 1 – 7 mapping
- 16-bit CRC, LCRC (32-bit)
- ECRC and Advanced Error Reporting
- Error Forwarding (Data Poisoning)
- Polarity Toggle
- VDDAUX Support (1.8V)
- Hot Plug Support

PCI/PCIX Features

- Two Level Internal Arbitration
- Support for up to 6 bus masters
- 3.3V Signaling with 5V I/O Tolerance
- PME# Support
- 16-bit Address Decode for VGA
- CLKRUN# Support
- VAUX Support (3.3V)
- Hot Plug Support
- Subsystem Device and Subsystem Vendor ID
- MSI and INT Support
- SM Bus
- PHY, data link, network layer, PEC, ARP, etc.
- I2C Serial EEPROM Support