



PI7C9X7958/PI7C9X7954/PI7C9X7952
Evaluation Board
User's Manual

PI7C9X7958/PI7C9X7954/PI7C9X7952 PCI Express Octal/Quad/Dual UART Evaluation Board User's Manual

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REVISION HISTORY

Date	Revision Number	Description
10/25/2007	0.1	Preliminary User's Manual
11/14/2007	0.2	Added Table 3.4 DB-62 Connector Pin Assignment

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1. General Information

The PI7C9X7958/ PI7C9X7954/ PI7C9X7952 Evaluation Board is built on the PI7C9X7958/ PI7C9X7954/ PI7C9X7952, a PCI Express Octal/Quad/Dual UART. The evaluation board is a rapid and complete solution for software and hardware development with low risk and fast time-to-market. The evaluation board allows the upstream port of the PI7C9X7958/PI7C9X7954/PI7C9X7952 UART to be directly plugged into a x1 PCI Express slot on a system board. The downstream port of the evaluation board allows serial connections to other devices.

1.1. PI7C9X7958/PI7C9X7954/PI7C9X7952 Features

- x1 PCI Express link host interface
- Eight (PI7C9X7958), four (PI7C9X7954), and two (PI7C9X7952) high performance 950-class UARTs
- Compliant with PCI Express Base Specification 1.1
- Compliant with PCI Express CEM Specification 1.1
- Compliant with PCI Power Management 1.2
- Fully 16C550 software compatible UARTs
- 128-byte FIFO for each transmitter and receiver
- Baud rate up to 15 Mbps in asynchronous mode and 62.5Mbps in synchronous mode
- Flexible clock prescaler from 1 to 31.875
- Automated in-band flow control using programmable Xon/Xoff in both directions
- Automated out-of-band flow control using CTS#/RTS# and/or DSR#/DTR#
- Arbitrary trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-of-band flow control
- Global Interrupt Status and readable FIFO levels to facilitate implementation of efficient device drivers
- Detection of bad data in the receiver FIFO
- Data framing size including 5, 6, 7 and 8 bits
- Hardware reconfiguration through Microwire compatible EEPROM
- Operations via I/O or memory mapping
- Dual power operation (1.8V for PCIe I/O and core, 3.3V for UART I/O)
- PI7C9X7958 in 160-pin LFBGA package and PI7C9X7954/PI7C9X7952 in 128-pin LQFP package

1.2. PI7C9X7958/PI7C9X7954/PI7C9X7952 Evaluation Board Features

- Supports one x1 upstream PCI Express port
- One DB-62 connector for UARTs
- DIP switches for the hardware configuration of PI7C9X7958/PI7C9X7954/PI7C9X7952
- Serial EEPROM support
- LED indicators for visual inspection

1.3. Evaluation Board Front View

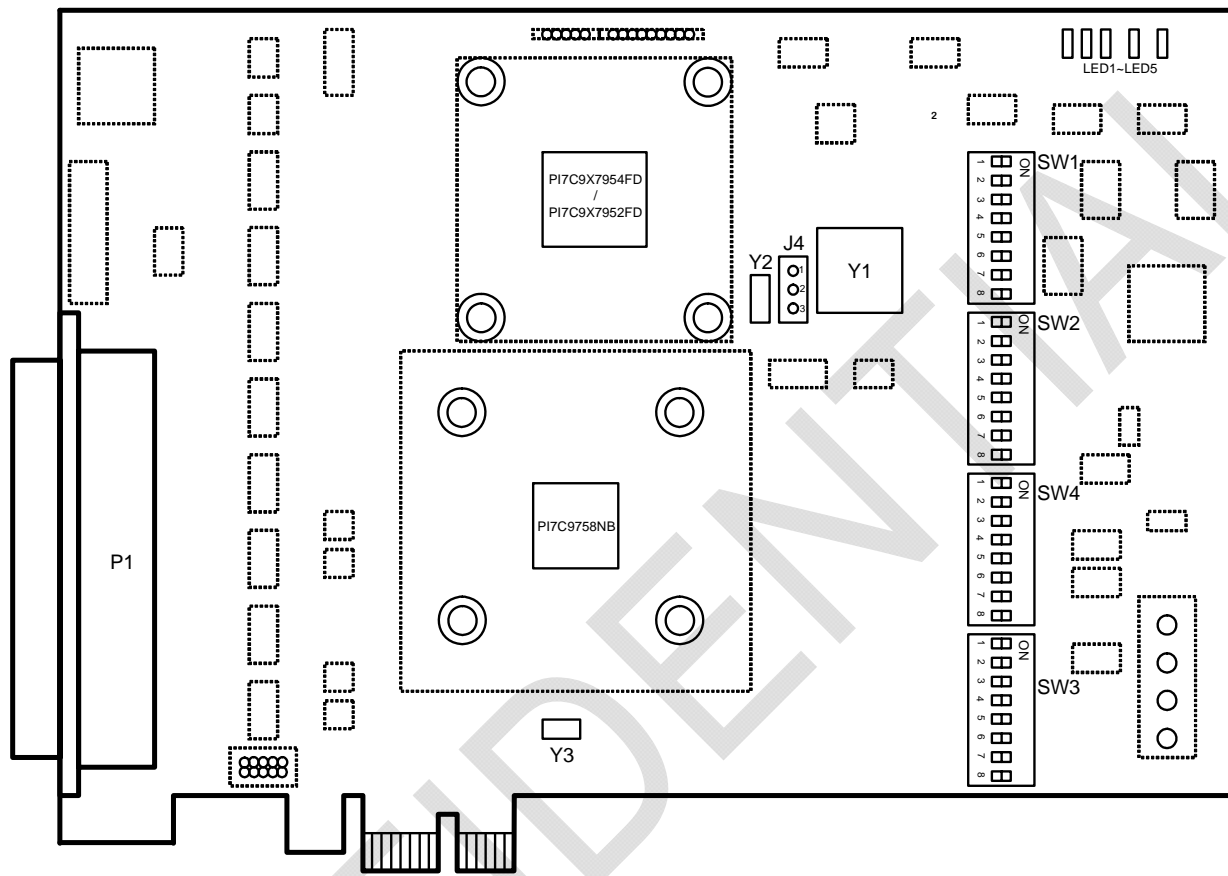


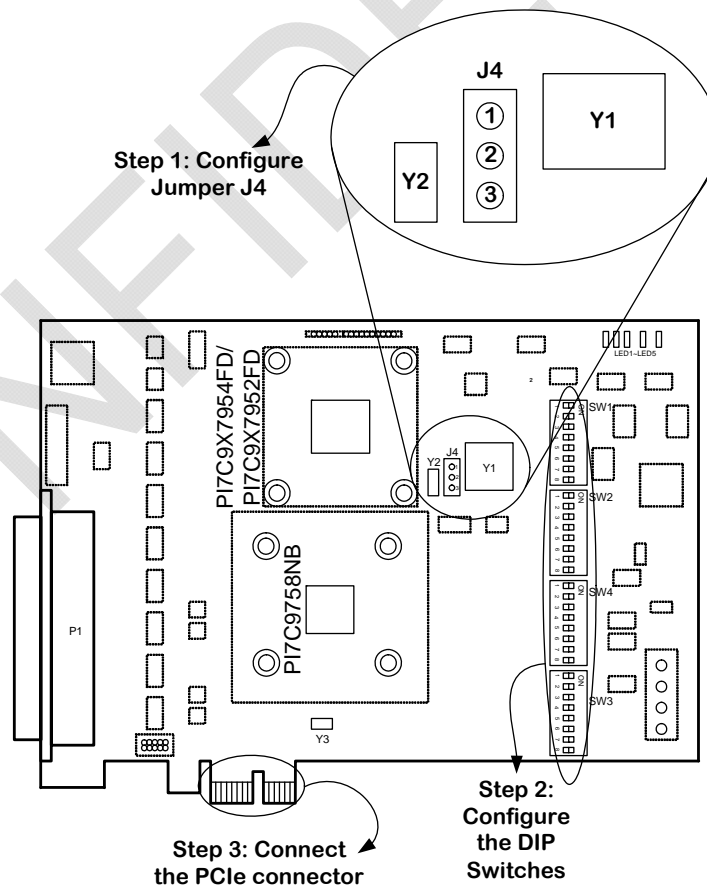
Figure 1-1 PI7C9X7958/PI7C9X7954/PI7C9X7952 Evaluation Board Front View

2. Initial Setup

- Step 1. Configure Jumper Pins (J4). Please refer the table 2-1 below.
- Step 2. Configure the DIP Switches. Please refer to section 3.2 for the default settings.
- Step 3. Connect the upstream PCI Express connector (P1) of the evaluation board to the PCI Express slot on the Root Complex.

Table 2-1 Jumper J4 Configuration

UART in Use	Oscillator (Y1) as the Clock Source	Crystal (Y2, Y3) as the Clock Source
PI7C9X7958	Strap Jumper Pin 1 and Jumper Pin 2 on J4. Make sure crystal Y2 and Y3 are not used. Use oscillator Y1 as the clock source.	Make sure none of the jumper pins on J4 are strapped. Use crystal Y3 as the clock source.
PI7C9X7954/ PI7C9X7952	Strap Jumper Pin 2 and Jumper Pin 3 on J4. Make sure crystal Y2 and Y3 are not used. Use oscillator Y1 as the clock source.	Make sure none of the jumper pins on J4 are strapped. Use crystal Y2 as the clock source.



3. On-Board LED Indicators, Switches, and Jumpers

3.1. LED Indicators

The evaluation board provides a number of LED indicators to conveniently display the status of the output signals. The name and function of each of the indicator is listed and explained in the table below.

Table 3-1 LED Indicator Description

LED Location	Name	Function	Description
D1 to D3	1.8V	1.8V System Power	Indicates the status of the 1.8V system power supply. It is active-high.
D4	3.3V	3.3V System Power	Indicates the status of the 3.3V system power supply. It is active-high.
D5	12V	12V System Power	Indicates the status of the 12V system power supply. The indicator is active-high.

3.2. DIP Switches

The evaluation board includes user-controllable DIP switches for selecting and controlling various functionalities. Each DIP Switch's status can be set to either ON (0) or OFF (1).

Table 3-2 DIP Switch Function Description

Switch	Position	Name	Function	Function Description	Default Value
SW1	1	PHY_MODE	Reserved		0
	2	DEBUG_MODE	Reserved		0
	3	EEPROM_BYPASS	EEPROM Bypass	When this switch is set to "1", the EEPROM pre-loading is bypassed, and no configuration data is loaded from the EEPROM. Otherwise, the EEPROM pre-loading is enabled.	0
	4	ORG_PIN	EEPROM Organization Pin	When this switch is set to "1", the EEPROM configuration data is organized in 16-bit structure. Otherwise, 8-bit structure is used.	N/A
	5	SYNCLK_IN_ENABLE	Reserved		0
	6	FAST_MODE	Reserved		0
	7	HIDRV	Reserved		0
	8	LODRV	Reserved		0
SW2	1 to 5	DEBUG_SEL1 to DEBUG_SEL5	Reserved		00000
	6	PME_ENA	PM Enable	When this switch is set to "1", PM is enabled.	0
	7	XA_MODE	Reserved		0
SW3	1	PORT_SEL	Reserved		0
	3	UR_TEST_MODE	Reserved		1
	4 to 5	TXTERM_ADJ0 to TXTERM_ADJ1	Reserved		00
	6 to 7	RXTERM_ADJ0 to RXTERM_ADJ1	Reserved		00
SW4	1 to 4	DTX0 to DTX3	Reserved		0000
	5 to 8	DEQ0 to DEQ3	Reserved		0001

3.3. Connector Ports

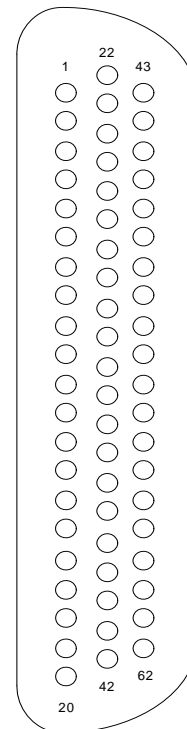
Table 3-3 Connector Port Function

Port	Function
P1	Upstream PCI Express ports. Connects to the Root Complex
DB-62 Connector (Non-standard)	<p>Connects up to eight to serial devices. This port uses a non-standard cable, which is provided with the Evaluation Board.</p> <p>PI7C9X7958: All ports are used.</p> <p>PI7C9X7954: Port 1, 2, 3, and 8 are used. Others are unused</p> <p>PI7C9X7952: Port 1 and 2 are used. Others are unused</p>

*Note: UART Port0 to Port7 correspond to DB-62 Connector Port1 to Port8.

Table 3-4 DB-62 Connector Pin Assignment

Pin	Function	Pin	Function	Pin	Function
1	SOUT[0]	22	SIN[0]	43	CTS[0]
2	DTR[0]	23	DSR[0]	44	RTS[0]
3	SIN[1]	24	DCD[0]	45	GND
4	DSR[1]	25	SOUT[1]	46	CTS[1]
5	DCD[1]	26	DTR[1]	47	RTS[1]
6	SOUT[2]	27	SIN[2]	48	CTS[2]
7	DTR[2]	28	DSR[2]	49	RTS[3]
8	SIN[3]	29	DCD[2]	50	GND
9	DSR[3]	30	SOUT[3]	51	CTS[3]
10	DCD[3]	31	DTR[3]	52	RTS[3]
11	SIN[4]	32	GND	53	CTS[4]
12	DSR[4]	33	SOUT[4]	54	RTS[4]
13	DCD[4]	34	DTR[4]	55	GND
14	SOUT[5]	35	SIN[5]	56	CTS[5]
15	DTR[5]	36	DSR[5]	57	RTS[5]
16	SIN[6]	37	DCD[5]	58	GND
17	DSR[6]	38	SOUT[6]	59	CTS[6]
18	DCD[6]	39	DTR[6]	60	RTS[6]
19	SIN[7]	40	GND	61	CTS[7]
20	DSR[7]	41	SOUT[7]	62	RTS[7]
21	DCD[8]	42	DTR[7]		



3.4. Jumpers

Table 3-5 Jumpers

Port	Function
J4	Configures the clock source from the oscillator or the crystal. Refer to table 2-1 for the configuration.

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