

Application: HDTV Networking (SMPTE292M) SaRonix device: S1569, S1613, ST1308, ST1317 Oscillators

Overview

As High Definition Television (HDTV) services increase, broadcasting networks are upgraded to move uncompressed HD signals between cameras, disk storage arrays, video routers, VTRs, workstations, test equipment, pattern generators, and monitors. The SMPTE292M standard establishes the process for transmitting 20-bit parallel words in a single, serialized 1.485 Gbps (or 1.485/1.001 Gbps) bit stream through coaxial or fibre cabling. This standard enables cost-effective high-bandwidth connectivity between HD video devices (see Fig 1).

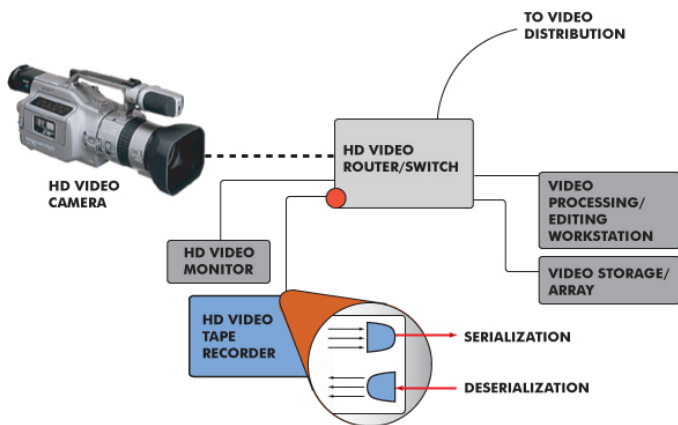


Figure 1: 1.485 Gbps SMPTE292M Network

The key to maintaining a high quality video stream throughout the network is to control jitter. Bit errors occur as jitter accumulates in the video signal, resulting in unsightly visual defects in the final video image. Areas of the network that are susceptible to jitter include the serialization process, the transmission cable (coaxial or fibre), and the clock/data recovery function in the deserializer (see Figure 2). SaRonix products minimize jitter in the serialization/deserialization processes.

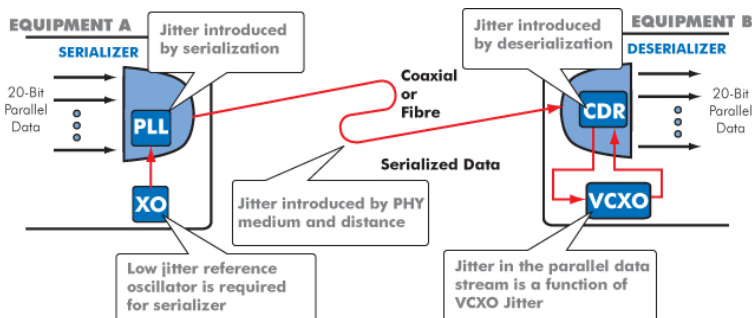


Figure 2: Points of Jitter Accumulation

SaRonix Solution: Serialization

The PLL-based clock generator in a typical SMPTE292M serializer introduces significant jitter when it multiplies the 74.25 MHz external reference clock to 1.485 GHz for timing the uncompressed serial data. In order to minimize the jitter, a stand-alone crystal clock oscillator, such as the [S1613](#) (3.3V) or [S1614](#) series (2.5V) with less than 30ps total peak-peak jitter, is recommended. Alternatively, the reference VCXO for a local deserializer may be shared.

SaRonix Solution: Deserialization

Although minimizing jitter in the serialization of uncompressed HD video streams is beneficial, the more critical point of jitter control is the deserialization process. To minimize jitter, typical SMPTE292M deserializers use a FIFO and an external, low-jitter oscillator operating at the parallel data rate to retime the parallel data recovered from the serial stream.

Due to the nature of HD Video formatting, the reference oscillator used for deserialization also serves a role in the clock and data recovery function of most SMPTE292M-compatible deserializers. Since HD Video may exhibit several dozen consecutive transition-free bits, conventional silicon-only PLL-based CDR often fail to sustain the 1.5 GHz internal PLL used to recover the data, resulting in lost data. To compensate, a voltage-controlled crystal oscillator (VCXO) may be used to provide a continuous reference signal to maintain CDR lock to the incoming signal. Contemporary deserializers, such as National Semiconductor's [CLC031](#), recommend using a low-jitter VCXO at the parallel data rate (74.25 MHz or 74.25/1.001 MHz). The deserializer adjusts the VCXO's output frequency through the voltage control function, pulling the device into phase lock with the clock embedded on the incoming data stream. This provides a continuous phase-locked reference during several dozen transition-free bits.

The [ST1308](#) series (LVTTTL) voltage controlled crystal oscillator offers a wide frequency pull range (+/-50 ppm minimum APR, or as specified) for tracking and locking to the incoming data signal, and tight stability over all operating conditions (+/-25 ppm, or as specified). Since the ST1308 uses non-PLL fundamental crystal Tab Mesa Technology (Tm™), it exhibits less than 25ps total peak-to-peak jitter.

The [ST1317](#) series (LVCMOS/LVTTTL) voltage controlled crystal oscillator offers a far more cost-effective solution than the ST1308 VCXO, however the ST1317 exhibits significantly higher output jitter (100ps total peak-to-peak). The specific application's jitter sensitivity will determine which of these two devices should be specified.

More...

Key Features & Specifications

Parameters	S1613	S1614	ST1308	ST1317
Type	XO	XO	VCXO	VCXO
Package Size (mm)	5 x 7	5 x 7	9 x 14	5 x 7
Frequency (MHz)	74.2500 74.1758	74.2500 74.1758	74.2500 74.1758	74.2500 74.1758
Overall Stability (ppM)	+/-25	+/-25	+/-25	+/-50
Supply Voltage (V)	+3.3	+2.5	+3.3	+3.3
Absolute Pull Range (ppM)	-	-	+/-50	+/-100
Jitter max (ps total peak-peak)	30	30	25	100
Output Logic	LVC MOS LVTTL	LVC MOS LVTTL	LVTTL	LVC MOS LVTTL

Key Benefits

- ❑ Tight frequency stability over all operating conditions, including aging
- ❑ Fundamental or Overtone technology ensures minimal phase noise and low jitter
- ❑ Wide Absolute Pull Range (APR) for tracking and holding ensures continuous frequency source, even upon temporary loss of data signal or data recovery PLL due to sequential transition-free bits
- ❑ Advanced manufacturing processes achieve tight overall stability, including aging

Product Status

- ❑ Samples: Available Today
- ❑ Production: Available Today (S1613, ST1317)
- ❑ Production: Q1-2004 (S1614, ST1308)

Additional Information

- ❑ Order Literature Online
 - <http://www.onfulfillment.com/pericom/>

Contact Information

A sales representative or franchised distributor can be found by visiting: <http://www.pericom.com/contact>