

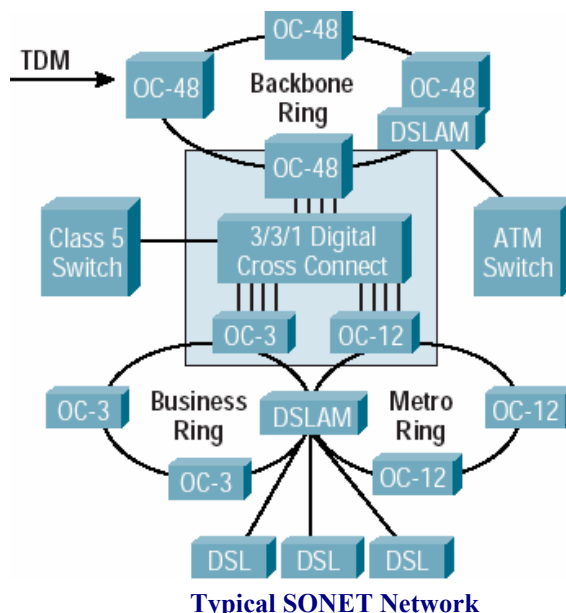
Application: SONET/SDH OC-12 Line Card
Pericom Device: PI6C2502: Zero-Delay Clock Driver

Overview

Synchronous Optical Network (SONET) is a standard for optical telecommunication transport. It was defined by the American National Standards Institute (ANSI) for US standards. The international version of SONET is synchronous digital hierarchy (SDH). The two standards provide the transport infrastructure for worldwide telecommunication network systems. SONET defines optical carrier (OC) levels and electrically equivalent synchronous transport signals (STS) for fiber optic based transmission hierarchy. The base level of OC/STS is OC-1/STS-1 with the bit rate of 51.84Mbps, and the highest bit rate is 40Gbps rate for OC/STS-768.

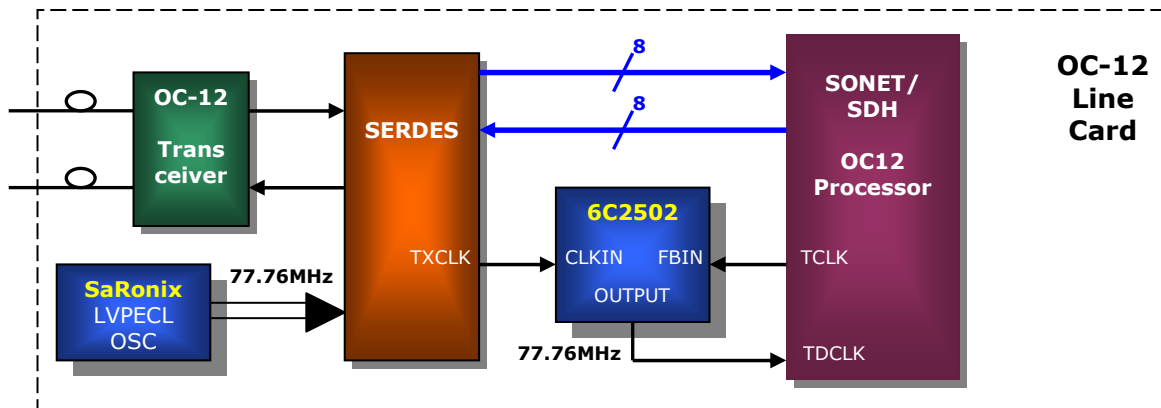
SONET Signal	SDH Signal	Bit Rate
STS/OC-1		51.84Mbps
STS/OC-3	STM-1	155.52Mbps
STS/OC-12	STM-4	622.08Mbps
STS/OC-48	STM-16	2.488Gbps
STS/OC-192	STM-64	9.953Gbps
STS/OC-256		13.271Gbps
STS/OC-384	STM-128	19.906Gbps
STS/OC-768	STM-256	39.813Gbps

SONET/SDH has been used in central office to transmit data in backbones, local loop networks, and metropolitan area networks. The most common speeds of a SONET/SDH network are OC-3, OC-12, and OC48, so the network routers contain multiple interface line cards to communicate with different speed of OC levels. All of the SONET/SDH optical signals are serialized to maintain high-speed data and voice transmission.



Pericom Solution

PI6C2502 is 3.3 volt LVTTL PLL clock driver with up to 80MHz operating frequency. This driver uses external feedback input and output to provide zero-delay, low-jitter, and low-skew outputs. A SERDES (Serializer and Deserializer) is required to convert optical serial input data to parallel the format to a SONET processor. However the transmit timing from a SONET processor to SERDES is delayed, and the PI6C2502 is a perfect solution for this application. 2502 synchronizes the timing between transmit data clock from the SONET processor and the transmit input clock of SERDES. A 77.76 MHz LVPECL clock is used for the OC-12 signal.



Key Features & Specifications

- Operating Frequency up to 80 MHz
- Fast Rise/Fall Time, typical at 1.0ns
- Phase Error between FBIN and CLKIN, less than 150ps
- Low Jitter, less than 100ps
- Low Output-to-Output Skew, less than 200ps
- 45/55% Duty Cycle
- Low Power 3.3V CMOS Technology
- 8-pin SOIC package

Key Benefits

- Spread Spectrum Clock Ready
- Zero-Delay input-to-output clock
- Synchronize clock between CLKIN and FBIN

Product Status

- Samples: Available Today
- Production: Available Today

Pricing

- Budgetary Pricing:
 - PI6C2502 \$1.08 in 10K quantities

Competitive Device Cross-reference

- Cypress: CY2502 (drop-in compatible)
- ICS: ICS571 (functional compatible)

Additional Information

- Website
 - Datasheets, Product Presentation, IBIS, App Notes, Quality & Package Data
- <http://www.pericom.com/pdf/datasheets/PI6C2502.pdf>
- Order Literature Online
<http://www.onfulfillment.com/pericom/>

Contact Information

Please contact your local Pericom Sales Representative or franchised distributor. Contact list provided on the web:
<http://www.pericom.com/contact/index.php>

Application Support:

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