

**Application: DDR SODIMM**  
**Pericom Device: PI6CV855: 1:5 DDR PLL Clock Driver**

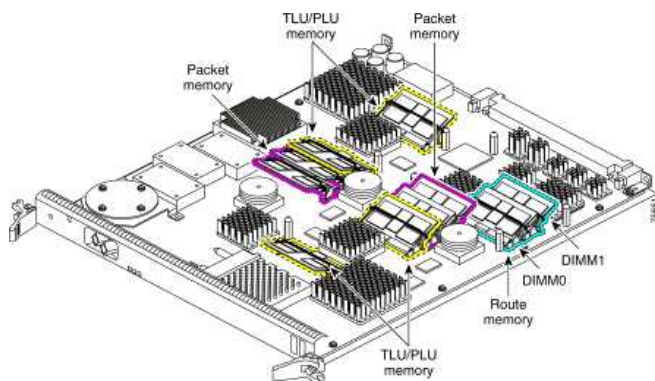
**Overview**

Memory is a place for systems to store and access data and each system requires a large amount of memories. To increase memory expandability and flexibility, all the memories are designed onto a board called Dual Inline Memory Module (DIMM). DIMM is a module with signal and power pins on both sides of the board. In some applications, like a notebook computer with limited space, a smaller and thinner module than DIMM called Small Outline DIMM (SODIMM) is needed. The dimension of SODIMM is around 50% smaller. Memory capacity is also 50% less than DIMM, but the functionality is similar. SODIMMs offer different types and speeds such as PC100, PC133, PC2700, unstacked and stacked. Although all the SODIMMs are unbuffered, some custom SODIMMs are designed with a PLL clock buffer to improve signal integrity, performance stability, and increase memory capacities.



**SODIMM socket inside notebook computer**

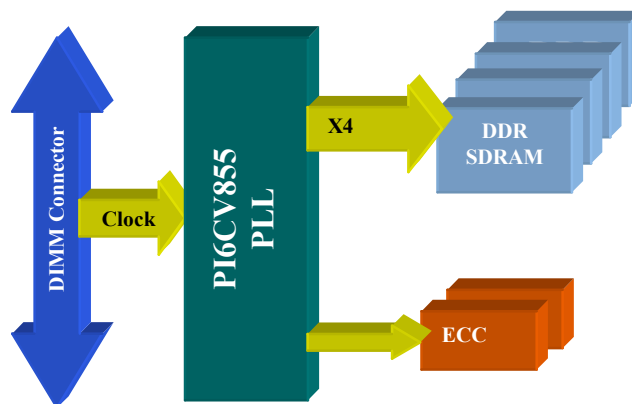
As microprocessor speeds increase along with more memory demanding software, the timing becomes more critical. A high density DDR SODIMM with PLL is designed for applications like networking router, switches, and other high-speed lab equipment.



**Networking device with SODIMMs**

**Pericom Solution**

Pericom's PI6CV855 DDR PLL Clock Driver is ideal for this application because it provides five differential outputs for each SDRAM on DDR SODIMM. Since each output of PI6CV855 supports up to four SDRAMs, it can support up to 1GB stacked ECC DDR SODIMM. ECC (Error Correcting Code) is an extra SDRAM that designed to detect and correct memory errors, and it also requires a clock signal from PLL. PI6CV855 has a maximum frequency of 170MHz (DDR333), low skew, and low jitter to support DDR SODIMM at PC2700 speed.



**Maximum 4 loads for each output**



**DDR PLL Clock Driver**

## Key Features & Specifications

- High-speed 2.5V SSTL<sub>2</sub> clock
- Differential I/O up to 170 MHz
- Five differential outputs
- Maximum output skew = 100ps
- Maximum cycle-to-cycle jitter = ±75ps
- Maximum static phase error = ±50ps
- Maximum cross voltage variance = ±200mV
- Less than 100ps Half-period Jitter
- Less than 75ps Period Jitter
- Better than 49.5/50.5% Duty Cycle
- Spread Spectrum Clock (SSC)
- 28-pin TSSOP Packages
  - [Package Outline Drawings](#)

## Key Benefits

- Low power 2.5V V<sub>DD</sub> and AV<sub>DD</sub>.
- Five outputs support ECC mode.
- External feedback for synchronization.
- Test mode ready when AV<sub>DD</sub> strapped low.
- EMI reduction with SSC.

## Competitive Offerings

- Texas Instruments: CDCV855\*
- Cypress: CY2SSTV855\*
- ICS: ICS93V847

(Note: Functionally compatible, but not pin compatible. TI and Cypress parts are 4 outputs only)

## Additional Information

- Datasheets on the web:  
<http://www.pericom.com/specs/PI6CV855.pdf>
- Web Presentation  
[http://www.pericom.com/presentations/clock\\_ow.pdf](http://www.pericom.com/presentations/clock_ow.pdf)  
(Page 12 for DDR clock specific presentation)
- DDR related websites:  
<http://www.pericom.com/products/ddr00.php>  
<http://www.intel.com/technology/memory/>  
<http://www.jedec.org/>
- Product Selection Guide and Cross Reference ([order](#))
- Applications support  
<http://www.pericom.com/docs/index.php>

## Product Status

Samples: NOW  
Production: NOW  
Lead-Time: 4 Weeks

## Budgetary Pricing

PI6CV855L: 10K units @ \$1.50

## Contact Information

Please contact your local Pericom Sales Representative or franchised distributor. Contact list provided on the web:

<http://www.pericom.com/partners/index.php>

Or

Product Marketing – Jaci Chang

Email: <mailto:jchang@pericom.com>