PI7C9X7958 / PI7C9X7954 / PI7C9X7952 PCIe® UART I/O Bridge
Application Note

1. Introduction

This application brief provides a concise and practical guide for the board designers to easily incorporate the Pericom PCI Express® UART I/O Bridge in their designs. This brief includes design outlines, layout cautions and application reminders, which can help the designers to achieve optimal performance in their systems.

2. Power System

The PCI Express UART I/O Bridge defines six power block types, as indicated in table 2-1.

Table 2-1 DC Electrical Characteristics

Power Pins	Min.	Typ.	Max.
VDDA	1.72V	1.8V	1.9V
VDDR	3.2V	3.3v	3.6V
VDDC	1.72V	1.8V	1.9V
VDDAUX	1.72V	1.8V	1.9V
VDDCAUX	1.72V	1.8V	1.9V
VTT	1.72V	1.8V	1.9V

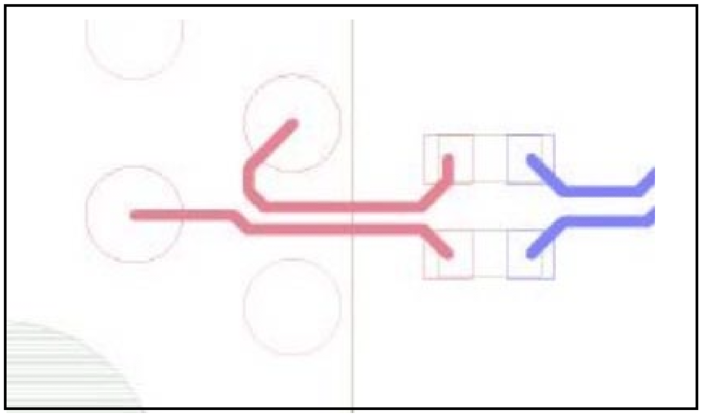
VDDA: analog power supply for PCI Express Interface
VDDR: digital power supply for 3.3v I/O Interface
VDDC: digital power supply for the core
VDDAUX: digital auxiliary power supply for PCI Express Interface
VDDCAUX: digital auxiliary power supply for the core
VTT: transmit termination power supply for PCI Express Interface

Every power pin needs one or more by-pass capacitors (0.1uF ~ 10uF).
By-pass capacitors must be close to the power pins. If it is possible, place the capacitors on the opposite side of the ICs. The power noise must be lower than 5%.

3. Differential Signal (Tx/Rx) Layout Guidelines

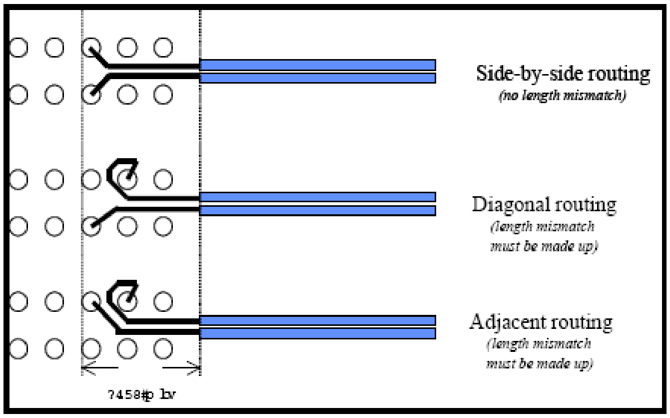
PCI Express is a dual simplex point-to-point serial differential low-voltage interconnect. The bit rate is 2.5 G bit/sec/lane/direction at introduction. The signal is 8b/10b encoded with an embedded clock. Each lane consists of two pairs of differential signals. Differential trace impedance target of 100Ohm with a tolerance of 15% or better is desired. Tight coupling within the differential pair and increased spacing to other differential pairs helps to minimize crosstalk and EMI. If possible, Tx and Rx differential pairs should route alternately on the same layer (Tx pair next to a Rx pair rather than another Tx pair) to help minimize FEXT.

AC coupling capacitors of 100 nF should be placed at the same location (as close as possible) and should not be staggered from one trace to the other within the pair. While size 0603 capacitors are acceptable, size 0402 capacitors are strongly encouraged. C-packs are not allowed for AC coupling capacitors. The exact same package size of capacitor should be used for each signal in a differential pair. Pad sizes for each of the capacitors should be minimized. The “breakout” into and out of the capacitors should be symmetrical for both signal traces in a differential pair.



From our experience, the high-speed transmission line design is very important and a good transmission line design is a critical factor to achieve good signal quality. If the PCB design can be further improved, especially the traces of the TX and RX of the PCIe lanes, and the reference clock, the overall system stability should be improved.

Breakout Areas near a device package that resulted in “neck-downs” and decreased spacing should be limited to no more than 500 mils in lengths. The necking-down should be done symmetrically on both nets of the differential pair. Breakout sections require special attention to minimize crosstalk.



Test points and probing structures may impact the loss and jitter budgets. If possible, test points and probe structures should not introduce stubs on the differential pairs.

4. Reference Clock Input Pairs

The reference clock input pins connect to external 100MHz differential clock. The signal must match to LVPECL or HCSL spec.

A 100nF capacitor should be placed between the clock source and the I/O Bridge. The purpose of this capacitor is to achieve AC coupling. This AC Coupling ensures the I/O Bridge is compatible with the differential clock signals regardless the type of the clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered.

5. Physical Layer Setting (via EEPROM Setting)

The PCI Express UART I/O Bridge supports physical signal fine-tuning. It can be achieved using hardware strapped pins or EEPROM.
Table 4-1 / 4-2 / 4-3 show the common configurations used by all the parts in the UART I/O Bridge family. Please consult the datasheet specific to the part for more details.

Table 4-1 Nominal Driver Current Values (Inom)

HIDRV	LODRV	NOMINAL DRIVER CURENT
0	0	20 mA
0	1	10 mA
1	0	28 mA
1	1	Reserved

Table 4-2 Ratio of Actual Current and Nominal Current

DTX [3:0]	ACTUAL CURRENT / NOMINAL CURRENT
0000	1.00
0001	1.05
0010	1.10
0011	1.15
0100	1.20
0101	1.25
0110	1.30
0111	1.35
1000	0.60
1001	0.65
1010	0.70
1011	0.75
1100	0.80
1101	0.85
1110	0.90
1111	0.95

Note: The default value of the registers DTX[3:0] is "0000".

Table 4-3 De-emphasis Level versus DEQ [3:0]

DEQ [3:0]	$(I_{TX} - I_{EO}) / I_{TX}$	De-emphasis (dB)
0000	1.00	0.00
0001	0.96	-0.35
0010	0.92	-0.72
0011	0.88	-1.11
0100	0.84	-1.51
0101	0.80	-1.94
0110	0.76	-2.38
0111	0.72	-2.85
1000	0.68	-3.35
1001	0.64	-3.88
1010	0.60	-4.44
1011	0.56	-5.04
1100	0.52	-5.68
1101	0.48	-6.38
1110	0.44	-7.13
1111	0.40	-7.96

Note: The default value of the registers DEQ[3:0] is "1000".

6. EEPROM Type

PCI Express UART I/O Bridge supports only **93C56** EEPROM (such as AT93C56 and ISSI93C56).

7. RS232 / RS422 / RS485 Mode Control

PCI Express UART I/O Bridge supports the RS232 / RS422 / RS485 2W / RS485 4W modes. User can modify the register offset B4H to select the mode. Alternatively, user can program the EEPROM offset 12H to select the mode at power-on.

The control pins' outputs define the UART mode.
UARTx_Drive[0] indicates the RS232 transceiver control mode (High Enable).
UARTx_Drive[1~3] indicate EIA 422/485 transceiver control mode.

Function	485EN0	485EN1	485EN2	232EN
RS232	0	0	1	1
RS422	1	0	0	0
485-4W□	ADDC	0	0	0
485-2W	0	ADDC	ADDC	0

```
UARTX_DRIVE[0] => RS232EAN
UARTX_DRIVE[1] => RS485_EN2
UARTX_DRIVE[2] => RS485_EN1
UARTX_DRIVE[3] => RS485_EN0
```

8. RI Function (Ring Indicator for Wake-Up)

The Pericom PCI Express UART I/O Bridge's UART port 0 supports RI function.

This function is enabled by the PME_ENA pin pull high and the Wake_up# pin must connect to the Slot B11 pin (WAKE#). When the modem sends the RI signal to UART port 0, The PCI Express UART I/O Bridge will wake up the system.