

Differences of Pericom SuperClocks and Competitor Programmable Skew Clocks

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Introduction

Timing is everything. A little too slow or a little too fast can result in a system crash. Pericom's SuperClock's offer a simple solution to these complex problems. SuperClock's are low-skew, low-jitter, Phase Locked Loop (PLL), programmable skew clock drivers. These are available in 5V and 3.3V, with a maximum frequency of 125 MHz. Pericom SuperClock's are "drop-in" compatible with the competitor clock offering with pin-to-pin compatibility replacement to existing board layouts.

Functionality wise, Pericom SuperClocks and the competitor's programmable skew clock both offer user selectable skew control for four output pairs, thus providing the proper timing necessary to optimize a systems timing requirements. Each output can be configured to one of nine delays in addition to some function configurations.

The 3.3V SuperClocks offer the option of having the outputs signal to synchronize on the rising or falling edge of the input clock signal. With Pericom's 3.3V SuperClocks, part numbers with the "A" suffix, the 3Qx outputs are synchronized on the clocks input rising edge, and 4Qx outputs are synchronized the clock's input on the falling edge (competitor compatible, see Figure 2). For 3.3V SuperClocks part number without the "A" suffix, the 3Qx and 4Qx outputs are synchronized on the rising edge of the clock's input (see Figure 1).

The following figures show the differences between Pericom PI6C3991 and PI6C3991A, or PI6C39911 and PI6C39911A. The alignment between 3Qx and 4Qx only applies with the following setting below:

3F1 & 3F0 = HIGH (3Qx outputs = +4)

4F1 & 4F0 = LOW (4Qx outputs = +2)

Alignment between	PI6C3991 & PI6C39911		PI6C3991A & PI6C39911A	
3Qx & REF	3Qx Rising Edge	REF Rising Edge	3Qx Rising Edge	REF Rising Edge
4Qx & REF	4Qx Rising Edge	REF Rising Edge	4Qx Rising Edge	REF Rising Edge
3Qx & 4Qx	3Qx Rising Edge	4Qx Rising Edge	3Qx Rising Edge	4Qx Falling Edge

PI6C3991A SuperClocks

The 3991A SuperClock's allow the REF (input) frequency to be divided by two on outputs 3Qx and 4Qx, or divided by four on 3Qx, or the inverted REF frequency on 4Qx, depending on the

selected configurations.

Most functions defined above are similar to competitor programmable skew clock. Performance wise, they are also very similar. In addition to "drop-in" compatibility, Pericom's SuperClock's offer the following advantages over competitor.

Power Sequencing

Pericom's SuperClocks do not need power sequencing. REF input clock can have input signal at any time regardless of the power condition. This advantage applies to both Pericom's 3.3V and 5V SuperClocks. With competitor 3.3V clocks, when the FS pin is selected HIGH, it requires that no input signal is applied to the REF pin upon power-up until V_{CC} has reached 2.8V. Similarly, the competitor's 5V clocks require that no input signal should be applied to the REF pin until V_{CC} has reached 4.3V.

SuperClock Advantages Over Competitor

1. SuperClocks without the "A" suffix have 4Qx output aligning with the falling edge of the input clock signal.
2. There is no limitation regarding power sequencing, meaning input signal can be applied to the REF pin regardless of V_{CC} condition.
3. Pericom has lower power consumption. Power consumption can be 50% or less.

Competitor Disadvantages

- Requires special Power-On condition.
- REF input MUST not transition upon power-on until V_{CC} has reached 2.8V
- For 5V competitor clock, the REF input MUST not transition upon power-on until V_{CC} has reached 4.3V
- 4Qx output can only be synchronized on the rising edge

Part numbers with 3Qx and 4Qx aligned:

PI6C3991
 PI6C3991-I
 PI6C3991-2
 PI6C3991-5
 PI6C3991-5I
 PI6C39911
 PI6C39911-2
 PI6C39911-5

Part numbers that are competitor compatible

PI6C3991A
 PI6C3991A-I
 PI6C3991A-2
 PI6C3991A-5
 PI6C3991A-5I
 PI6C39911A
 PI6C39911A-2
 PI6C39911A-5

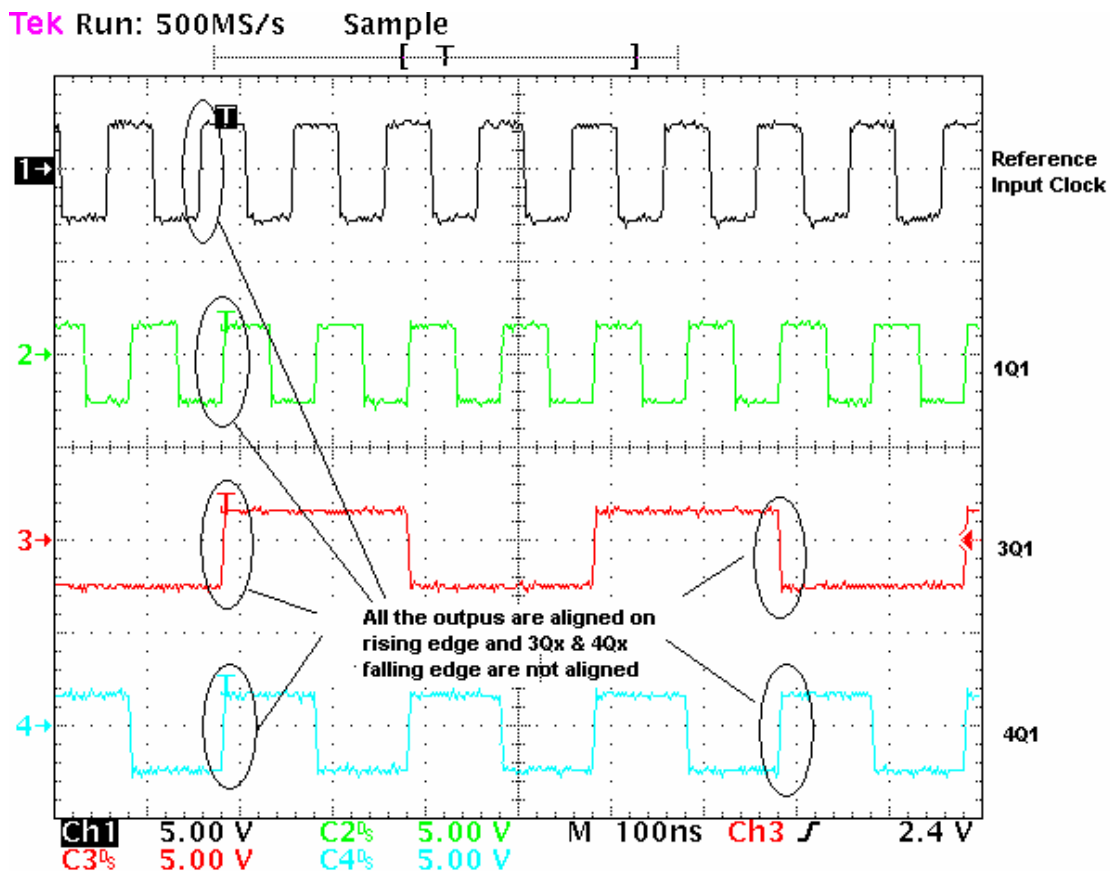
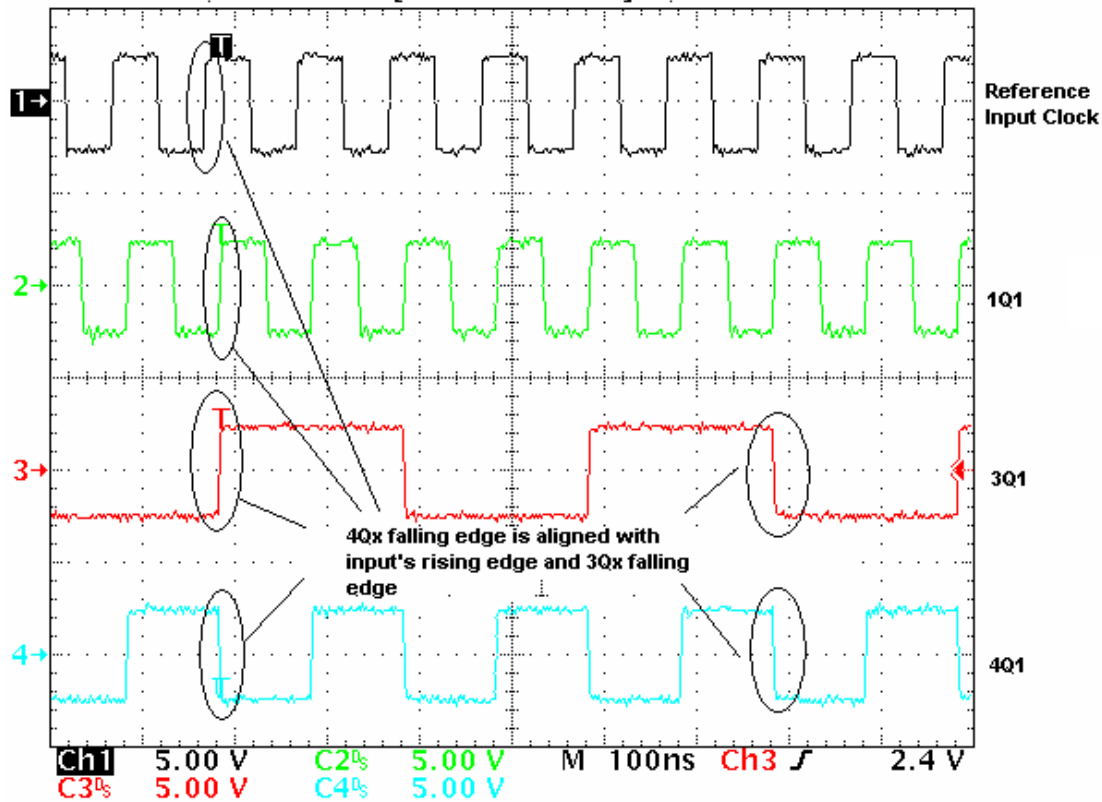


Figure 1. Pericom SuperClock's 3Qx and 4Qx output synchronizing on the rising edge

Tek Run: 500MS/s Sample



Board setting:

FS: M
TEST: L
1F1/0: MM
2F1/0: MM
3F1/0: HH
4F1/0: LL

Figure 2. Pericom's SuperClocks and competitor clocks 3Qx output synchronizing on the rising edge and 4Qx output synchronizing on the falling edge