Schematic and Layout Guidelines for PI7AT04

By Jimmy Ma

Introduction

As speed increases, the paths which allow data transmission can no longer be considered as simple copper wires, but as complex transmission lines. Reflection, overshoot, and undershoot are commonly associated with transmission lines. Many times, traditional termination such as series termination, AC termination, and diode termination are used to minimize the unwanted burden of the transmission line effects. As an alternative to traditional terminations, Pericom offers the PI7AT04 active clamping device. This application note will discuss some layout techniques to get the best performance out of the PI7AT04.

PI7AT04

The PI7AT04 actively clamps overshoot and undershoot voltages on transmission lines and backplanes. The PI7AT04 provides up to four line terminations and can be used in 5V or 3.3V applications. The PI7AT04 can work with frequency up to 133 MHz depending on the application. Pericom's active terminator works most effectively in a point-to-point application.

Decoupling Capacitor

Decoupling capacitors are very critical in terms of limiting noise. Without proper decoupling capacitors to minimize heavy VDD ripple and GND bounce, it can cause system-false triggering or may even cause complete system failure.

Noise on the VDD line (ripples) and GND (GND bounce) can also drastically increase skew and output jitter. To minimize noise to the device's VDD and GND, a high-frequency ceramic (surface mount recommended) 0.47µF and a 0.01µF bypass capacitor should be connected as close as possible between VDD pin and GND pin. In addition to the 0.47µF and a 0.01µF, there should also be sufficient amounts of decoupling capacitors added to the main power supply. A recommendation is to have 10µF capacitors distributed throughout the board for every 1.5 or 2 inches.

PC Board Consideration

It is recommended that at least four PCB layers be used with the signal layers separated by the GND and power planes. Typical stacking for a four layer board is as follows: Primary signal on the top layer followed by the GND plane, then a power plane, and finally the bottom layer for secondary signal. The same stacking technique for a four-layer board should also be applied to the PCB with more than four layers stacking. Figure 1 below shows the stacking for a four layers PC board.

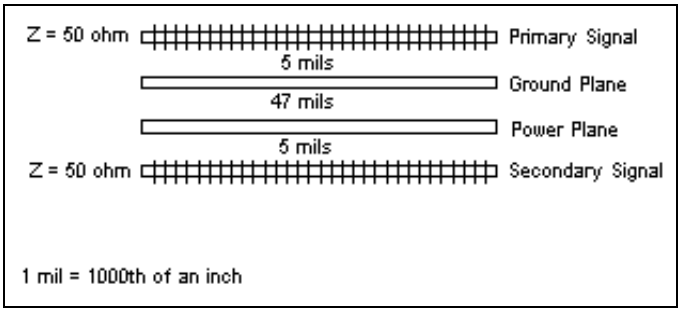

Figure 1. Four Layer Board Stackup

Placement of the PI7AT04

The PI7AT04 should be placed as close as possible to the receiver's input as shown is Figure 2. Figure 3 shows a before and after picture when using the PI7AT04. The PI7AT04 should be no more then 1/4 inch away from the receiver's input. Again, placing the PI7AT04 as close as possible to the receiver's input will provide the best results.

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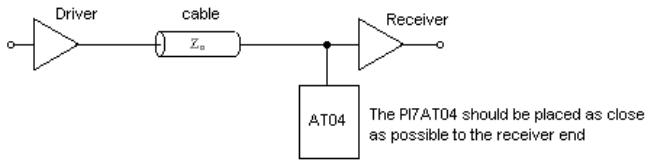

Figure 2. A point-to-point application for the PI7AT04

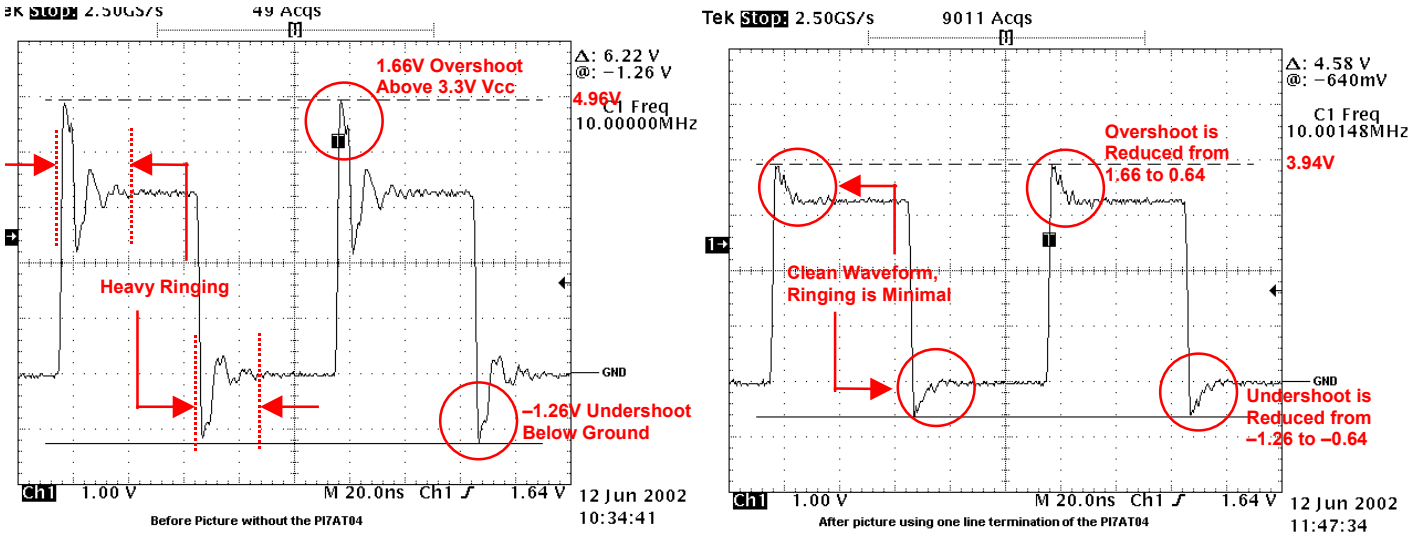

Figure 3. Before (left) and after (right) picture of waveform when using the PI7AT04

Increasing Clamping Effective for the PI7AT04

When needed, shorting another line termination together can increase the clamping effect of overshoot and undershoot. The more line terminations that are used, the better the clamping effect. Figure 4 shows the waveform without the PI7AT04, one line termination, two line terminations, and four line terminations of the PI7AT04, respectively.

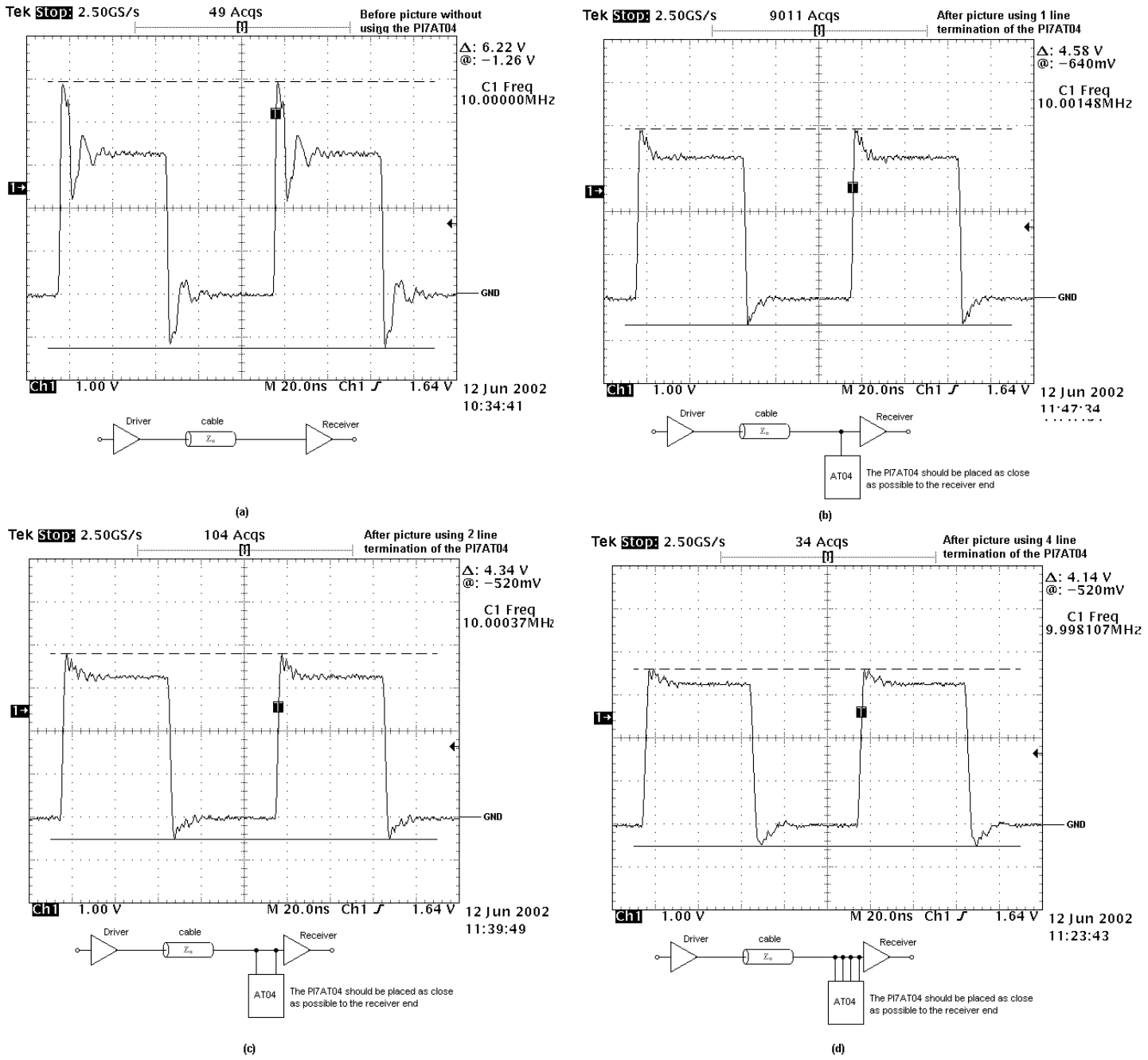

Figure 4. Clamping effect with increase in line termination. Line terminations shorted together to increase clamping effect. Top left: Without PI7AT04; Top right: 1 line termination of PI7AT04; Bottom left: 2 line terminations of PI7AT04; Bottom right: 4 line termination of PI7AT04

Schematics and Layout for PI7AT04

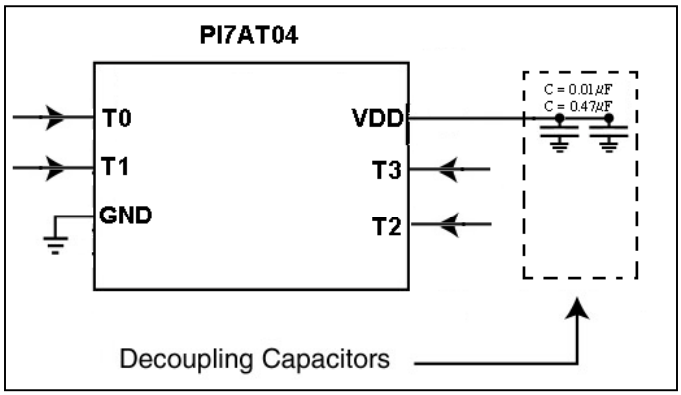

Figure 5. Schematic for the PI7AT04 with decoupling capacitors

Recommendations

1. A 0.47µF and a 0.01µF decoupling capacitors should be connected between the VDD and GND for all VDD pins. Placement of decoupling capacitors should be connected as close as possible to the VDD pin of the device (within 2mm recommended).

2. In addition to the 0.47µF and a 0.01µF decoupling capacitors connected between VDD and GND of the device, there should be sufficient amount of capacitance added to the main power supply.

3. Distribute 10µF capacitors every 1.5 or 2 inches throughout the board.

4. Use solid VDD and GND planes.

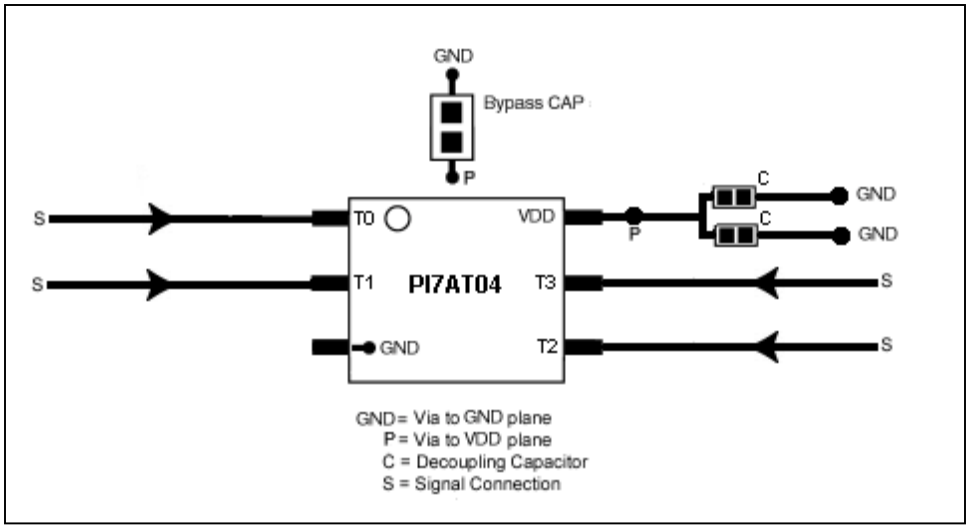

Figure 6. Layout for the PI7AT04 with decoupling capacitors

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